DESCRIPTION OF FREQUENCY DETERMINING AND STABILING CIRCUIT

2.1 INTRODUCTION

The frequencies for transmitter and receiver local frequencies are all drived from a single 4.0 (MHz) crystal by means of a CPU, U203. The first local oscillator frequency is 10.7MHz below the incoming frequency. The CPU generates the fundamental frequency and controls the VCO, Q1502& Q1501.

During transmit, the VCO of the PLL can only operate 144.000 MHz to 148.000MHz.

The VCO operating frequency for the receiver is 121.300MHz to 168.300MHz at the as the first local oscillator, injected through the buffer AMP Q13 into the first TR Mixer Q4.

2.2 DESCRIPTIONS OF EACH BLOCK

(1) INTRODUCTION

The synthesizer is implemented with the following components: PLL IC U203, Q1501 & Q1502 VCO, VARICAP Diode D9

The CPU U203 is a CMOS LSI that includes prescaller, the U204, U206, U207, U208 Varicap. Transistor Q10 is clapp oscillator circuit to operate as part of the VCO. The Q28/Q29 are switch transistor to connect or disconnect the tuning capacitor in the VCO oscillator tank circuit for transmitter or receiver. The Q13 works as a buffer AMP for RX local frequencies and TX carrier generating frequencies.

(2) REFERENCE FREQUENCY

The 4.0MHz Crystal, make a reference frequency oscillator with internal amplifier.

(3) VCO

The Q1501 & Q1502 and surrounding parts are consisting a clapp oscillator works a VCO of U4 & U203 with appropriate control voltage on D301. The VCO can be oscillate over the required range of 121.3MHz to 168.3MHz.

(4) PROGRAMMABLE DIVIDER AND ITS CONTROL

The programmable inputs for each channels are setted IC inside.

Each input signal to control the CPU is done with the provided AAR-147 DTMF BOARD.

Key Matrix input pins – PIN25 to PIN28 and for each key matrix input, an internal code convert EPROM provides the appropriate binary control to the u1 & u2, U3 for that channel. Since the binary number necessary to change during transmit and receive, an additional bit is required at CPU to allow the ROM to recognizing the status is TX or RX. During transmit, the push to talk switch makes PIN.42 of CPU IC is hi digitally under transmit mode. The programmable divider to PLL. The output is fed to the phase detector for comparing with the reference frequency inside.

(5) PHASE DETECTOR AND VCO CONTROL

The phase detector is a digital phase comparator which compares the phase of the reference signal with programmable divider output square waves and develops a series of pulses whose DC level depends on the phase error of each signal. The phase detector pulse output is fed to an active low pass filter, and fed to varicap D9 control the VCO frequency.

(6) TRANSMITTER/RECEIVER BUFFER/AMP

Output signal of Q1502 is fed into the buffer AMP Q13 to increase the strength of TX carrier frequency and first local frequencies.

(7) SWITCHING OF TUNING CAPACITOR IN VCO

The VCO circuit must tune with a wide range of frequencies 132-179.00MHz for the receiver and 144.00 to 148.00MHz for the transmitter.

To comply above range of VCO, the tuning capacitance should switched for transmission or reception. The tuning circuit consists with Q1402, U1401 q1404, Q1403 & LPF. when the VCO is working as a TX, the voltage is turned off of the receiver

(8) RECEIVER LOCAL OSCILLATOR OUTPUTS

1st MIXER: The output signals of D11 is injected to the sources of 1st mixer Q4 in the 1st mixer section.

FM signals are recovered with envelope detector.