Functional Description
For Enfora Enabler-A
CDPD Modem

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1. CDPD Background

The Cellular Digital Packet Data (CDPD) network is a two-way wireless data communication system. This system uses cellular telephone channels to transfer data seamlessly from a mobile end system. CDPD operates within the already existing cellular telephone infrastructure utilizing the idle time that exist on cellular voice channels to send small packets of data, called datagrams, to a designated receiver. Researchers estimate that over 30% of a cellular channel's airtime is idle, even during heavy traffic.

The CDPD system sends down the various cellular channels to locate an open channel. This process is called "sniffing." Once the CDPD system has located an open channel, the modem begins to send datagrams over the channel to the designated end user. In order that this process does not interfere with the cellular phone transmission, the CDPD system has regulated channel "hops" to ensure that CDPD usage will not block a cellular voice channel for an extended period of time. Also, if a voice channel is activated, the CDPD system detects this voice message and automatically "hops" to the next available idle channel. This process is quite complex. However, the user need not be aware of this process. The CDPD system manages the routing of the individual data packets to the proper destination.

On a basic level, the CDPD network operates like any other computer network with the exception that the CDPD mobile end system is free to roam wirelessly and conduct network operation from other locations using the network of cellular carriers. The CDPD network is made of a series of cellular networks that are operated by various cellular carriers. These carriers provide the user with network management as well as application services. To increase user security carriers use forward error correction, authentication, and encryption. The cellular carrier is responsible for all accounting services for the CDPD service.

The user selects the CDPD carrier service with which to operate by registering with an individual carrier. Generally, an area will have two cellular carriers that provide CDPD service. The user may sign up with either of the two carriers.

2. Theory of Operation

2.1 Introduction

Enfora's Enabler-A CDPD M-ES RF circuitry may be divided into 3 major sections namely, 2 independent sections, the RX circuit, and the TX circuit and LO's in which the RX circuit and TX circuits depend on for proper operation.

The RX section uses a dual conversion superheterodyne technology to downconvert the cellular RF channel signal to its 1st IF of 45 MHz and then to the 2nd IF of 60 KHz. IF pre-filtering is performed at 45 MHz but the main IF filtering is performed at 60 KHz inside the Sony CXA1742Q device.

For the TX section, the I & Q waveforms from the FPGA output are conditioned and filtered before they are modulated and upconverted to the 836.01 MHz (±12.5 MHz) transmit frequency. Mixing 90 MHz with the Main LO derives the TX frequency.

The receive channel and transmit channel frequencies are always 45 MHz apart from each other with an allocated channel BW of 30 KHz. The 30 KHz BW is also known as the channel spacing. The M-ES transmit frequency band is from 824 MHz to 849 MHz. The M-ES receive frequency band is from 869 MHz to 894 MHz. The band gap between the highest transmit frequency (849 MHz) and the lowest receive frequency (869 MHz) is 20 MHz. The minimum specified receive RF signal level at the antenna port is -111 dBm, GMSK modulated. The maximum specified transmit RF signal level at the antenna port is +28 dBm, GMSK modulated. These 2 signal levels represent the extremes at which the M-ES RX and TX section must operate independently at full duplex mode.

2.2 Abbreviations

CDPD	Cellular Digital Packet Data
RF	Radio Frequency
IF	Intermediate Frequency
GMSK	Gaussian Magnitude Shift Keying
FM	Frequency Modulation
DAC	Digital to Analog Converter
RX	Receiver
TX	Transmitter
LO	Local Oscillator
VCO	Voltage Control Oscillator
LNA	Low Noise Amplifier
NF	Noise Figure
dBm	Signal level in milliwatt
PA	Power Amplifier
BW	Bandwidth
RBW	Resolution Bandwidth
RSSI	Receive Signal Strength Indicator
BER	Bit Error rate
SNR	Signal to Noise Ratio
M-ES	Mobile End System
MDBS	Mobile Data Base Station
BIT	Build In Test
~	Notes an active low signal

2.3 Frequency Allocation (M-ES)

Table 1.1.2 shows the frequency parameters for the CDPD M-ES RX and TX sections.

Table 1.1.2

Channel Number (N)	CDPD M-ES TX Frequency (MHz)	CDPD M-ES RX Frequency (MHz)	Main LO Frequency (MHz)
1	825.03	870.03	915.03
367	836.01	881.01	926.01
799	848.97	893.97	938.97
990 (not used)	824.01	869.01	914.01
991(wrap-around)	824.04	869.04	914.04
1023(wrap-around)	825.00	870.00	915.00

For Channel number
$1 \leq N \leq 799$

TX frequency (MHz) = (0.03 x N) + 825.00
RX frequency (MHz) = (0.03 x N) + 870.00
LO frequency (MHz) = (0.03 x N) + 915.00

For Channel number
$990 \leq N \leq 1023$
(Wrap around Channel)

TX frequency (MHz) = (0.03 x [N-1023]) + 825.00
RX frequency (MHz) = (0.03 x [N-1023]) + 870.00
LO frequency (MHz) = (0.03 x [N-1023]) + 915.00

2.3.1 Power control

Power comes in at a range of 3.15 to 4.2 VDC. Using LDO regulators the system voltages are derived:

3.0 VDIG – This provides the voltage required by the main processor and the AVR processor.

3.0 VOSC – Control is on when modem is not in sleep mode (“XON” is high). This powers up the 15.36 MHz oscillator and CMOS conditioning devices. There is provision to prevent the clock from powering up the synthesizer devices when “RXPOW” or “TXPOW” is low. The AVR controls the frequency accuracy and is set at the factory test.

3.0 VTX – Control is through signal “TXPOW”. This provides a regulated voltage used in the transmitter section to form I&Q and to modulate the TX.

3.0 VRX – Control is through signal “RXPOW”. This provides a regulated voltage used by the RX section.

3.0 VXIL – Control is through the AVR “XON”. This supplies voltage to the FPGA and is powered off during sleep.

2.4 Digital Section

The PCB consists of a processor, flash memory for program storage, and DRAM for program execution. The FPGA connects the Modem to the host through the AT90LS8535 (AVR). It also provides interface logic for RF tuning, data conversion for transmit and receive, demodulator and data bit recovered clock, and some of the BIT interface. The FPGA also works as an I&Q generator to form the GMSK modulation for transmission.

2.4.1 Processor and Memory

The processor provides the command set for communicating to the host PC, top level protocol, including Reed-Solomon Coding, and the command structure for interface, normal and BITE, for the rest of the Modem.

The first action taken is the AVR releases the modem processor from reset and turns on the voltage for the main clock (15.36 MHz) and FPGA. The main processor will then transfer the program from FLASH into DRAM for 16-bit execution. The DRAM device is set up to be high and low word data. During this time all default values of the processor output lines are set.

The second function provided at power up is the programming of the FPGA device, commanding all registers to their default value. This is done across the parallel bus.

2.4.2 I&Q Generation and Transmission Control

The FPGA provides the I&Q signals that are filtered and sent to the modulator. The processor sends up to 96 bytes of data to a FIFO in the FPGA. The state machine within the FPGA writes the appropriate digital word to internal PWM that form the signals. There is debug provision to transmit all 1's, all 0's, CW carrier, and pseudo-random modes. Signals provided by the FPGA to facilitate a transmission are as follows:

TXPOW – controls the regulator and synthesizer reference clock.
TXEN – controls the Filter, Mixer and modulator active states.
TPC – A dc voltage from the AVR PWM, which the power control circuit uses to reach a specific power level. The P.A. power control is accomplished through the use of a current feedback control amplifier that senses the current from the battery to the P.A. and compares to the TPC signal. The power control table is stored within system memory.

2.4.3 ADC – System and Data

The AVR has 8 channels of ADC available. The main processor requests that measurements be made and the AVR responds with the appropriate channel information. The channels used are:
PA_TEMP – This reports the temperature near the PA.

RSSI – Receive Signal Strength Indication.

VCC/2 – Incoming voltage divided by two.

DMLD – Demodulator lock detect.

IFBB – IF Baseband. BIT purposes.

ADC1 – External ADC channel.

ADC2 – External ADC channel.

There are two comparators that provide the digitized data signals “DMLT” and DMHT”. These signals take the IFBB signal from the discriminator and digitize it for the demodulator within the FPGA. The FPGA has a state machine within it that will load the serial demodulated data and format and store in a 32 byte FIFO for the processor.

2.4.4 Debug Serial Interface

The serial interface pins of the processor are the mode pins immediately after reset is released. The three pins are RX, TX, and SCLK. The signal names on the schematic for these pins are “RXCOMM”,”TXCOMM”.

2.4.5 FPGA Functions

As the heart of the modem, there are many functions that the FPGA provides. From the host perspective, it supplies the main processor with interface to the AVR. From the modem processor side it provides the means to communicate and control the RF section and to respond to the host commands or data flow manager. It also provides the means for the Spider Modem Manager software to communicate to the modem processor, giving channel number, RSSI, IP control and several other functions and reports to the user’s screen. The UART function itself is provided by the AVR.

2.5 RF interface and Frequency Generation

The RF section control is done by a parallel to serial translator for programming the synthesizers and register locations for the static signals. Power control was discussed above in section 2.3.1. The I&Q generation was discussed in section 2.4.2. The ADC section is discussed in section 2.4.3.

Frequency generation for the RF Section is accomplished through the use of two synthesizers fed from the system 15.36 MHz oscillator. The synthesizers are programmed using 24 bit serial data from the FPGA. Frequency stability is achieved through the use of a temperature compensated main oscillator (15.36 MHz) with a stability rate of 2.5 ppm. A dual synthesizer chip generates the Main LO (915-939 MHz) and RXLO (89.88 MHz). A discrete VCO/PLL circuit generates the TXLO (90 MHz).

2.6 Receiver Section

2.6.1 Duplexer

The received RF signal level may be injected at the main antenna port. This signal is connected to the Duplexer (FL2, Ant port) via a low loss 50-ohm transmission line. The duplexer is a low loss RF signal combiner and an extremely high performance RF filter built into one structure. The function of the duplexer is to suppress the RF signal and noise generated by the transmitter in the receive band. Since the minimum receive RF level is -111 dBm and the transmit RF level is +28 dBm, the isolation between transmit signal level and receive signal level at 20 MHz apart must be at least 139 dB. The duplexer provides a majority of the isolation. The duplexer must also provide minimum loss for the TX RF signal and RX RF signal to reduce current consumption and improve sensitivity, respectively. 3.5 dB of insertion loss in the RX section of duplexer is typical. Higher loss will result in degradation in sensitivity performance.

2.6.2 LNA and First Conversion

The LNA/downconverter chip is a multi-purpose device that provides low noise amplification of the receive signal and mixes the signal with the main LO to produce the RXIF carrier. A SAW bandpass filter is inserted between the stages to further reduce out-of-band signals first attenuated by the duplexer.

2.6.3 First IF Stage

The RF mixer is configured to perform frequency down conversion from the received cellular channel signal between 869 MHz and 894 MHz to a fixed 45 MHz IF signal. The main LO (926.01 MHz for center band) is injected to mix with the incoming signal.

The output of the downconverter is a high impedance port which is coupled into a tuned RF stage to provide an optimum Q for the 45 MHz IF. The purpose of the RF tuning stage is to match the monolithic crystal filter. It also maximizes the SNR of the 45 MHz IF at the input sensitivity level.

The 45 MHz monolithic crystal filter has a minimum BW of about 30 KHz. The filter is followed by a IF amplifier that provides additional isolation and gain.

2.6.4 Second Conversion, Limiter and IF filtering

The 45 MHz 1st IF is downconverted to a 60 KHz 2nd IF through a mixer in the FM IF chip. It incorporates a mixer, two limiting IF amplifiers, quadrature detector, logarithmic RSSI and driver, voltage regulator and internal audio amplifier and 60 KHz filtering. The external RXLO is phase locked at 89.88 MHz and injected into the FM IF system. The chip divides the LO in half and uses that to mix with the incoming 45 MHz to produce the 60 KHz internal to the chip. The IF baseband signal (GMSK data) is obtained from

the internal audio amplifier output. The GMSK data is fed to comparators that send the digitized data to the FPGA.

2.7 Transmit Path

The input to the modulator is a filtered I&Q signal. As discussed earlier, the processor fills the transmit FIFO in the FPGA. A state machine within the FPGA, takes the parallel data, converts it to a serial bit stream at 19.2 KHz and splits the data into sine and cosine values. These signals are then measured from bit to bit to determine whether an unchanged or changed signal state has occurred. There is a waveform table for each state. This data is written to the PWM and the resultant waveform is created. The modulator uses the I&Q to mix with the TX frequency (836.01 MHz center channel).

A mixer is used to create the TX frequency by mixing the Main LO with 90 MHz. This is buffered and then filtered to prevent spuruious frequencies from being transmitted. Another SAW filter removes any harmonics amplified by the modulator stage. An additional pad provides isolation between the filter and the PA input stage.

The PA receives it power directly from the external voltage source and is controlled by a current sensing feedback amplifier. The output tuning of the PA is designed to limit the maximum available power from the amplifier to +30.5 dBm. Subtracting the loss of the duplexer (2.5 dB), the maximum achievable output of the modem is +28 dBm.