Functional Description
For Nextcell Pocket Spider
CDPD Modem

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1. CDPD Background

The Cellular Digital Packet Data (CDPD) network is a two-way wireless data communication system. This system uses cellular telephone channels to transfer data seamlessly from a mobile end system. CDPD operates within the already existing cellular telephone infrastructure utilizing the idle time that exist on cellular voice channels to send small packets of data, called datagrams, to a designated receiver. Researchers estimate that over 30% of a cellular channel's airtime is idle, even during heavy traffic.

The CDPD system sends down the various cellular channels to locate an open channel. This process is called "sniffing." Once the CDPD system has located an open channel, the modem begins to send datagrams over the channel to the designated end user. In order that this process does not interfere with the cellular phone transmission, the CDPD system has regulated channel "hops" to ensure that CDPD usage will not block a cellular voice channel for an extended period of time. Also, if a voice channel is activated, the CDPD system detects this voice message and automatically "hops" to the next available idle channel. This process is quite complex. However, the user need not be aware of this process. The CDPD system manages the routing of the individual data packets to the proper destination.

On a basic level, the CDPD network operates like any other computer network with the exception that the CDPD mobile end system is free to roam wirelessly and conduct network operation from other locations using the network of cellular carriers. The CDPD network is made of a series of cellular networks that are operated by various cellular carriers. These carriers provide the user with network management as well as application services. To increase user security carriers use forward error correction, authentication, and encryption. The cellular carrier is responsible for all accounting services for the CDPD service.

The user selects the CDPD carrier service with which to operate by registering with an individual carrier. Generally, an area will have two cellular carriers that provide CDPD service. The user may sign up with either of the two carriers.

2. Theory of Operation

2.1 Introduction

Nextcell's Pocket Spider CDPD M-ES RF circuitry may be divided into 3 major sections namely, 2 independent sections, the RX circuit, and the TX circuit and LO's in which the RX circuit and TX circuits depend on for proper operation.

The RX section uses a dual conversion superheterodyne technology to downconvert the cellular RF channel signal to its 1st IF of 45 MHz and then to the 2nd IF of 90 KHz. IF pre-filtering is performed at 45 MHz but the main IF filtering is performed at 90 KHz.

For the TX section, the I & Q waveforms from the microprocessor DAC output are conditioned and filtered before they are modulated and upconverted to the 90 MHz transmit IF. The TX IF frequency has to be upconverted to its final cellular RF channel frequency by mixing with the main LO frequency.

The receive channel and transmit channel frequencies are 45 MHz apart from each other with an allocated channel BW of 30 KHz. The 30 KHz BW is also known as the channel spacing. The M-ES transmit frequency band is from 824 MHz to 849 MHz. The M-ES receive frequency band is from 869 MHz to 894 MHz. The band gap between the highest transmit frequency (849 MHz) and the lowest receive frequency (869 MHz) is 20 MHz. The minimum specified receive RF signal level at the antenna port is -111 dBm, GMSK modulated. The maximum specified transmit RF signal level at the antenna port is +28 dBm, GMSK modulated. These 2 signal levels represent the extremes at which the M-ES RX and TX section must operate independently at full duplex mode.

2.2 Abbreviations

CDPD	Cellular Digital Packet Data
RF	Radio Frequency
IF	Intermediate Frequency
GMSK	Gaussian Magnitude Shift Keying
FM	Frequency Modulation
DAC	Digital to Analog Converter
RX	Receiver
TX	Transmitter
LO	Local Oscillator
VCO	Voltage Control Oscillator
LNA	Low Noise Amplifier
NF	Noise Figure
dBm	Signal level in milliwatt
PA	Power Amplifier
BW	Bandwidth
RBW	Resolution Bandwidth
RSSI	Receive Signal Strength Indicator
BER	Bit Error rate
SNR	Signal to Noise Ratio
M-ES	Mobile End System
MDBS	Mobile Data Base Station
BIT	Build In Test
~	Notes an active low signal

2.3 Frequency Allocation (M-ES)

Table 1.1.2 shows the frequency parameters for the CDPD M-ES RX and TX sections.

Table 1.1.2

Channel Number (N)	CDPD M-ES TX Frequency (MHz)	CDPD M-ES RX Frequency (MHz)	Main LO Frequency (MHz)
1	825.03	870.03	915.03
367	836.01	881.01	926.01
799	848.97	893.97	938.97
990 (not used)	824.01	869.01	914.01
991(wrap-around)	824.04	869.04	914.04
1023(wrap-around)	825.00	870.00	915.00

For Channel number
$1 \leq N \leq 799$

TX frequency (MHz) = (0.03 x N) + 825.00
RX frequency (MHz) = (0.03 x N) + 870.00
LO frequency (MHz) = (0.03 x N) + 915.00

For Channel number
$990 \leq N \leq 1023$
(Wrap around Channel)

TX frequency (MHz) = (0.03 x [N-1023]) + 825.00
RX frequency (MHz) = (0.03 x [N-1023]) + 870.00
LO frequency (MHz) = (0.03 x [N-1023]) + 915.00

2.3.1 Power control

Power comes in from the Lithium Ion battery and goes simultaneously to two low voltage LDO regulators and boost converter that creates the 5.0 volts used in the transmit and receive sections. The frequency of operation is approximately 1.4 MHz. The other voltages required by the system are as follows:

2.8 VOSC – Control is always on. This powers up the 15.36 MHz oscillator and CMOS conditioning devices. The output swing is sufficient for the 3-volt logic. There is provision to prevent the clock from powering up the synthesizer devices when "RXPOW" is low. It is also used to power up the serial DAC. One channel of the DAC controls the frequency of the 15.36 MHz oscillator and the other channel creates the "TPC" or "Transmit Power Control" voltage that changes the gain selection level of the P.A.

2.8 VTX – Control is through signal "TXPOW". This provides a regulated voltage used in the transmitter section to form I&Q and to modulate the TXLO.

4.5 VTR – Control is through signal "TXPOW". This provides a regulated voltage used by the TXIF RF amps.

4.5 VRX – Control is through signal "RXPOW". This provides the voltage used in the entire receive path, up to and including the one bit ADC comparators.

2.4 Digital Section

The PCB consists of a processor, flash memory for program storage, and DRAM for program execution. The FPGA connects the Modem to the host pocket PC. It also provides interface logic for RF tuning, data conversion for transmit and receive, demodulator and data bit recovered clock, and some of the BIT interface. The FPGA also works in conjunction with a serial DAC as an I&Q generator to form the GMSK modulation for transmission. Power conditioning is accomplished through the use of LDO regulators whose input is from the system battery.

2.4.1 Processor and Memory

The processor provides the command set for communicating to the host PC, top level protocol, including Reed-Solomon Coding, and the command structure for interface, normal and BITE, for the rest of the Modem.

The first action taken is the transfer of the program into DRAM for 32-bit execution. The two-DRAM devices are set up to be high and low word data. During this time all default values of the processor output lines are set.

The second function provided at power up is the programming of the FPGA device, commanding all registers to their default value. To accomplish this the serial port is used. A clock rate of approximately 2 MHz is achieved. An 8-bit word is retrieved from the FLASH and stored in a buffer.

2.4.2 I&Q Generation and Transmission Control

The serial DAC provides the interface between the FPGA and the filtering components leading to the modulator. The processor sends up to 96 bytes of data to a FIFO in the FPGA. The state machine within U18 writes the appropriate digital word to first the A then the B channel, then updates both simultaneously. There is debug provision to transmit all 1's, all 0's, CW carrier, and pseudorandom modes. Signals provided by the FPGA to facilitate a transmission are as follows:

TXPOW – controls the regulators.
TXEN – controls the Mixer and a FET switch for power to the transmit chain. The 4.5 VTR is given enough time to fully charge the large capacitors prior to the actual transmission.
TPC – A dc voltage from the serial DAC, which the power control circuit uses to reach a specific power level. The P.A. power control is accomplished through the use of a current feedback control amplifier that senses the current from the battery to the P.A. and compares to the TPC signal. The power control table is stored within system memory.

2.4.3 ADC – System and Data

A 7-channel ADC provides the processor visibility through the FPGA to the analog reporting signals within the system. The channels used are:
PA_TEMP – This reports the temperature near the PA.

RSSI – Receive Signal Strength Indication.
PVSB – divided by two. Battery voltage monitor.

There are two comparators that provide the digitized data signals “DMLT” and DMHT”. These signals take the IFBB signal from the discriminator and digitize it for the demodulator within the FPGA. The FPGA has a state machine within it that will load the serial demodulated data and format and store in a 32 byte FIFO for the processor.

2.4.4 Serial Interface

The serial interface pins of the processor are the mode pins immediately after reset is released. The three pins are RX, TX, and SCLK. The signal names on the schematic for these pins are “RXCOMM”,”TXCOMM”, and “SCKCOMM”. These pins are used for programming the FPGA. SCLK is used as the configuration clock and TX is used as the data bit stream.

2.4.5 FPGA Functions

As the heart of the modem, there are many functions that the FPGA provides. From the PC, or host perspective, it supplies the attribute memory, configuration registers, and the appearance of the parallel side of a 16550 UART. From the modem processor side it provides the means to communicate and control the RF section and to respond to the host commands or data flow manager. It also provides the means for the Spider Modem Manager software to communicate to the modem processor, giving channel number, RSSI, IP control and several other functions and reports to the user’s screen. The device was designed so that any control or data register other than the RX and TX UART registers can be read to or written from either side, host or processor.

2.5 RF interface and Frequency Generation

The RF section control is done by a parallel to serial translator for programming the synthesizers and register locations for the static signals. Power control was discussed above in section 2.3.1. The I&Q generation was discussed in section 2.4.2. The ADC section is discussed in section 2.4.3.

Frequency generation for the RF Section is accomplished through the use of two synthesizers fed from the system 15.36 MHz oscillator. The synthesizers are programmed using 24 bit serial data from the FPGA. Frequency stability is achieved through the use of a temperature compensated main oscillator (15.36 MHz) with a stability rate of 2.5 ppm. A dual synthesizer chip generates the Main LO (915-939 MHz) and TXLO (180 MHz). A discrete VCO/PLL circuit generates the second RXIF LO (44.91 MHz).

2.6 Receiver Section

2.6.1 Duplexer

The received RF signal level may be injected at the main antenna port test connector on the RF PCB. This signal is connected to the Duplexer (FL2, Ant port) via a low loss 50-ohm transmission line. The duplexer is a low loss RF signal combiner and an extremely high performance RF filter built into one structure. The function of the duplexer is to suppress the RF signal and noise generated by the transmitter in the receive band. Since the minimum receive RF level is -111 dBm and the transmit RF level is +28 dBm, the isolation between transmit signal level and receive signal level at 20 MHz apart must be at least 139 dB. The duplexer provides a majority of the isolation. The duplexer must also provide minimum loss for the TX RF signal and RX RF signal to reduce current consumption and improve sensitivity, respectively. 3.5 dB of insertion loss in the RX section of duplexer is typical. Higher loss will result in degradation in sensitivity performance.

2.6.2 LNA and First Conversion

The LNA/downconverter chip is a multi-purpose device that provides low noise amplification of the receive signal and mixes the signal with the main LO to produce the RXIF carrier. A SAW bandpass filter is inserted between the stages to further reduce out-of-band signals first attenuated by the duplexer.

2.6.3 First IF Stage

The RF mixer is configured to perform frequency down conversion from the received cellular channel signal between 869 MHz and 894 MHz to a fixed 45 MHz IF signal. The main LO (926.01 MHz for center band) is injected to mix with the incoming signal. The internal mixer buffer amplifier provides some RF isolation to the input of mixer. The internal LO buffer also provides an alternate output that drives the TX upconverter. The signal from the main LO is padded to reduce unwanted spurious emissions in the buffer amplifier.

The output of the downconverter is a high impedance port which is coupled into a tuned RF stage to provide an optimum Q for the 45 MHz IF. The purpose of the RF tune stage and the matching circuit is to prevent the 2nd and 3rd harmonics of the main LO from being further amplified by IF amplifier. It also maximizes the SNR of the 45 MHz IF at the input sensitivity level.

The IF amplifier provides RF isolation between the tuned stage and the 45 MHz monolithic filter. The 45 MHz monolithic crystal filter has a minimum BW of about 30 KHz. The filter is followed by an additional IF amplifier that provides additional isolation and gain.

2.6.4 Second Conversion, Limiter and IF filtering

The 45 MHz 1st IF is downconverted to a 90 KHz 2nd IF through a mixer in the FM IF chip. It incorporates a mixer, two limiting IF amplifiers, quadrature detector, logarithmic RSSI and driver, voltage regulator and internal audio amplifier. The external 2nd LO is phase locked at 44.91 MHz and injected into the FM IF system. The 2nd IF signal from the first IF amp is connected to a buffer amplifier. The buffer amplifier stage provides SNR improvement and isolation between the mixer and the main IF bandpass filter.

The main IF active bandpass filter is divided into 3 identical sub filter sections. The BW of each individual section is 35 KHz. The cascaded BW of the 3 sections is 23.5 KHz. The 1st and 2nd stage is cascaded and placed before the 1st IF amplifier to reduce intermodulation distortion. The Phase Detector and Output Filtering feed and internal audio amplifier. The IF baseband signal (GMSK data) is obtained from the internal audio amplifier output. The GMSK data is fed to comparators that send the digitized data to the FPGA.

2.7 Transmit Path

The input to the modulator is a filtered I&Q signal. As discussed earlier, the processor fills the transmit FIFO in the FPGA. A state machine within the FPGA, takes the parallel data, converts it to a serial bit stream at 19.2 KHz and splits the data into sine and cosine values. These signals are then measured from bit to bit to determine whether an unchanged or changed signal state has occurred. There is a waveform table for each state. This data is written to the DAC and the resultant waveform is created. The modulator uses the I&Q to mix with the 90 MHz derived by the divide by two quadrature phase generator within the modulator chip. The resultant signal is differentially output to a differential buffer.

The differential buffer utilizes a tuned tank to suppress the harmonics, and an output impedance transformation filter set its output to 50 ohms. An additional buffer amplifier drives the mixer. The mixer upconverts the modulated 90 MHz. At the output of the mixer is a SAW filter with a bandwidth of 30 MHz. It is used to suppress any harmonics. There is an additional gain stage used to control the input power to the PA. Another SAW filter removes any harmonics amplified by the gain stage. An additional pad provides isolation between the filter and the PA input stage.

The PA receives it power directly from the battery and is controlled by a current sensing feedback amplifier. The output tuning of the PA is designed to limit the maximum available power from the amplifier to +30.5 dBm. Subtracting the loss of the duplexer (2.5 dB), the maximum achievable output of the modem is +28 dBm.