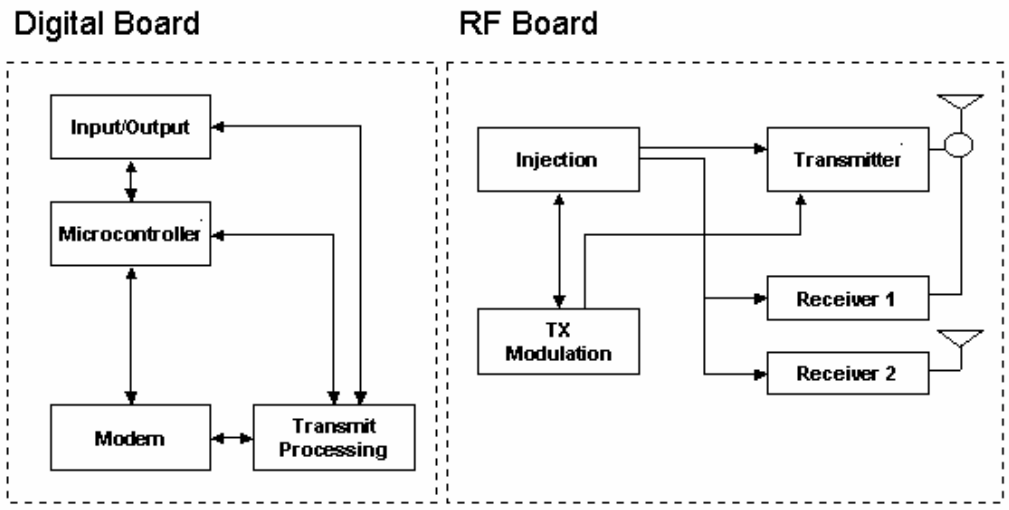
General Block Diagram



General Block Diagram Definitions

For increased data security, the modem supports the Federal Government developed Digital Encryption Standard (DES) data encryption and decryption protocols. This capability requires installation of third party, Internet Protocol (IP) compliant DES encryption and decryption software on the system.

The M32450-25 mobile radio is comprised of two (2) circuit boards, the digital board and the RF board. The digital circuit board contains the following sections:

Input/Output — Circuitry associated with the following data connectors:

- RS232 Serial Port DB9 Data Connector
- RJ45 Ethernet 10 Base T Interface Connector

For further details on the Ethernet Controller, refer to the Crystal LAN™ Ethernet Controller Product Bulletin (CS8900A-EthernetCtrlr.pdf) available on the Product Documentation CD.

Microcontroller — Manages the operation of the radio, the modem, and determines which receiver provides a better signal from a given transmission. Also provides transmit time-out protection in the event a fault causes the radio to halt in the transmit mode.

Modem — Converts serial data into an analog audio waveform for transmission and analog audio from the receiver to serial data. Within a single chip it provides forward error detection and

correction, bit interleaving for more robust data communications, and third generation collision detection and correction capabilities.

Power Supply — The power supply creates the various voltages required by the digital portion of the mobile radio.

The RF circuit board contains the following sections:

Transmit Processing — Circuitry that amplifies the analog audio signal from the modem and uses it to modulate the voltage controlled oscillator (VCO) and 10 MHz reference oscillator in the injection synthesizer section. Modulating the VCO and reference oscillator simultaneously results in a higher quality FM signal.

Injection Synthesizer — Provides programmable, ultra stable signals for the radio. Synthesizer incorporates phase lock loop technology used for both receiving and transmitting.

Injection — In the receive mode, the synthesizer provides a local oscillator signal of 45 MHz above or below the selected receive channel frequency.

Transmitter — Consists of an exciter and power amplifier module. The transmitter covers the various frequency bands in segments. A different power amplifier module is required for each segment. The transmitter circuitry includes a T/R switch switching the antenna between transmitter and receiver 1 (TX/RX1).

Receiver 1/Receiver 2 — Required to support the mobile DRS; two (2) discrete receivers are tuned to the same channel and use two (2) antennas.

The receivers are double-conversion superheterodyne with a first Intermediate Frequency (IF) of 45 MHz and a second IF frequency of 455 KHz. Each receiver consists of bandpass filters, an RF amplifier, a MMIC mixer, crystal filters, and a one-chip IF system. The injection synthesizer provides the first local oscillator signal. Outputs from each receiver include RSSI and analog audio for the baseband routing circuitry and modem.

Power Supply — Consists of circuitry that derives the various operating voltages for the RF portion of the mobile radio.

M32450-25 Mobile Radio Section Descriptions

The M32450-25 Mobile Radio works within a frequency range of 450 to 480 MHz and requires a 1/4-wavelength antenna.

This section provides detailed descriptions of each of the sections within the M32450-25 Mobile Radio. Refer to Appendix A to view the M32450-25 Mobile Radio Circuit Board Diagram.

Microcontroller

The microcontroller (U30) is a major component of the radio as it manages the operation of the radio. It also controls the operation of the modem, and determines which receiver provides a better signal from a given transmission. It provides transmit time-out protection in the event a fault causes the radio to halt in the transmit mode. It utilizes a reduced instruction set computer (RISC) architecture which provides low power operation and a powerful instruction set. Other features include a watchdog timer, serial universal asynchronous receiver/transmitter (UART), two 8-bit timers, and 2 KB of electrically erasable programmable read only memory (EEPROM) storage.

NOTE: The EEPROM Random Access Memory (RAM) stores the setup data entered by the technician even if there is a loss of power.

Support circuitry

The support circuitry consists of the following:

- A Supervisor Control Chip (U25) provides power-on reset.
- The clock controls microcontroller operation and is generated by crystal Y3 and a Pierce oscillator circuit (inside the U30-microcontroller).
- The latch (U28) decodes low order address bits (A0-A7) from the address/data bits (AD0-AD7). It is controlled by Address Latch Enable (ALE) output of U30 and the bits are used by the modem.
- A 512Kx8 Static RAM Chip (U31) provides temporary storage of the radio's configuration data facilitating the technician with access to make changes.
- Control logic is also an important part in the microcontroller section. The RAM chip select (RAMCS*) and modem chip select (MODEMCS*) command lines are created by U26A, U27BCD, and U44ABC. These gates decode four (4) high order address bits (A11-A15). The RAM is addressed by five (5) memory addresses (MA14-MA18) bits decoded by U26D, U27A, and U24. This logic decodes port address bits (PA14-PA18) to produce memory address bits (MA14-MA18) for the RAM chip.

Input/Output

Input/output components convert serial and handshake data from the modem section to RS232 levels, and vice-versa. Chip U22 is an RS232 transmitter and receiver. It converts data in 5-volt logic form to data in +/-12-volt form, as required by the RS232 standard. A charge pump power supply on the chip converts the +5-volt DC logic power on pin 26 to the +12-volt and –12-volt levels required. Capacitors C106-C109 generate these voltages by a charge pump. These values determine the operating voltages.

Modem

The single-chip modem circuit converts parallel data to an analog audio waveform for transmission and analog audio from a receiver to parallel data. In addition to the modem functions, the chip provides forward error detection and correction (FEC), bit interleaving and Viterbi Soft Decision Algorithms for more robust data communications.

The microcontroller section controls the modem operation. Address bus, address/data bus, and control lines operate the modem chip. The modem circuitry is also run by a crystal-controlled clock, which consists of crystal Y1 and an internal Pierce oscillator.

The received audio signal is demodulated into digital data appearing on the AD0-AD07 lines when the MODEMCS* and RD* lines are low. The data goes to the microcontroller section for futher processing, and then to the input/output section for conversion to RS232 or Ethernet signal levels.

During a transmission, outgoing data appearing on the AD0-AD07 lines is converted into a 4-level FSK analog signal by the modem chip. This operation takes place when the MODEMCS* and WR* lines are low. Data from the user's MDC or VIU passes through the input/output section and microcontroller section to the AD0-AD07 bus. After processing, data passes through a root raised cosine filter and is output to TXMOD.

This modem supports 115.2 KBPS (serial port) and 32 KBPS (over-the-air) data transmission rates.

VLogic and Digital Ground

The VLogic and Digital Ground section consists of a pulse-width modulation (PWM) step-down DC-DC converter (U20) that provides an adjustable output. It also reduces noise in sensitive communications applications and minimizes drop out voltage.

An external Schottky diode (D2) is required as an output rectifier to pass inductor current during the second half of each cycle to prevent the slow internal diode of the N-channel MOSFET from turning on. This diode operates in pulse-frequency modulation (PFM) mode and during transition periods while the synchronous rectifier is off.

Receiver 1 Front-End

This section contains components that include several RF Bandpass filters, a low-noise amplifier, and a MMIC mixer.

Incoming signals pass through one (1) pre-selector filter (FLT6) that selectively provides a high degree of out-of-band signal rejection. An MMIC amplifier (U15) amplifies the selected signals and is followed by an image and noise reject filter (FLT5). The output from FLT5 passes through a mixer (U16). U16 is a MMIC mixer which mixes the receive injection (RXINJ1) signal from the synthesizer and the RF signal from the antenna to produce a 45 MHz IF signal. This 45 MHz signal passes through crystal filters (FLT7 and FLT8) to the Receiver 1 IF section to provide the bulk of the Receiver's selectivity.

Receiver 2 Front-End operates identical to Receiver 1 Front-End.

Receiver 1 IF

The major contributor of the IF subsystem (U20) a complete 45 MHz superheterodyne receiver chip incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), voltage regulator and audio and RSSI op amps.

Incoming 45 MHz signals appearing at RX1_45MHz pass through the low-voltage high performance monolithic FM IF system. Within U20, the signals pass through a simple LC filter and are boosted by the RF amplifier. The output of the RF amplifier drives a mixer. A crystal oscillator is controlled by crystal Y3 and provides the injection frequency for the mixer. The mixer output passes through a 455 KHz ceramic filter (FL3). It is then amplified and passed through another ceramic filter (FL4) to a second gain stage. The Diversity Reception Controller uses BRSSI1 to select the receiver with the best quality signal.

The audio is amplified by two (2) op amps (U19CD) and delivered to the power and analog ground circuitry via the RXMOD1 output. High frequency de-emphasis is provided by a filter consisting of a resistor and a capacitor. In order to match the audio signal levels with the other circuitry, a gain control is included. A pot (RV7) is necessary to adjust gain.

Receiver 2 IF operates identical to Receiver 1 IF.

Transmit Modulation

The analog circuitry in this section modulates the Transmitter. The data-bearing audio signal from the modem appears at TXMOD. The audio is amplified by op amp (U1D). The output of U1D drives two (2) amplifiers (U1B and U1C).

The transmitter uses dual-point modulation meaning the modulation is applied both to the VCO as well as the reference oscillator (VCTXO).

The upper amplifier (U1B) has adjustable gain. The output drives op amp (U1A), which inverts the phase of the signal. Upon the start of a transmission, the modulating signal passes through to the VCTXO reference oscillator in the synthesizer. Some makes of VCTXO oscillators do not require the modulation signal to be inverted and a jumper block (JMP1) is provided to accommodate the oscillators.
The lower op amp (U1C) amplifies the signal from the low pass filter and applies it to the VCO via the VCOMOD output. Pot RV2 and RV4 are used to adjust maximum deviation.

Injection Synthesizer

Two dual fractional synthesizer chips (U6 and U8) are the major contributor of the receiver and transmitter injection oscillators. This device contains the key components of a phase locked loop (PLL), including a prescaler, programmable divider, and phase detector. The selected frequencies are loaded into U6 and U8 as a clocked serial bit stream via the PLL_DATA, PLL_CLOCK, and PLL_ENABLE signals.

Frequency stability is determined by a temperature-compensated crystal oscillator module (VCTCXO) (Y1) at a frequency stability of 1 PPM from –30C to +60C. This device has an input (REFMOD) that accepts transmit modulation and voltage from a RX FREQ ADJUST pot. The pot allows the receiver to be fine-tuned to the exact operating frequency.

Two (2) voltage control oscillators (VCO) are formed by integrated low-noise oscillators with buffered outputs (VCO1 and U9) and associated circuitry. The VCO's generate receiver and transmit injection signals. The output of U9 is split by a two-way power divider (U10) leading to outputs RXINJ1 and RXINJ2. A second output of U9 is returned to the synthesizer FIN input via RXFB. This completes the loop signal path.

Transmitter/TR Switch

The transmitter section consists of an amplifier (U3) and an op amp (U4). To transmit, 5-volt power is applied to the KEYPWR line. PA12V line is also powered up. This causes power amplifier (U2) to boost the RF power to the desired level. Up to 40 watts are available from the transmitter. Harmonic suppression is provided by C13, L2, and L3.

Power and Analog Ground

These sections consist of the power supplies and transmit control circuitry. Power from the vehicle's battery appears at VBATT. Diode D1 protects the voltage regulators by clamping any transient spikes on the supply line. Such spikes typically occur while the engine is started. The supply line powers a series of voltage regulators and the transmitter control circuitry, as follows:

- Voltage regulator VR1 provides 8-volt power for most other sections in the radio.
- Voltage regulator VR2 powers the transmit driver and T/R switch diodes as controlled by the microcontroller.
- Voltage regulator VR3 provides a low noise 3.3-volt source for the radio electronics.