IP8B Base Station Section Descriptions

System Controller *(refer to schematic on page 26)*

This section displays the Central Processing Unit (CPU)(U1), clock, and power-on reset circuitry. It provides more processing power than required for future capabilities to be incorporated without changing processors. Such capabilities include data encryption/decryption (DES) and remote fault monitoring. U1 features a 16-bit address bus and 128K of internal flash random access memory (RAM).

NOTE: To enter the programming mode it is necessary to reset the switch (S1) and power up again.

CPU operations are controlled by Y3 an 18.432 MHz clock module. Capacitor (C1) and an internal Schmidt trigger circuit inside of U1 generates the power on reset signal. The RESET* output from U1 drives a latch and decoder found elsewhere on the board.

This section displays the RAM, decoder, EEPROM, and programming power supply circuitry. U2 is a 512K x 8 bit static RAM chip, which provides temporary storage of base station configuration data while the power is on. This is necessary in order to program the base station. U2 is controlled directly by the address, data, and control busses from the CPU.

Chip U5 decodes the A11-A14 address bus to provide chip selects for the modem and EEPROM memory. Chip U6 is an 8-bit latch. It latches inputs from the D0-D7 bus and lights the front panel status indicators (*TX, CD, RX1, RX2, and RX3*).

Chip U3 is a serial EEPROM, which provides 2K bits of pre-programmed data storage for the CPU. Data is clocked out of U3 by EECLK, and back into the CPU via EEDATA.

A programming power supply is required for the flash RAM inside of the CPU, and this function is performed by U4. This chip is a low dropout voltage regulator with a shutdown control. Resistors R22 and R21 set the output voltage. When the base station configuration data is to be stored in flash RAM, the CPU makes VPP_ENABLE high. This turns on the regulator, producing a 12-volt output via VPP for the flash RAM.

This section displays a dedicated processor and voltage regulator. Chip U7 is a processor, which permits manual keyboard operation of the base station. Regulator VR2 provides 5 volts DC power for all logic circuitry on the System Controller Board.

Input/Output *(refer to schematic on page 30)*

This section displays the CPU input/output circuitry. Chip U8 is an RS232 transceiver, which interfaces the CPU to the modem via J1. From there, the RS232 data goes directly to a rear panel DB9 connector. U8 converts 5-volt logic-level data to +/-12 volt data in RS232C form, and vice-versa. A charge pump power supply on the chip converts the +5 volt DC power to the +/-12 volt levels required. The charge pump uses capacitors (C28 to C31) to generate voltages.

NOTE: The RS232 serial port data transmission rate of the base station is 115.2 KBPS.

Modem Switching

This section displays the connector wiring and modem switching circuitry. Connector J7 is routed to the front-panel TX, CD, and RX1-RX3 LED indicators. The base station will also accept

modulation from an external source (modem or amplified microphone audio). Transmission gate U10A switches this signal source.

Modem *(refer to schematic on page 29)*

This base station uses separate modems for receive and transmit functions so that full-duplex operation may be obtained. The A0-A1 address bus in addition to the individual read (RD*), write (WR*), and chip select (MODEMTXCS*) lines control all three (3) modems. Modem operations are timed by Y2, a 4.9152 MHz clock module.

Modem chip U14 is dedicated to the transmit operation. Data from the D0-D7 bus is read by the chip, and then converted to a 4-level FSK analog signal, which appears on the TXOUT pin. Op amp U21B buffers the signal, which becomes the MODEM_TXMOD output. From this point, the signal is routed to the modulation circuitry on the Exciter Board.

Chip U14 has the ability to demodulate receiver audio, although this capability is not used in most systems. Incoming data-bearing audio from the Diversity Reception circuitry (and selected receiver) appears at DISC_AUDIO. The signal passes through resistor R54 and into the modem chip. Resistor R52 and capacitor C41 serve as feedback elements, limiting both the gain and bandwidth of an amplifier within U14. The modem chip demodulates the audio into 8-bits of data, which exit U14 on the D0-D7 bus.

Chip U14 also provides a bias voltage for the analog circuitry on the Exciter Board. This voltage is about 2.5 volts DC, and it appears on the VBIAS line. The purpose of VBIAS is to bias the Exciter Board analog circuitry for proper operation. Please note that if this voltage is low or missing, the Exciter Board circuitry may not work.

Modem chip U15 is dedicated to the receive operation. Incoming data-bearing audio from the Diversity Reception circuitry (and selected receiver) appears at DISC_ AUDIO. The signal passes through resistor R56 and into the modem chip. Resistor R55 and capacitor C46 serve as feedback elements, limiting both the gain and bandwidth of an amplifier within U15. The modem chip breaks down the audio into 8 bits of data, which exit U15 on the D0-D7 bus.

Modem chip U16 is also dedicated to the receive operation, although it may not be used in this application. The operation of U16 is exactly the same as U15.

Receive Signal Strength Indication Comparator *(refer to schematic on pages 32 & 33)*

This section displays the RSSI comparator circuitry. A series of comparators (U20BCD) simultaneous compare RSSI1 to RSSI2, RSSI2 to RSSI3, and RSSI1 to RSSI3. Within this process eight (8) possible results are then forwarded by the comparators to a series of NAND gates (U18ABC), which reduce the number of results to three (3) and translates the results for an analog multiplexer (U19A). To determine which of the three (3) results is the strongest, the following needs to occur:

- For Receiver 1 to be selected as the strongest signal, both input pins on the NAND gate (U18D) must go high (driving pin 7 of U19A). If Receiver 1 has the strongest signal, a light emitting diode (LED)(D1) lights indicating Receiver 1 was selected.
- For Receiver 2 to be selected as the strongest signal, the inverter (U17B) must go high (driving pin 6 of U19A). If Receiver 2 has the strongest signal, D2 lights indicating Receiver 2 was selected.
- For Receiver 3 to be selected the strongest signal, the inverter (U17C) must go high (driving pin 5 of U19A). If Receiver 3 has the strongest signal, D3 lights indicating Receiver 3 was selected.

SEL_RSSI is the output selected with the strongest signal. When RSSI voltage exceeds a threshold, another LED (D4) lights. As the other three (3) LEDs, this circuit is intended as a diagnostic tool. It provides a go/no go indication that an RF signal has been received. A pot (R74) sets the turn-on voltage.

Baseband *(refer to schematic on page 34)*

This circuitry amplifies the audio from each receiver, routes it through a RF multiplexer, and selects the audio from the receiver with the highest RSSI value. The comparator circuit on the previous sheet controls it.

There are three (3) channels of audio, with separate gain and DC offset adjustments to compensate for performance differences in the receivers. For example, incoming audio from receiver 1 appears at AUDIO 1. An op amp (U12D) is then amplifies the audio. A pot (R72) adjusts the gain, while another pot (R57) adjusts the DC offset on the output. The amplifier output passes through a RF multiplexer (U19B), then drives a low pass filter (U9) through another op amp (U12A) and through the AUDIO_OUT line, which goes to a switch (S3) and to pin 4 of a connector (J3).

The remaining audio circuits work in the same manner.

The output from U19B also appears on DISC_AUDIO, which goes to the CPU (U1) and from there the audio is demodulated by the modems.

Receiver Board *(refer to schematic on page 44)*

Please be aware that the base station uses three (3) identical receiver boards. As a result, the circuitry will be described only once.

Front end. Incoming signals pass through a bandpass filter (FLT1). The desired signals are amplified by U4 and additional selectivity is provided by a SAW filter (FLT2). The signal passes through an IC mixer (U5) and the output passes through two (2) crystal filters (FLT3 and FLT4).

IF Amplifier *(refer to schematic on page 45)*

The incoming 45 MHz signal passes through C15, C17, and R12 which provides impedance matching to the IF amplifier input. U2 is a super heterodyne IF subsystem. Inside the chip, the signal is applied to a mixer. The mixer also accepts a 44.545 MHz local oscillator input. The local oscillator consists of an internal amplifier, plus crystal (Y1) and associated components. The mixer output passes through Y4, a 455 KHz ceramic IF filter. It is amplified, passed through another 455 KHz ceramic filter (Y3), and on to a second IF stage. The IF output drives a quadrature detector. The phase shift elements for the detector are C8 and Y5. The recovered audio appears at pin 9, while RSSI appears at pin 7.

Within the RSSI circuitry, chip U2 uses a detector, which converts the AGC voltage generated inside the chip into a DC level corresponding logarithmically to signal strength. RSSI is used by Diversity Reception on the System Controller to select the receiver with the highest quality signal.

A filter consisting of a resistor (R8) and a capacitor (C18) provides high frequency de-emphasis for the audio. The audio is buffered by op amp U1A. From there the AUDIO output line goes to a connector, for hookup to Diversity Reception on the System Controller Board.

Resistor (R9) and capacitor (C10) provides RF filtering for the DC RSSI voltage. The RSSI is buffered by op amp U1B. From there the RSSI output line goes to a connector, for hookup to Diversity Reception on the System Controller Board.

Several sets of 455 KHz IF filters (Y4 and Y3) are available to suit receiver selectivity requirements. Should replacement of these filters be required, exact replacement parts must be used.

Receiver Injection *(refer to schematic on page 20 & 21)*

This displays a serial data input/output interface, synthesizer, and VCO. The I/O interface circuitry accepts clock, serial data, and enable signals from the System Controller Board via terminal block TB1. A lock detect (LD) status output is returned to the System Controller Board from the synthesizer. U6 is a hex Schmidt Trigger inverter, which squares up incoming signals for reliable operation of the synthesizer chip. This is necessary because of a cable run between the two (2) boards.

The main section of this board is synthesizer chip (U5). The device contains the key components of a phase locked loop (PLL), including a 1.1 GHz prescaler, programmable divider, and phase detector. In operation, the desired frequency is loaded into U5 as a clocked serial bit stream via the CLK and DATA/I inputs. The lock detection circuitry consists of inverters U6E/U6F, diode CR1, and resistor R3. When the synthesizer is in lock, the LD pin on U5 is high, making the LD output on terminal block TB1 high.

The UHF injection signal is generated by module VCO1. This device is a wide-range voltage controlled oscillator (VCO). A voltage on the C input determines the VCO frequency. The voltage is generated by the phase detector output (PD/O) of U5, which drives a loop filter consisting of R2, C23, C7, R5, C15, and C16. The filter integrates the pulses, which normally appear on PD/O into a smooth DC control signal for the VCO. The output of VCO1 is attenuated by module AT1, resulting in improved VCO stability.

Reference module (Y1) provides a high-stability 10 MHz reference frequency. Y1 is a voltage controlled, temperature controlled crystal oscillator (VCTCXO). This device also has a VC input which accepts a control voltage from pot R7. The pot permits a slight shift in the reference frequency which enables the three (3) receivers to be tuned precisely to the assigned receive frequency. A diode (CR2) provides additional voltage regulation, improving the frequency stability of reference Y1.

The RF output circuitry consists of RF amplifier (U4), and two-way power splitters (U3, U1, and U2). U4 increases the signal level to correct for losses in the splitters. The splitter U3 provides two (2) RF outputs. One output drives splitter U1, which provides local oscillator injection for receivers 2 and 3. The other output drives splitter (U2), which drives receiver 1 and the PLL_FEEDBACK input on chip U5.

Exciter Board *(refer to schematic on page 49)*

This section displays the input/output interface, transmitter keying, and power supply circuitry. The input/output interface is built around terminal block (TB1) and Schmidt Trigger inverters (U4). Incoming clock, serial data, and chip select signals on block TB1 are squared up by U4. Then they are sent to the appropriate inputs on the low pass Bessel filter (U2). The EXCDATA source comes from the receive synthesizer on the Injection Synthesizer Board. A Schmidt Trigger chip is used here because of a cable ran to the System Controller Board. The synthesizer returns a lock detect output to the Injection Synthesizer Board via U4D and EXCLD.

A regulator (VR3) powers the T/R switch circuitry. When the System Controller Board makes TXKEY* low, turning on transistor Q4 and FET Q1. This applies 5-volt power to the TXENABLE output, turning on the T/R switch on the Power Amplifier Board. At the same time, transistor Q2 conducts, grounding the KEY* input of the Power Amplifier Board. Finally, inverter U4E goes high and turns on RF switch U5, connecting the VCO output to the Power Amplifier Board for transmission.

The power supply consists of two (2) voltage regulators. A regulator (VR1) provides 9-volt power for the VCO. Another regulator (VR2) provides low noise 5-volt power for the logic circuitry, synthesizer chip, and analog circuitry.

Analog Modulation *(refer to schematic on page 52)*

This section displays the analog modulation circuitry. Incoming modem audio from the System Controller Board appears at TXMOD, and is buffered by op amp U3A. If an external modulation source (modem or amplified microphone) is connected to the base station's DB9 connector, audio appears at EXTMOD. From there the audio passes through low pass Bessel filter U2. The audio is inverted and amplified by an op amp (U3B). It then passes on to the VCO module via VCOMOD. Pot R11 adjusts the level to suit the VCO.

The 10 MHz reference is also modulated in order to counteract the corrective effects of the synthesizer loop circuitry. For example, if only the VCO were modulated, the synthesizer would try to compensate for the frequency "error," caused by the modulation. This effectively reduces the amount of modulation available. Modulating the reference *and* the VCO simultaneously deceives the loop into not compensating for the modulation, because when the reference frequency goes high, the VCO frequency goes high, and vice-versa.

An op amp (U1A) amplifies the AUDIO output from another op amp (U3D) and applies it to jumper block JP1. Pot R4 adjusts the gain of U1A. Op amp (U1B) inverts the phase of the audio and applies it to the other side of jumper block JP1. The purpose of the jumper block is to select the proper phase of the audio. If the wrong phase is used, on modulation peaks the reference will swing in the same direction as the VCO, canceling out most of the modulation. The output from the jumper block goes to the 10 MHz reference via REFMOD.

The VBIAS input is a 2.5-volt DC source, which biases the op amps to the correct operating point. It is generated by modem chip (U14) on the System Controller Board.

Phase Locked Loop *(refer to schematic on page 53)*

This section displays phase locked loop (PLL) circuitry. The 10-MHz reference (Y1), runs synthesizer (U6), which in turn controls VCO VCO1. The main section of this board is the synthesizer chip (U6). The device contains the key components of a PLL, including a 1.1 GHz prescaler, programmable divider, and phase detector.

In operation, the desired frequency is loaded into U6 as a clocked serial bit stream via the CLK and DATA inputs. The lock detection circuitry consists of inverters U4D, diode CR1, and resistor R28. When the synthesizer is in lock, the LD pin on U6 is high, making the EXCLD output on terminal block (TB1) high. The EXCLD output on TB1 routes the lock detect output from the Exciter Board. This configuration tells the CPU on the System Controller Board that it is acceptable to process received data, or to key the transmitter when LD is high. Otherwise, if a fault in either synthesizer prevents a lock, receive and transmit operation will be inhibited.

The switch (JP1) is used to select the supply voltage to chip U6. The UHF injection signal is generated by module VCO1. This device is a wide-range voltage controlled oscillator (VCO). A voltage on the VT input determines the VCO frequency. The voltage is generated by the phase detector output (PD/O) of U2, which drives a loop filter consisting of R31, C50, C28, and C25. The filter integrates the pulses, which normally appear on PDOUT into a smooth DC control signal for the VCO. The output of VCO1 is attenuated by module AT1, resulting in improved VCO stability.

RF amplifier U8 amplifies the signal and applies it to a two-way power splitter (U7). One output of U7 is connected to a switch (U5). U5 is enabled by signal TX when the transmitter is enabled. The other output of the splitter provides feedback to U6.

Power Amplifier *(refer to schematic on page 40)*

The transmit injection signal from the RF injection section is applied to the high-powered linear amplifier (U1) one (1) watt amplifier. The signal is then routed to the final power amplifier boosting the output signal to 20 watts.