EXHIBIT A:

DT800 Product Specification Manual

DT800 Product Specification
ECS 516-82014 Revision X1

1. INTRODUCTION

1.1 Document Scope

This document describes the ElectroCom Model DT800 mobile radio comprehensively.

Section 1: non-technical overview of the product and its features.

Section 2: more detailed; describes various interfaces (i.e. connectors, power sources, interconnections, etc.).

Section 3: covers various specifications the product is designed to meet.

Section 4: contains operating and maintenance instructions.

Section 5: theory of operation, this section contains detailed functional descriptions of circuit operation.

The remaining sections need no explanation.

Throughout this document, SMALL CAPITAL LETTERS are used to indicate signal names used on schematics and *italics* are used when describing circuitry, methods, or devices which affect regulatory compliance.

1.2 Reference Documents

Schematic Diagram, DT800 ECS PN 502-82001 Rev B (attached)

MX•COM MX919A 4-Level FSK Modem Data Pump Product Specification

ATMEL AT89S8252 8-Bit Microcontroller Product Specification

BRXI Protocol Specification ECS PN 517-00001

1.3 Product Features

DT800 Features:

- Patented, dual receiver, diversity reception system

  U.S. Patent No. 5,640,695

- High stability - 1.0 ppm
- Internal 4-level FSK modem, 4800, 9600, 19200 bps with DES
- Fast transmit attack time - less than 1 msec
- 2 advanced-architecture, extremely sensitive, high-overload, FM receivers
- 25 Watt Tx output power
- Digital PLL frequency synthesizer
- Broadband operation by design
- Compact size, rugged construction

1.4 General Product Description

The DT800 is a no-compromise, high-performance, synthesized, UHF (800 MHz) mobile radio with dual-receiver, post-detection diversity reception. The diversity reception system significantly reduces the damaging effects of multipath fading.

Frequency stability over temperature is ensured by a TCVCXO (Temperature Compensated Voltage Controlled Crystal Oscillator) with 1.0 ppm (part per million) frequency stability over the temperature range of -30 to +60 C.

The DT800 includes a 4-level FSK (Frequency Shift Key) modem which supports data rates of 4800, 9600, and 19200 bps. The radio is intended to operate at data rates of up to 19200 bps in a 25 kHz channel, and up to 9600 bps in a 12.5 kHz channel.

The transmitter design enables stable, on-frequency, RF carrier attack times of less than 1 milliseconds and an output power level of 25 Watts.

The DT800 receivers feature an advanced architecture, cascaded LNA (Low-Noise Amplifier) design which results in extreme sensitivity and high overload capability.

The radio operates with a 45 MHz transmit-to-receive frequency separation and is capable of operating on all authorized channels within the 806 to 869 MHz band.

The mechanical package of the DT800 is extremely robust, constructed primarily of machined 1/4" aluminum plate. The excellent thermal conductivity characteristics of heavy gauge aluminum enable the chassis to act as a heat spreader, distributing heat uniformly throughout the entire structure. A mil-spec chemical finish protects the chassis from oxidation.

All inputs and outputs are via EMI/RFI filtered connectors resulting in extremely low undesired emissions (both radiated and conducted) and reduced susceptibility to external sources of EMI/RFI.

The DT800 electrical design reflects a total commitment to Surface Mount Technology (SMT) resulting in reduced size, lower cost, and increased performance.

1.5 Functional Block Diagram

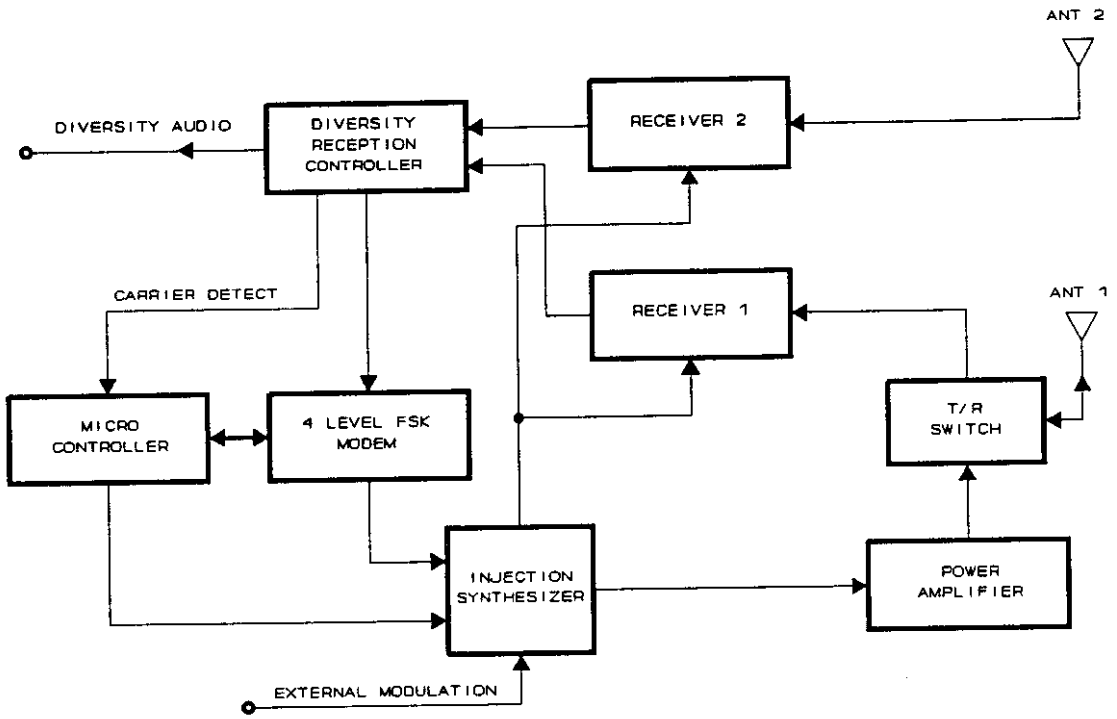

Figure 1. DT800 Functional Block Diagram

The DT800 is divided into eight functional blocks as depicted in *Figure 1*.

Microcontroller: Programs the injection frequency synthesizer, controls the internal 4-level FSK (Frequency Shift Key) radio modem, the RS232 interface, transmit timer, and peripheral devices.

4-Level FSK Modem: Interfaces with the microcontroller and the radio modulation/demodulation circuits to deliver reliable two-way transfer of high-speed data over a wireless link. The modem supports data rates of 4800, 9600, and 19200 bps, under software control.

Injection Synthesizer: Generates the receiver injection signals in the receive mode. Generates the exciter injection signal and accomplishes frequency modulation in the transmit mode.

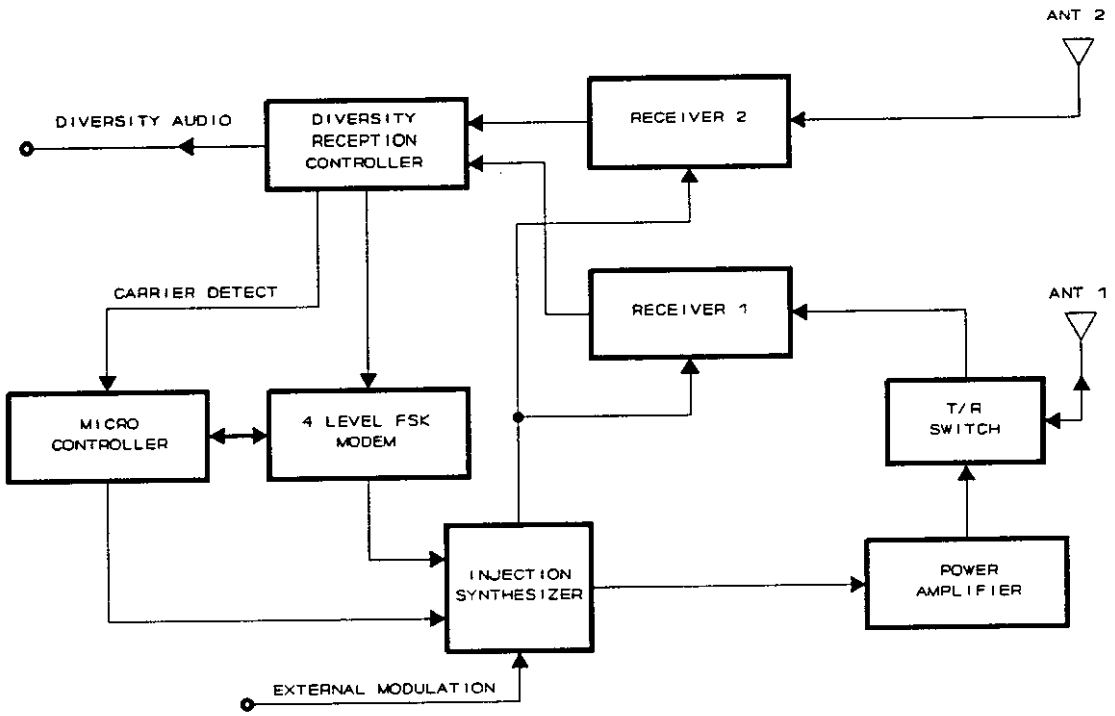

Figure 2. DT800 Functional Block Diagram ***(Repeated for reader convenience)***

Receiver: Provides reception and demodulation of Frequency Modulated (FM) UHF (851 to 869 MHz) RF signals. The receivers also provide RF carrier amplitude information used by the diversity reception system.

DRC (Diversity Reception Controller): A patented feature which provides diversity reception capability by continuously selecting the receiver with the higher SNR (Signal to Noise Ratio).

Power Amplifier: Amplifies the low-level transmit carrier signal from the RF injection section to the final output power level (25 Watts).

T/R Switch: Allows one antenna to be used for both transmit and receive operations.

2. INTERFACE DESCRIPTION

2.1 External

2.1.1 RF Ports

The DT800 has two external RF ports. Both are type "N" coaxial connectors mounted directly to the chassis of the radio. J2 is a bi-directional port which serves as the transmit port during transmit operation, and as the receive port for receiver 1 in the receive mode. J3 is a receive only port for receiver 2 and is dedicated to diversity reception.

2.1.2 DC Input Power

DC input power (for the power amplifier) and ground (for the entire radio) is supplied via J4, a 2-conductor quick-disconnect connector. *The positive conductor (red) feeds DC input power to the power amplifier through EMI/RFI (ElectroMagnetic Interference / Radio Frequency Interference) filtered connector FLT1.* The ground conductor (black) is soldered directly to the body of FLT1.

2.1.3 Interface Pinouts

External interface to the radio is provided by connector J1, a EMI/RFI filtered 25 pin "D"type connector. All signals are CMOS levels unless otherwise specified. An asterix at the end of a signal name indicates the signal is active low. The pinouts for J1 connector are defined below.

PIN #	SIGNAL
1	GND
2	SW12VIN
3	TXKEY*
4	RXDATA
5	CTRLHEADENABLE
6	EXTMOD
7	CD*
8	RSSI
9	RCS0*
10	RCS1*
11	RCS2*
12	RCS3*
13	GND
14	GND
15	RCS4*
16	TXD
17	RXD
18	RESETIN*
19	SPIDATAOUT
20	SPICLOCK
21	SPIDATAIN
22	CTS
23	RTS
24	RX1/RX2*
25	GND

2.1.4 Interface Functional Description

Signal Name	Input Output Power	Description
GND	P	Signal ground
SW12VIN	P	Switched 12.0 volt DC power source
TXKEY*	I	A logic low on this pin will cause the DT800 to key, used by a control head or an external modem device to key the radio
RXDATA	O	Recovered modulation, diversity reception discriminator audio, low-pass filtered by a 4th-order 4800 Hz Bessel filter, approximately 600 mV peak-to-peak for a 1.0 kHz test tone at +/- 4.0 kHz deviation
CHENABLE	O	Control head enable, used to program the DT control head.
EXTMOD	I	External transmit modulation from the DT control head or an external modem device
CD*	O	Carrier Detect signal, a logic level low on this pin indicates channel activity
RCS0 - RCS4	I	Parallel data interface Radio Channel Select lines, 5 bit - 32 channel. Used by an external device to select radio channels
TXD	I	RS232 transmit data, this pin is used by an external device to transmit application data to the internal modem, this pin is not used when the DT800 is using an external modem
RXD	O	RS232 receive data, this pin is used by the internal modem to transmit application data to the external device, this pin is not used when the DT800 is using an external modem
RESETIN*	I	This pin is used to program the DT800 microcontroller
SPIDATAOUT	O	Serial communication data out line, used to program the DT800 control head
SPICLOCK	IO	Serial communication clock line, bi-directional
SPIDATAIN	I	Serial communication data in line,
CTS	O	RS232 Clear To Send signal, used for hardware flow control
RTS	I	RS232 Request To Send signal, used for hardware flow control
RX1/RX2*	I	A logic high on this pin will manually select receiver #1 to supply recovered modulation; a logic low will select receiver #2 to supply recovered modulation, used for receiver maintenance and alignment purposes

3. SPECIFICATIONS

3.1 DT800 General Specifications

PARAMETER	SPECIFICATION
Frequency range	806 to 869 MHz
Channel spacing	12.5 / 25.0 kHz
Mode of operation	Half-duplex, diversity reception
Operating temperature range	-30 to +60 C (-22 to +140 F)
Power supply voltage	13.8 VDC +/- 20%
Power supply current consumption	0.75 A receive 6.0 A transmit
Diversity reception system	Dual-receiver, diversity reception system
Antenna connections	Two type "N" connectors (Tx/Rx1, Rx2)
Interface connection	*EMI shielded 25 pin "D" type connector*
Frequency selection: External frequency control	Parallel data interface, five bit 32 channel or serial communication interface

3.2 Transmitter Specifications

PARAMETER	SPECIFICATION
Frequency range	806 to 821 MHz
Channel spacing	12.5/25.0 kHz
Frequency source	Dielectric resonator based VCO
Frequency stability	+/- 1.0 ppm (.00001%) -30C to +60C (-22F to +140F)
Spurious and harmonic emissions	*-13 dBm (maximum level)*
Transmit power	25 watts minimum
VSWR at transmit antenna port	2.0 or less
Load mismatch tolerance	8.8 : 1 (no degradation)
Transmit attack time	Less than 1 ms
Transmit duty cycle	Intermittent
Modulation	4-level FSK using internal modem, or any CPM compliant narrow-band FM modulation using an external modem device
Transmit modulation group delay	Constant (+/- 2.0 usec) from 3 Hz to 4.8 kHz, fourth-order Bessel response
Modulation input	1.0 volt peak-to-peak for + / - 4.0 kHz deviation (1.0 kHz test tone).

3.3 Receiver Specifications

PARAMETER	SPECIFICATION
Frequency Range	851 to 869 MHz
Channel Spacing	12.5 / 25.0 kHz
Injection Frequency	45 MHz below the base station frequency (low-side injection)
Sensitivity	12.0 dB SINAD at -119 dBm maximum level 12.0 dB SINAD at -120 dBm typical 12.0 dB SINAD at -121 dBm typical with diversity
Selectivity	70 dB (minimum at +/- 25 kHz)
Spurious response	85 dB minimum
Intermodulation distortion	75 dB minimum
IF bandwidth	+/- 7.5 kHz standard, +/- 4.5 kHz & +/- 10 kHz optional
Modulation acceptance	+/- 7.5 kHz minimum with standard bandwidth
Recovered modulation	Approximately 600 mV peak-to-peak for 1.0 kHz test tone at +/- 4.0 kHz deviation
Distortion	Less than 3% at 1.0 kHz, less than 1.5% at 1.0 kHz typical

3.4 Mechanical Specifications

PARAMETER	SPECIFICATION
Width (excluding mounting bracket)	4.40"
Depth (excluding mounting bracket)	8.60"
Height (excluding mounting bracket)	2.75"
Width (including mounting bracket)	8.60"
Depth (including mounting bracket)	8.60"
Height (including mounting bracket)	3.50"
Weight	4.0 lbs

3.5 Environmental Specifications

PARAMETER	SPECIFICATION
High Humidity - Transmitter	EIA/TIA-152-C
High Humidity - Receiver	EIA/TIA-204-D
Shock Stability - Transmitter	EIA/TIA-152-C
Shock Stability - Receiver	EIA/TIA-204-D
Vibration Stability - Transmitter	EIA/TIA-152-C
Vibration Stability - Receiver	EIA/TIA-204-D
Temperature Range - Transmitter	EIA/TIA-152-C
Temperature Range - Receiver	EIA/TIA-204-D

3.6 Regulatory Agency Specifications

3.6.1 FCC

SPECIFICATION	RULE SECTION
Transmitter conducted spurious emissions	*CFR 47 Part 2 Section 991*
Transmitter radiated spurious emissions	*CFR 47 Part 2 Section 993*
Transmitter frequency stability	*CFR 47 Part 2 Section 995*
Transmitter RF output power	*CFR 47 Part 2 Section 985*
Transmitter occupied bandwidth	*CFR 47 Part 2 Section 989*

3.7 Reliability

The DT800 is constructed of top quality components with the highest possible level of integration resulting in an inherently reliable product.

The DT800 shall operate reliably.

4. OPERATION AND MAINTENANCE

4.1 Modes of Operation

The DT800 is a half-duplex two-way mobile radio with dual receiver diversity reception. The radio can operate with carrier frequencies between 806 and 869 MHz. The DT800 has two RF ports, one transmit/receive port, and one receive only port (dedicated to diversity reception).

The radio operates with a 45 MHz transmit-to-receive frequency separation and is capable of operating on all authorized channels within the 806 to 869 MHz band.

The DT800 is capable of voice operation with an external control head. In this configuration, the radio is also capable of talk-around operation (transmitting on the repeater down-link frequency for short range communications). The radio may also be used with an external radio modem provided the modulation scheme is a form of CPM (Continuous Phase Modulation).

The DT800 includes a 4-level FSK modem which supports data rates of 4800, 9600, and 19200 bps. The ability to operate at any particular data rate is subject to regulatory compliance and is primarily a function of channel bandwidth. The radio is intended to operate at data rates of up to 19200 bps in a 25 kHz channel, and up to 9600 bps in a 12.5 kHz channel.

The DT800 receivers come standard with a 15 kHz IF bandwidth (standard for 25 kHz channel spacing). Other IF bandwidths (20 kHz, 12.5 kHz, etc.) are available optionally.

4.2 Programming

Radio channel transmit/receive frequencies, internal / external modem operation, voice operation parameters, and transmit timer functions are programmed into the radio prior to operation. Programming can be accomplished at the factory, or in the field using a DT series radio programming kit ECS PN 502-82029. The kit consists of software (which will run on any IBM PC or compatible), a radio programming cable (which connects from the PC's printer port to the radio), and a radio programming instruction manual. The radio may be re-programmed up to 1,000 times.

4.3 Maintenance

WARNING

FCC regulations require that the frequency and deviation of a transmitter must be checked before it is place into service and re-checked at one year intervals thereafter.

FCC regulations also state that the RF output power of a radio transmitter shall be no more than that required for satisfactory operation considering the area to be covered and local conditions.

FCC ID number for the DT800 Transmitter: MI7-ECSDT800TX

In addition to the required annual frequency and deviation checks, it is recommended the following items be checked (and adjusted, if necessary) at yearly intervals:

- Transmit output power
- Receiver sensitivity
- Receiver distortion
- DRC (Diversity Reception Controller) operation

5. THEORY OF OPERATION

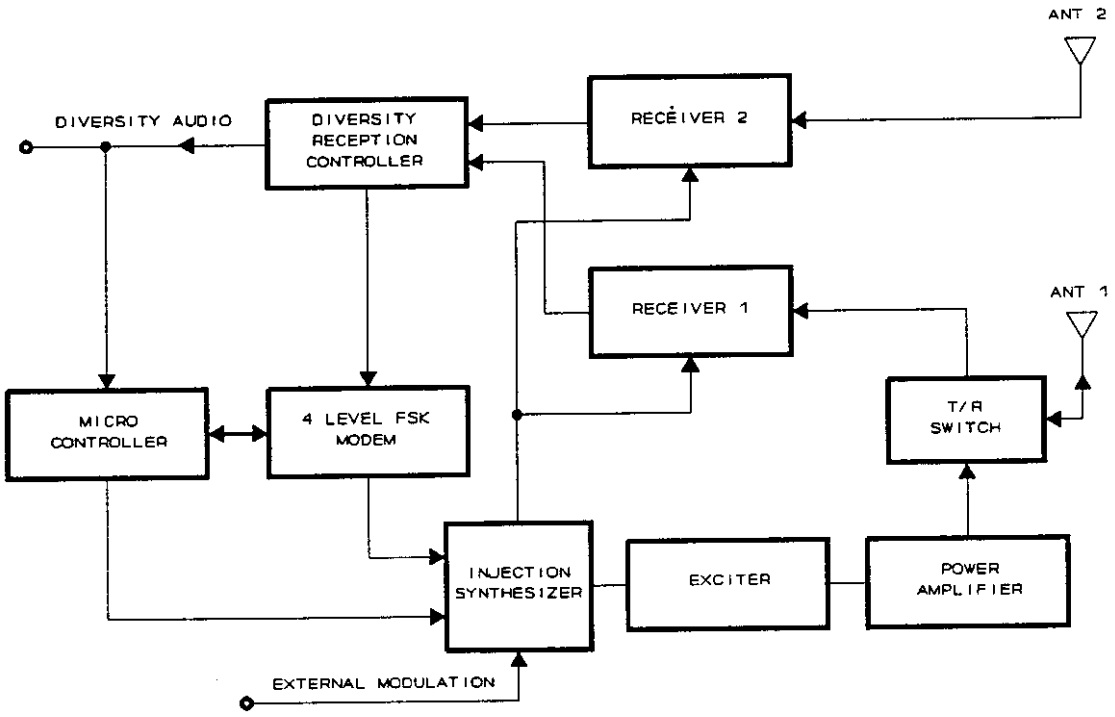

Figure 3. DT800 Functional Block Diagram *(Repeated for reader convenience)*

The DT800 is divided into eight functional blocks as depicted in *Figure 3*.

Microcontroller: Programs the injection frequency synthesizer, controls the internal 4-level FSK radio modem, the RS232 interface, Parallel RCS (Radio Channel Select) interface, the transmit timer, and peripheral devices (control head display, CTCSS (Continuous Tone Coded Squelch System) encoder/decoder, etc.)

4-Level FSK Modem: Interfaces with the microcontroller and the radio modulation/demodulation circuits to deliver reliable two-way transfer of high-speed data over a wireless link.

Injection Synthesizer: Generates the receiver injection signals in the receive mode and generates the exciter injection signal and accomplishes modulation in the transmit mode

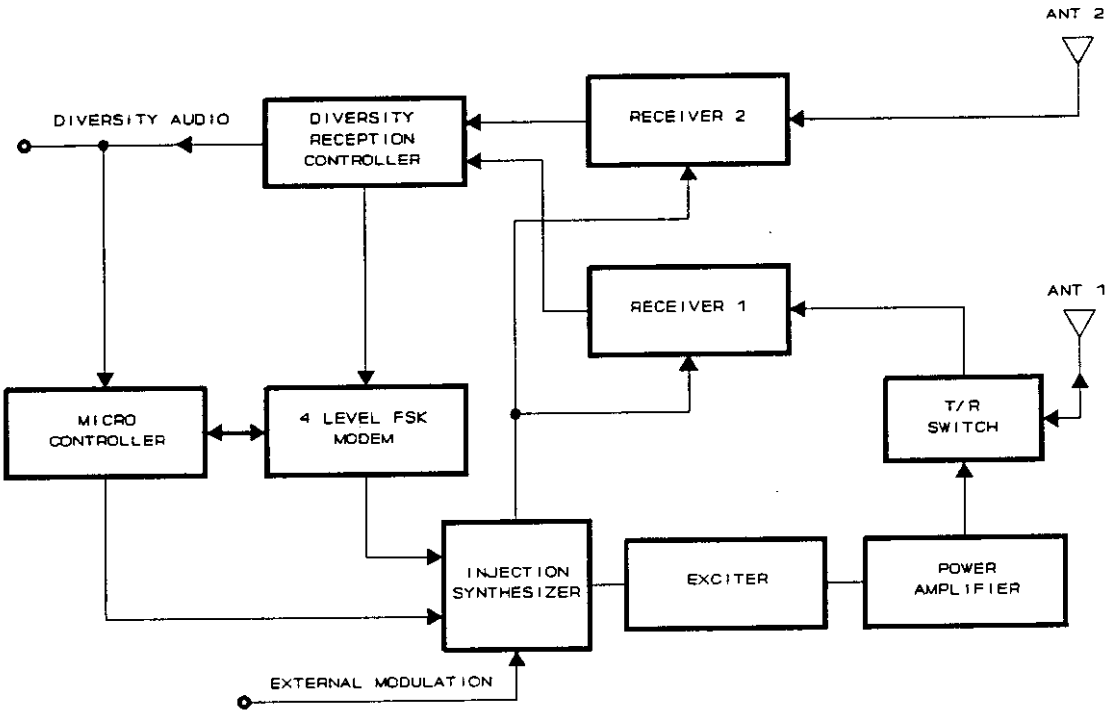

Figure 4. DT800 Functional Block Diagram ***(Repeated for reader convenience)***

Receiver: Provides reception and demodulation of FM (Frequency Modulated) UHF RF signals. The receivers also provide RF carrier amplitude information used by the DRC.

DRC (Diversity Reception Controller): Provides diversity reception operation by continuously selecting the receiver with the highest SNR (Signal to Noise Ratio) at any particular point in time.

Power Amplifier: Amplifies the low-level transmit carrier signal from the injection synthesizer to the final output power level (25 Watts).

T/R Switch: Allows one antenna port to be used for both transmit and receive operations.

5.1 Microcontroller Section

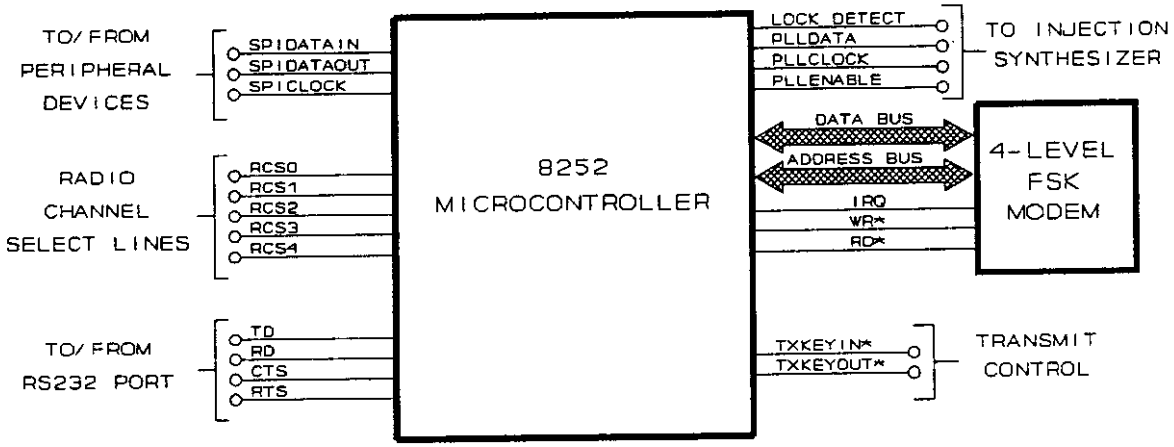

Figure 5. Microcontroller Functional Block Diagram

The DT800 microcontroller controls all programmable devices in the radio and handles all internal and external communications. The microcontroller is in essence, the brain of the radio. The microcontroller is designed around the ATMEL AT89S8252 8-Bit Microcontroller with 8k bytes of downloadable Flash memory (programmable and erasable read only memory), 2k bytes of EEPROM (Electrically Erasable Programmable Read Only Memory), and 256 x 8 bit internal RAM (Random Access Memory). The microcontroller also contains a SPI serial interface for programming peripheral devices, and a programmable UART (Universal Asynchronous Receiver/Transmitter) which handles the serial port. Reference ATMEL AT89S8252 product specification for more detailed information on this part.

The microcontroller is responsible for keeping the radio on channel by programming the digital PLL frequency synthesizer. This task is accomplished via a serial communications interface which consists of three signals PLLDATA, PLLCLOCK, and PLLENABLE. The PLLDATA signal provides the PLL data for the synthesizer, the PLLCLOCK signal clocks the data into the synthesizer, and the PLLENABLE signal enables synthesizer programming. After initially programming the synthesizer, the microcontroller monitors the synthesizer's lock detect signal. Upon detecting a un-locked condition, the microcontroller will re-program the synthesizer to lock the radio on channel.

The microcontroller controls the DT800's internal 4-Level FSK modem. In the transmit mode of operation, the microcontroller accepts application data from an external device via a RS232 interface using the BXRI protocol. The BRXI protocol provides for error checking and identifies the individual messages (also known as frames) in the serial data stream. The microcontroller then encrypts the message using DES and forwards this data to the modem

for transmission. In the receive mode of operation, the modem passes received application data to the microcontroller. The microcontroller checks the ID field of the standard message portion of the received message to determine whether to pass this message to the external device. If so, it decrypts the message, attaches the BRXI header and forwards the data to the external device via the RS232 interface.

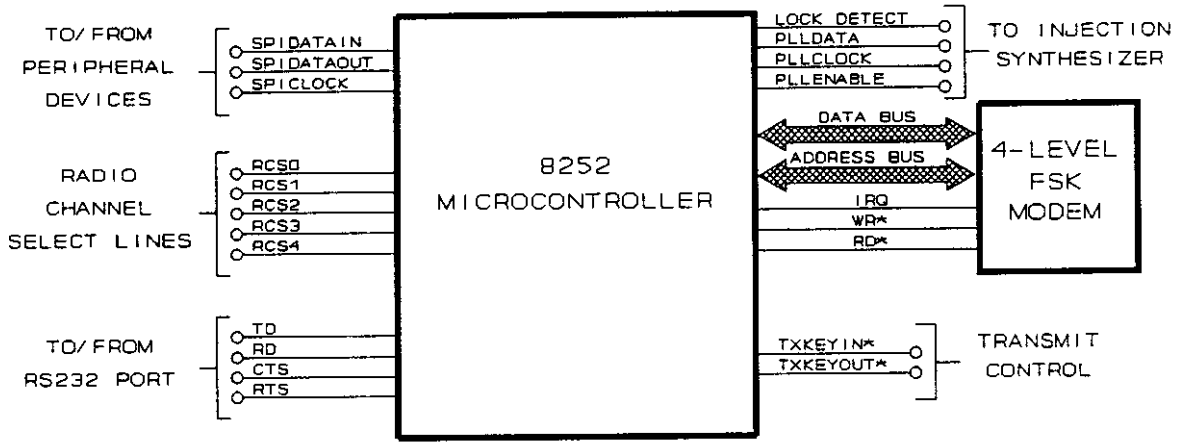

Figure 5. Microcontroller Functional Block Diagram ***(Repeated for reader convenience)***

The microcontroller controls peripheral devices (control head display, CTCSS encoder/decoder, etc.) via a serial communications interface which consists of SPIDATAIN, SPIDATAOUT, SPICLOCK, and various chip enable signals. SPIDATAIN provides data to the microcontroller, SPIDATAOUT provides data from the microcontroller to various devices, SPICLOCK provides synchronization of the data and the various chip enable lines determine which device is communicating with the microcontroller. The microcontroller also supports a 5-bit parallel data interface for external channel selection (32 channels can be accommodated by this method). The microcontroller continuously monitors the five RCS (Radio Channel Select) lines (RCS0* through RCS4*); and, upon detecting a change in state, will automatically load new frequency information into the frequency synthesizer. The microcontroller also reloads the frequency synthesizer when switching between transmit and receive modes.

The microcontroller provides a programmable transmit time-out-timer function to eliminate the possibility of inadvertent continuous transmit operation.

5.2 4-Level FSK Modem Section

The DT800 contains an internal 4-Level FSK modem for reliable transfer of data over-the-air. The modem interfaces with the microcontroller and the DT800's modulation / demodulation circuits to deliver reliable two-way transfer of high-speed application data over a wireless link.

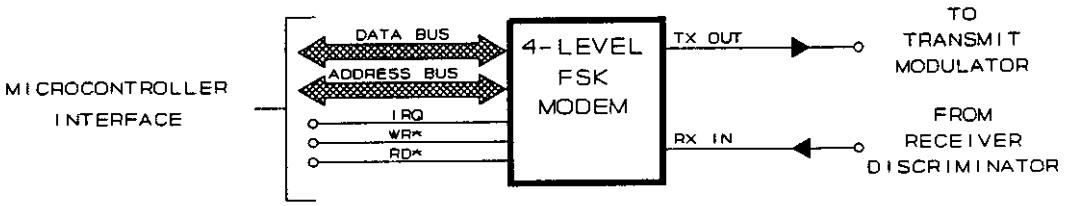

Figure 6. 4-Level FSK Modem Functional Block Diagram

The modem assembles application data received from the microcontroller, adds forward error correction (FEC) and error detection (CRC) information and interleaves the result for burst-error protection. After automatically adding symbol and frame sync codewords, the data packet is converted into filtered 4-Level analog signals for modulating the DT800's transmitter.

In the receive mode, the modem performs the reverse function using the analog signals from the receivers discriminator. After error correction and removal of packet overhead, the recovered application data is supplied to the microcontroller. CRC detected residual errors will be flagged.

The modem uses data block sizes and FEC/CRC suitable for high-speed transfer of data over narrow-band radio links. The modem can be operated at 4.8 kbps, 9.6 kbps, and 19.2 kbps under software control.

The modem is a highly integrated device incorporating many advanced features which are beyond the scope of this document. Reference MX•COM MX919A 4-Level FSK Modem Data Pump product specification for more detailed information regarding this device.

5.3 Injection Synthesizer

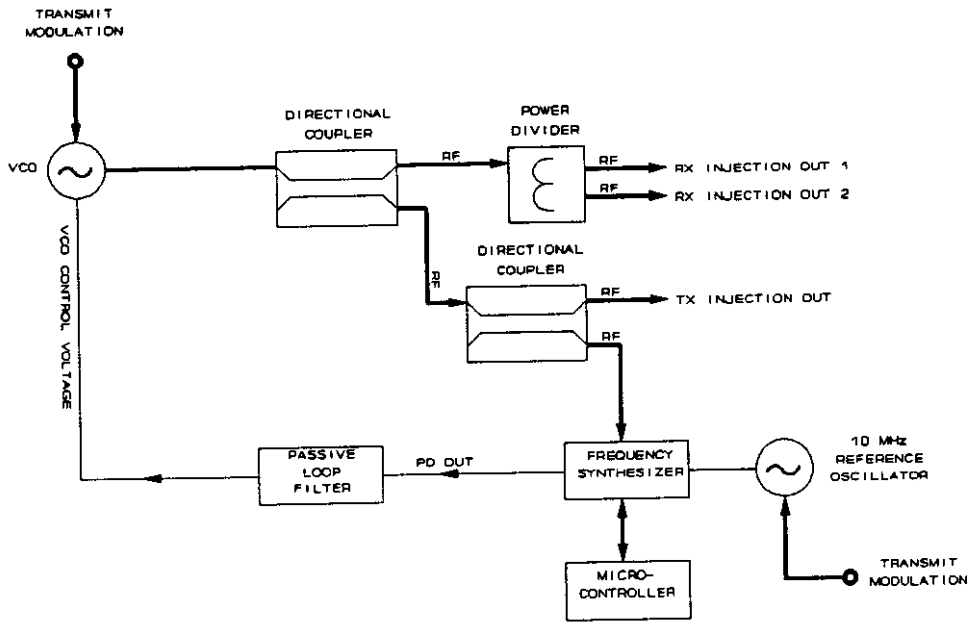

Figure 7. Injection Synthesizer Functional Diagram

The injection synthesizer creates the receiver injection signals in the receive mode of operation, and the transmit injection signal during transmit operation. *Figure 7* is a functional diagram of the DT800's injection synthesizer section.

The receiver injection frequency is 45 MHz below the base station transmit frequency

The 815 MHz (nominal) signal from the VCO is applied to a directional coupler. The coupler splits this signal into two signals. One of these signals is divided by a power divider into two equal amplitude signals (RX INJECTION OUT 1 and RX INJECTION OUT 2) which are used by the DT800's dual receivers mode. The receivers mix the injection signals (45 MHz below the operating frequency) with the 860 MHz (nominal) received signal to produce a 45 MHz IF (Intermediate Frequency) signal. The other signal from the directional coupler is applied to a second directional coupler which produces the TX INJECTION OUT signal and the feedback signal to the frequency synthesizer.

TX INJECTION OUT is used by the DT800's transmitter during transmit operation. Transmit modulation is applied to VCO as well as the 10 MHz reference oscillator to produce FM modulation (reference the transmit processing section for more detailed information). The TX INJECTION OUT signal is sent to the power amplifier section for final amplification prior to transmission.

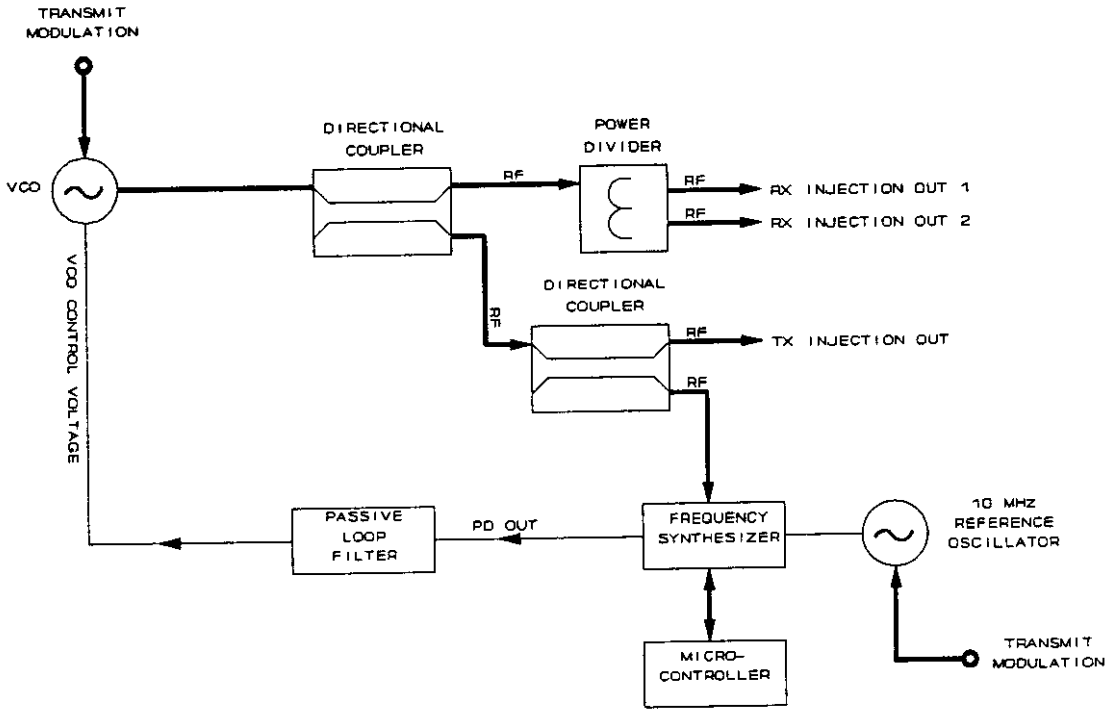

Figure 8. Injection Synthesizer Functional Diagram

The feedback signal is used at all times by the digital frequency synthesizer to keep the radio on channel.

The frequency synthesizer divides the injection signal to produce a quotient signal of 12.5 kHz. The synthesizer also divides the signal from the 10.0 MHz reference oscillator to produce a 12.5 kHz signal. The synthesizer compares the phase of these two signals and outputs a signal (PD OUT) proportional to their phase difference. A passive loop filter converts the PD OUT signal to a DC control voltage which locks the VCO on channel.

In this manner, the VCO is compared to - and forced to emulate - the high-stability reference oscillator. This configuration is commonly referred to as a digital Phase-Locked-Loop (PLL) frequency synthesizer.

5.4 Transmit Baseband Processing

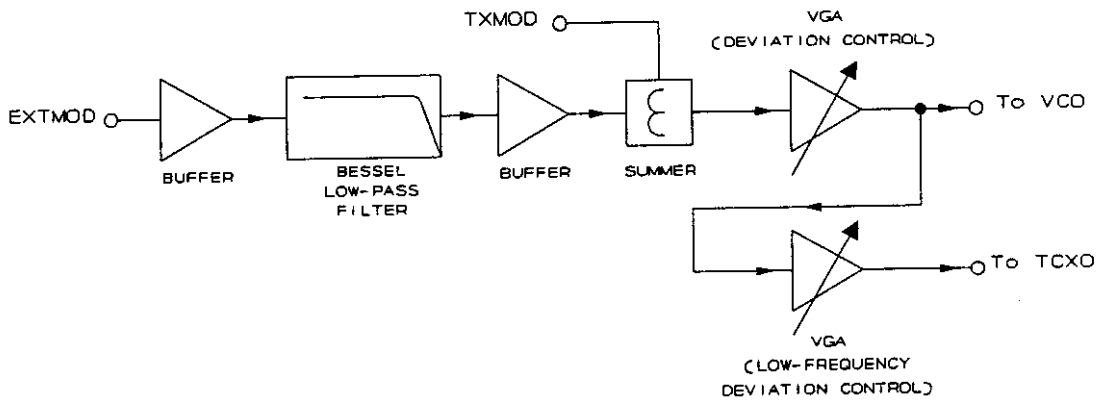

Figure 9. Transmit Baseband Processing Functional Diagram

Figure 9 is a functional diagram of the DT800's transmit baseband processing section.

The DT800 is capable of being modulated by an external device (control head, external modem, etc.) or by the internal 4-level FSK modem. External modulation and internal modem modulation are, at any one point in time, mutually exclusive.

External modulation (EXTMOD) from an external device (control head, external modem, etc.) is buffered to provide load isolation and is then routed to a fourth-order Bessel low-pass filter. The purpose of this filter is to remove any high-frequency components present in the external modulation prior to application to the transmit modulator. Following the filter, the external modulation is buffered to provide load isolation to the filter. The modulation is routed though a summer and is applied to a VGA (Variable Gain Amplifier) which provides transmit modulation deviation control.

The output of the first VGA directly modulates the VCO. This signal is also routed through another VGA which provides low-frequency deviation control by modulating the reference oscillator. This configuration is referred to as two-point modulation (with the VCO and the reference oscillator being the two modulation points). Two point modulation prevents the radio's PLL circuitry from counteracting the modulation process, and provides a clean flat modulation response to the low frequency portion of the baseband spectrum.

4-level FSK modulation from the internal modem bypasses the Bessel filter as the modem contains built-in filtering. This modulation is routed through the summer and is similarly sent to the VCO and reference oscillator in the same manner as the external modulation.

5.5 UHF Receiver

The DT800 employs two independent, high-performance, low-noise, dual conversion FM receivers. The receiver is divided into two main sections, a front-end section and a 45 MHz receiver section.

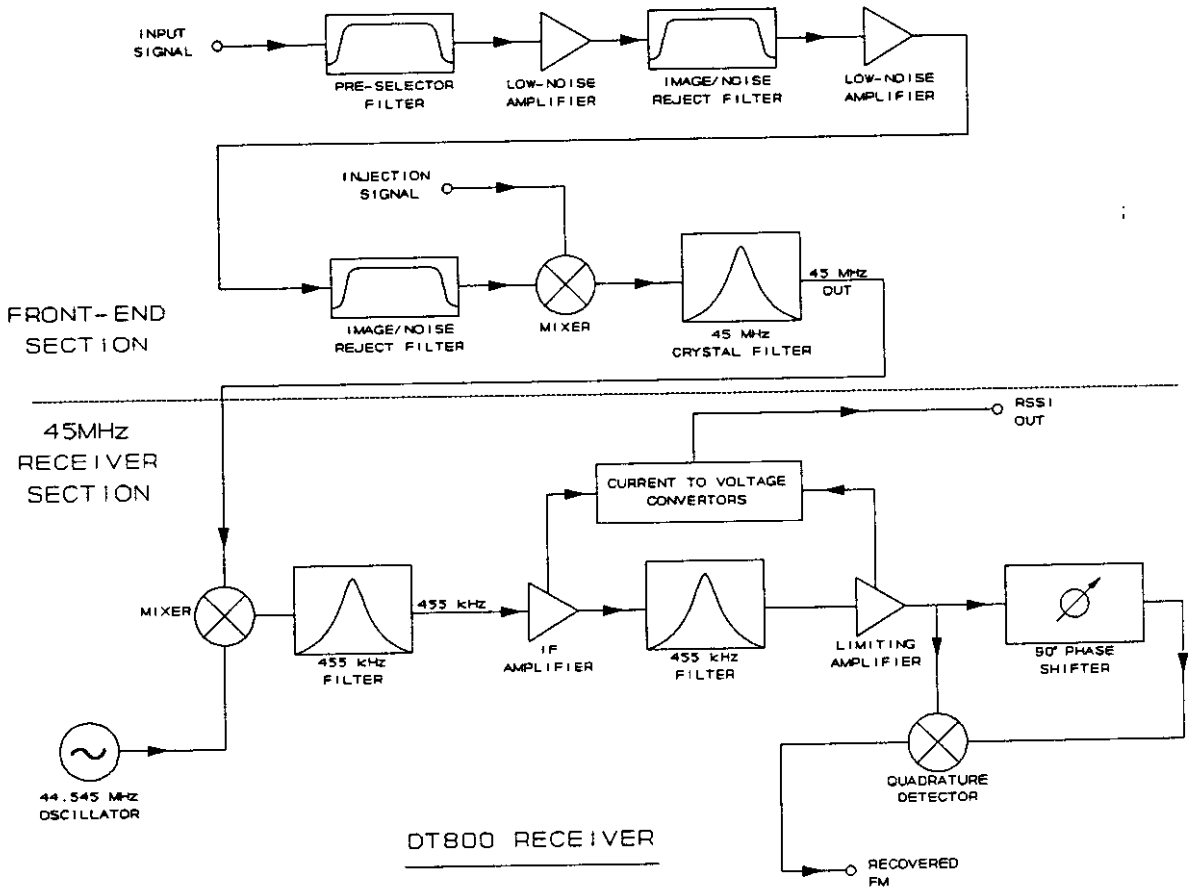

Figure 10. UHF Receiver Functional Diagram

5.5.1 UHF Front-End Section

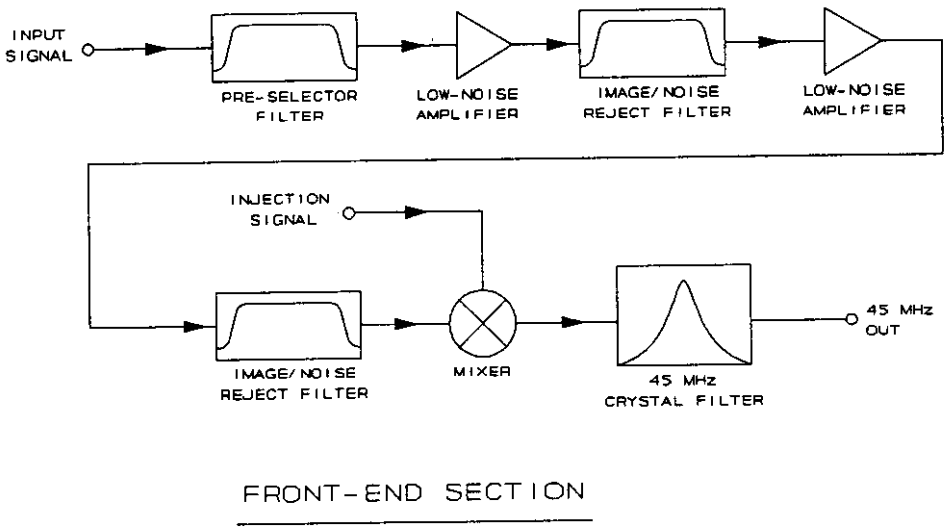

Figure 11. UHF Receiver Front-End Functional Diagram

Figure 11 is a functional block diagram of the receiver front-end section. The front-end section employs an advanced-architecture cascaded-LNA (Low Noise Amplifier) design for extreme sensitivity and high-overload performance.

Receiver input signals are first filtered by a pre-selector band-pass filter and are then routed to a LNA. The amplified signal is routed through another band-pass filter (which functions as a image/noise reject filter) to a second LNA. The output of the second LNA is passed through yet another band-pass filter.

The cascaded LNA configuration ensures a very low receiver noise figure which translates to increased sensitivity. The cascaded band-pass filter configuration acts to sharpen the filter's frequency response skirts, thereby providing greater out-of-band rejection performance.

After the final band-pass filter, the signal is applied to a mixer where it is mixed with the receiver injection signal (45 MHz below the received signal) to produce a first IF (Intermediate Frequency) of 45 MHz. The 45 MHz IF is passed by a 45 MHz crystal filter and is routed to the 45 MHz receiver section for further processing.

5.5.2 45 MHz Receiver Section

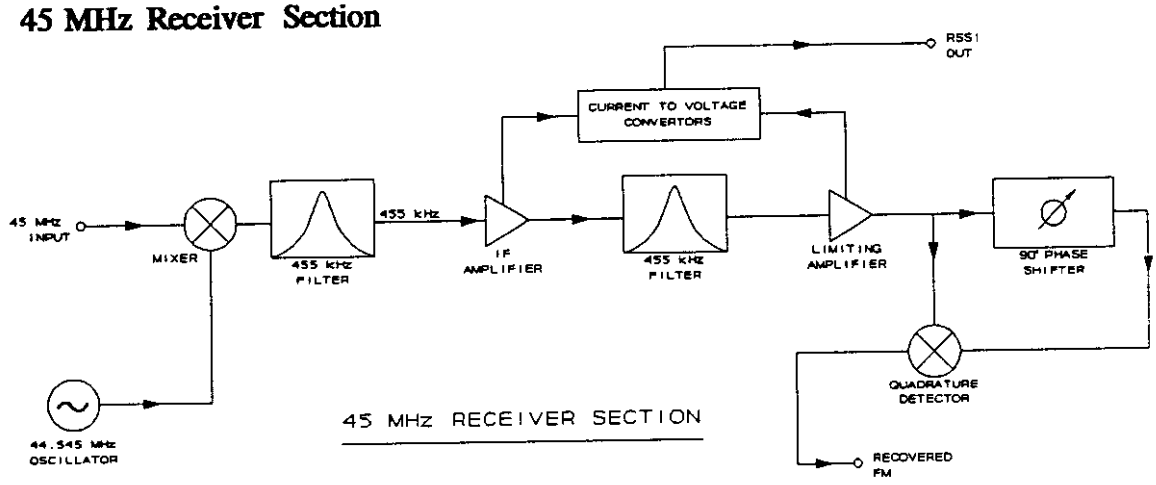

Figure 12. 45 MHz Receiver Functional Diagram

Figure 12 is a functional block diagram of the 45 MHz receiver. The 45 MHz first IF from the front-end is mixed with a 44.545 MHz injection frequency to produce a 455 kHz second IF which is passed by a 455 kHz filter. The second IF is then amplified and limited by an IF amplifier and limiting amplifier respectively. A 455 kHz filter provides interstate filtering between the IF amplifier and the IF limiting amplifier.

This section includes the current-to-voltage convertors which produce the RSSI signal (a DC voltage proportional to the log of the received signal strength). The RSSI responds to signals as low as -132 dBm and rises monotonically over a range of approximately 90 dB. RSSI is used by the diversity reception system to select the best receiver at any particular point in time.

The output of the limiting amplifier is applied to a tuned quadrature detector which outputs recovered Frequency Modulation (FM).

5.6 Diversity Reception Controller

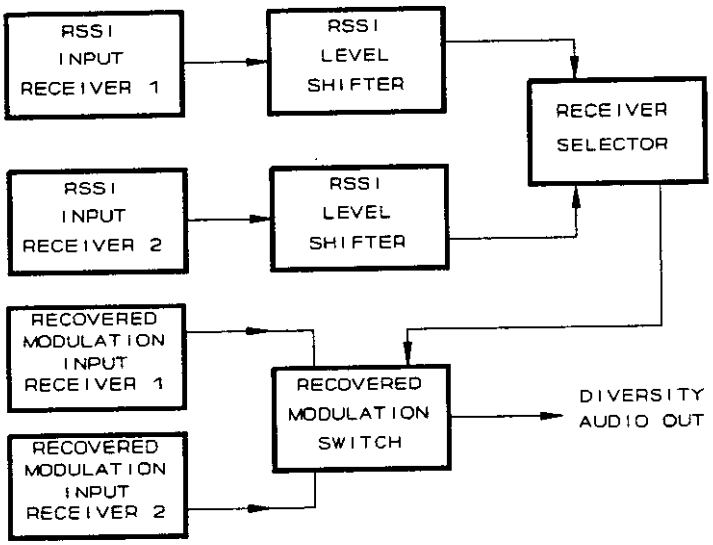

Figure 13. DRC Functional Block Diagram

Figure 13 is a functional block diagram of the DRC (Diversity Reception Controller). The DRC is the central processor of a dual-receiver diversity reception system. The DRC accepts inputs from two receivers, determines which receiver has the better SNR (Signal to Noise Ratio), and selects that receiver to supply recovered modulation.

High-speed RSSI from both receivers are processed by the RSSI input and RSSI level shifter sections and are then forwarded to the receiver selector, and carrier detector sections. The receiver selector selects the appropriate receiver and the carrier detector provides a high-speed indication of channel activity.

Recovered modulation from both receivers is processed by the recovered modulation input and is sent to the recovered modulation switch which performs the actual selection process as directed by the receiver selector.

The DRC is divided into 7 functional sections.

5.6.1 RSSI Input Section

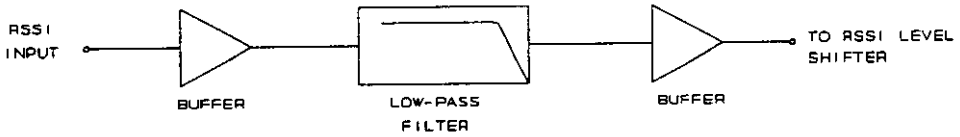

Figure 14. RSSI Input Section Functional Diagram

Figure 14 is a functional diagram of the RSSI input section of the DRC (or ease off explanation, only one section is shown). RSSI from each receiver is buffered to provide RSSI load isolation. Next, the buffered RSSI is low-pass filtered to remove high frequency components (above the frequency of fade induced amplitude fluctuations). This improves the diversity selection process at relatively low RF levels. Finally, the conditioned RSSI is buffered again for isolation and forwarded to the level shifter for further processing.

5.6.2 RSSI Level Shifter

Figure 15. RSSI Level Shifter Block Diagram

Figure 15 is a block diagram of the DRC's RSSI level shifter (or ease of explanation, only one section is shown). The purpose of the level shifter is to compensate for discrepancies in RSSI and sensitivity between receivers. The RSSI level shifter essentially equalizes the performance of the receivers. The level shifter contains an amplifier with adjustable slope and adjustable threshold levels. The output of the level shifter is sent to the receiver selector and carrier detector sections.

5.6.3 Receiver Selector

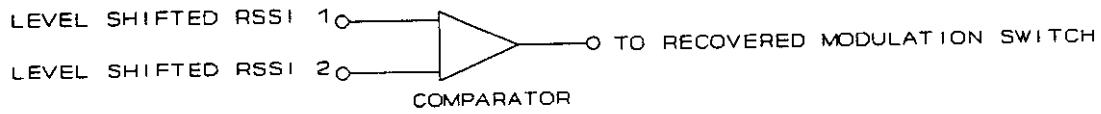

Figure 16. Receiver Selector Functional Diagram

Figure 16 is a functional diagram of the DRC's receiver selector. The receiver selector uses level-shifted RSSI to select the appropriate receiver. In essence, the selector is a comparator which will output one logic level if receiver 1 RSSI is higher than receiver 2 RSSI (and will output the other logic level otherwise). This section develops the control signal used to actuate the recovered modulation switch.

5.6.4 Recovered Modulation Input

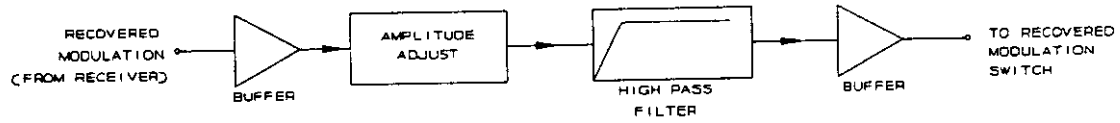

Figure 17. Recovered Modulation Input Functional Diagram

Figure 17 is a functional diagram of the recovered modulation input. Recovered modulation from the receiver is first buffered to provide load isolation. This buffered signal is then sent to a level adjust circuit which equalizes its amplitude. The signal is then high-pass filtered to remove low-frequency components of the recovered signal (below the frequency of the modulation). Finally, the signal is buffered for isolation and forwarded to the recovered modulation switch.

5.6.5 Recovered Modulation Switch

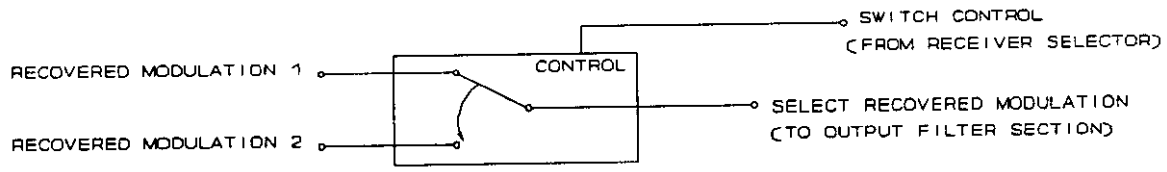

Figure 18. Recovered Modulation Switch Functional Diagram

Figure 18 is a functional diagram of the DRC's recovered modulation switch. This section receives recovered modulation from both receivers as inputs. A control signal from the receiver selector actuates the switch appropriately. The output of the switch is diversity reception recovered modulation.

5.6.6 Carrier Detector

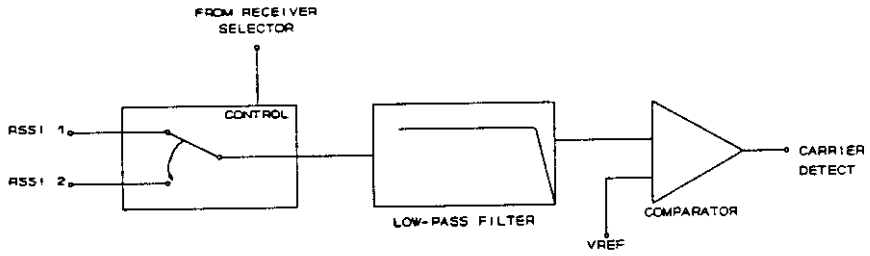

Figure 19. Carrier Detector Functional Diagram

Figure 19 is a functional diagram of the DRC carrier detector. The carrier detector receives RSSI from both receivers. A control voltage (from the receiver selector) continuously selects RSSI from the selected receiver. This select RSSI signal is then low-pass filtered to remove any switch induced transients and to improve performance at relatively low RF levels. This signal is applied to a comparator. If the signal is above a reference value, the comparator will generate a logic low indicating carrier activity. The threshold of carrier detect is factory set to -107 dBm.

5.7 Receive Baseband Processing

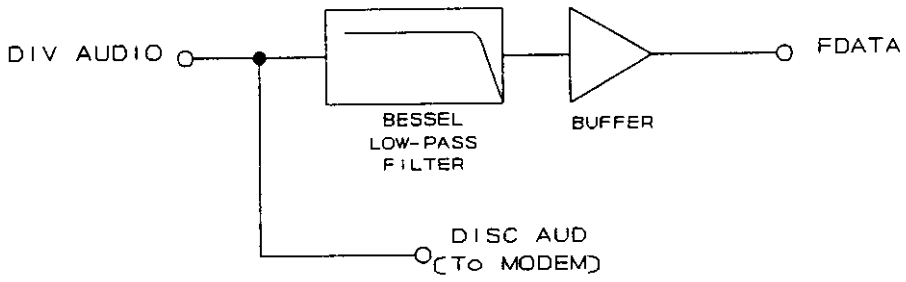

Figure 20. Receive Baseband Processing

Figure 20 is a functional diagram of the receive baseband processing section.

DIVAUDIO (diversity audio) from the diversity reception controller is routed to two separate paths, depending on whether the audio is destined for an external device (control head, eternal modem, etc.) or for the internal 4-level FSK modem.

DIVAUDIO is routed directly to the internal modem as the modem contains internal filtering of received signals.

For an eternal device, DIVAUDIO is routed through a 4800 Hz fourth-order Bessel low-pass filter. The primary purpose of the filter is to improve the SNR (Signal to Noise Ratio) of the recovered signal. Secondarily, the filter removes any transients induced by the high-speed switching action of the diversity reception controller. Following the filter, the signal is buffered to provide load isolation and is routed to an external device as FDATA (filtered, diversity recovered modulation).

5.8 Power Amplifier Module

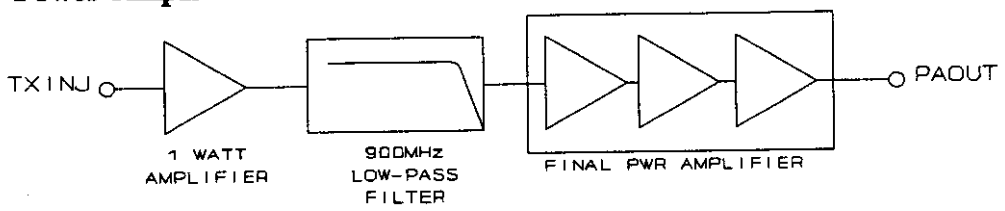

Figure 21. Power Amplifier Functional Diagram

Figure 21 is a functional diagram of the power amplifier. The transmit injection signal from the RF injection section is applied to a 1 watt amplifier. *Following the amplifier, a 900 MHz low-pass filter reduces spurious and harmonic emissions*. The signal is then routed to the final power amplifier which provides approximately 20 dB of gain, boosting the output signal to 25 Watts. This signal is routed to the T/R switch for transmission.

5.9 T/R (Transmit/Receive) Switch

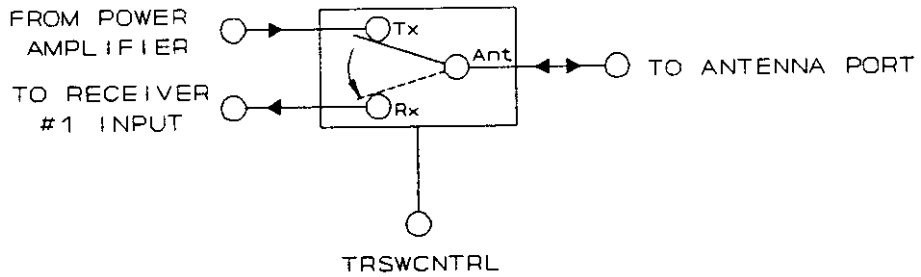

Figure 22. Transmit/Receive Switch Functional Diagram

Figure 22 is a functional diagram of the T/R switch. The T/R switch enables one antenna port to function as both a transmit port and as a receive port. A control signal TRSWCNTRL is used to actuate the switch. *The internal configuration of the T/R switch also attenuates even-order harmonics.*

6. GLOSSARY

BASEBAND	A signal whose frequency content is centered around DC (or 0 frequency)
BESSEL FILTER	A filter with a linear phase response.
CMOS	Complementary Metal Oxide Semiconductor - A type of integrated circuit with low power consumption.
CPM	Continuous Phase Modulation, a family of modulation schemes in which no phase discontinuities are present.
CTCSS	Continuous Tone Coded Squelch System, a sub-audible signalling format which utilizes tones between 67 and 254 Hz. Used primarily to separate different voice systems sharing the same RF channel.
DES	DES is the Data Encryption Standard, a block cipher defined and endorsed by the U. S. government in 1977 as an official standard.
EEPROM	Electrically Erasable Programmable Read Only Memory
EMI	Electromagnetic Interference
FM	Frequency Modulation - a form of modulation where the carrier frequency is shifted an amount proportional to the modulating signal's amplitude at a rate proportional to the modulating signal's frequency.
FSK	Frequency Shift Key - digital modulation (a form of FM) where the carrier frequency is shifted above and below the operating frequency (in discreet steps) in response to a digital data input.
4-LEVEL FSK	A form of FSK where the carrier frequency is shifted from the operating frequency by 1 of 4 displacement frequencies, 2 above and 2 below the operating frequency
IMAGE FREQUENCY	The unwanted sum or difference frequency

	which occurs naturally in the frequency conversion process.
HALF DUPLEX	A dual frequency mode of operation which inhibits simultaneous transmission and reception.
LNA	Low Noise Amplifier
NOISE FIGURE	The "Figure of Merit" of an amplifier. Specifically, noise figure is a measure of the degradation in SNR between the input and output ports of a network.
PCB	Printed Circuit Board
PHASE NOISE	A measure of the purity of a discreet frequency (expressed in -dBc/Hz at some offset frequency)
PLL	Phase Locked Loop - a circuit configuration used to lock the frequency of a VCO to a high stability reference oscillator.
PPM	Parts Per Million (normally expressed with lower case letters, ppm)
RCS	Radio Channel Select
RF	Radio Frequency
RFI	Radio Frequency Interference
SINAD	The ratio of (Signal + Noise + Distortion) to (Noise + Distortion)
SMT	Surface Mount Technology - electronic components which make electrical contact on the surface layer of a PCB (as opposed to thru-hole components). SMT devices provide reduced size and increased performance.
SNR	Signal to Noise Ratio
TCVCXO	Temperature Compensated Voltage Controlled Crystal Oscillator

TRANSMIT ATTACK TIME	The elapsed time from transmit key assertion to 90% rated RF power is achieved.
UHF	Ultra High Frequency, the frequency band from 300 to 3,000 MHz
VCO	Voltage Controlled Oscillator - an oscillator whose frequency can be adjusted by a DC control voltage.
VGA	Variable Gain Amplifier