Letter of Class I Permissive Change

June 20, 2017

Subject: Class I Permissive Change for FCC ID: VOB-P2180, IC:7361A-P2180

To whom it may concern:

We Audix Technology Corp., hereby declare that FCC ID: VOB-P2180, IC:7361A-P2180 is applied class I permissive change, The differences between this application and original's ID as clarify in following pages.
After we confirmed there is nothing changed to RF related part and assessment that do not degrade the RF characteristics reported by the manufacture.

Sincerely Yours,

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Mr. Ben Cheng
Manager
AUDIX Technology Corporation

Incremental schematics and layout change history from P2180_A01 to P2180_A04 is below.
Note: FAB 1 = A01, FAB 2 = A02, FAB 3 = A03, FAB 4 = A04

Summary of P2180 Fab 2 Schematic and Layout Change History 10/28/15

1. Converted using A01 Rev #13 schematic in the P4. No change in the schematic.

P2180 Fab 1 Layout Change History

1. Changed the solder mask and solder paste to populate only C801, C784, C780, C803A, C806A.

Detail P2180 Fab 2 Schematic Change History

Revision 1: 9/24/15
Converted using A01 Rev #13 schematic in the P4.

Summary of P2180 Fab 3 Schematic and Layout Change History 4/12/16

P2180 Fab 3 Schematic & BOM Change History

1. Fix Power down sequence
   a. VIN_PWR_BAD, TMP451 Therm, Tegra SHUTDOWN Pin, Force OFF are tied to MON input pin of PMIC instead of SHDN pin of PMIC.

      SW Need to program MBLPD Bit to 1 in BL to turn OFF the system when MON I/P goes Low.

      SW changes in BL and Kernel are highlighted in the table below:

	OTP	Bootloader	Kernel
New	1.28ms FPS	1.28ms FPS (same as OTP)	1.28ms FPS
	LDO4 Discharge enabled CNFG2_L4[1]= 1	LDO4 Discharge Disabled CNFG2_L4[1]= 0	LDO4 Discharge Disabled CNFG2_L4[1]= 0
	MBLPD = 0	MBLPD = 1	MBLPD = 1

b. Added discharge circuitry on CVM for CPU, GPU, 1.8V (SD3), DDR 1.1V (SD1), PLL 1.05V (LDO7), 3.3V (Ext Reg) which gets triggers from nRST_IO of PMIC.

c. Added active discharge for PMIC GPIO's that enables CPU & GPU Regulators (100K Pulldown on GPIO's are not enough).

d. CARRIER_PWR_ON will ramp down faster using VIN_PWR_BAD (Wired OR).

e. Added x4 330uF POS Caps at 5V Pre-reg O/P.

2. Support LAN WAKE up feature by connecting Ethernet WAKE signal to QSPI_CS (IO3_PEE.01)

3. Connected CVM Connector pin USB2_EN_OC to Tegra USB_VBUS_EN1 GPIO.
This change applies only when using P2180 with E2598 SLT SKU 1199 and MODS SW has to control ON/OFF of J503 USB2 Power thru USB_VBUS_EN1 GPIO and can also check for Over Current.

4. Changed U103 EEPROM from 8Kb NVPN 174-0165-000 to 2K, Atmel AT24C02D-MAHM-T, NVPN 174-0159-000.

5. To select the right trip point for voltage comparator.
   a. Removed R57 100K 1% 00402.
   b. Replaced R58 from 44.2K 1% 0402 to 34K 1% 0402, NVPN 195-0260-000.
   c. Replaced R50 from 100K 1% 0402 to 110K 1% 0402, NVPN 195-0026-000.
   d. Replaced R56 from 25.5K 1% 0402 to 49.9K 1% 0402, NVPN 195-0340-000.
6. To change 5.0V pre-regulator output to 4.8V and adjust compensation values
   a. Removed C526, C1205, R517, R518.
   b. Replaced R519 from 13.7K 1% 0402 to 30.9K 1% 0402.
   c. Replaced R520 from 100K 1% 0402 to 95.3K 1% 0402.
   d. Replaced C527 from 6.8nF 50V 10% 0402 to 33nF 16V 10% 0402, NVPN 036-0111-000.
   e. Replaced U503 TPS54335DRCT, NVPN 316-0420-000 to TPS54335ADRCT, NVPN 316-0460-000.

7. MISC BOM changes.
    a. Not populated R871 0 ohm 0201, NVPN 195-1636-000.
    b. Replaced U503 TPS54335DRCT, NVPN 316-0420-000 to TPS54335ADRCT, NVPN 316-0460-000.
    c. Replaced R976, R977 from 10 ohm 5% 0805 to 20 ohm 5% 0805, NVPN 195-1948-000.
    d. Removed R984, R985 10 ohm 5% 0805.
8. Change J1 NVPN 080-1277-000 (Samtec PN: REF-186137-01) to NVPN 080-1337-000 (Samtec PN: REF-186137-03).

P2180 Fab 3 Layout Change History

1. Changed the layout based on the schematic changes above as major items.
2. It's to remove the voids (shape keep outs) on layers 2, 4, 7 and 9 to allow the ground net to fill in and help even out the copper distribution to help prevent warpage. Requested on 10/21/15.

Detail P2180 Fab 3 Schematic Change History

Revision 1: 10/7/15

1. Page 25:
   a. Replaced L27 from 2.2nH NVPN 130-0293-000 to 0.6nH 0201, NVPN 030-0341-000 – No layout change.
   b. Changed C155, C158 4.7pF 0201 to L30, L31 15nH 0201, NVPN 130-0360-000 – No layout change.
2. Page 41:
   a. Changed R813 from 0 ohm 0201 to 10K 5% 0201, NVPN 195-2005-000 – No layout change.
   b. Moved R516 0 ohm 0201 from page 44.
   c. Changed Q509.3 from THERM_SHUTDOWN* to U4.A2 PS_PMIC_MONITOR.
   d. Changed R871 0 ohm 0402 to 0 ohm 0201 and changed the connection.
   e. Added R818 0 ohm 0201.
3. Page 44:
   a. Moved R516 0 ohm 0201 at VIN_PWR_BAD* to page 41.
   b. Removed C972 at Q977 gate.
4. Page 48:
   a. Changed D970 from BAT54ALT1 SOT23, NVPN 091-0004-000 to CFSH05-20L SOD882, NVPN 090-0283-000.
   b. Changed C970 from 22uF 20% 35V 0805, NVPN 032-0213-000 to 22uF 10V 15% 0805LP, NVPN 039-0190-000.
   c. Removed Q970, R970 –R972, C971.
   d. Added R979 10 ohm 5% 0805, NVPN 195-1592-000 at Q971.3 and changed the other side of 10 ohm from VDD_EXT_CPU_REG_EN_R to VDD_CPU_AP.
   e. Added R980 10 ohm 5% 0805, NVPN 195-1592-000 at Q973.3 and changed the other side of 10 ohm from VDD_EXT_GPU_REG_EN to VDD_GPU_AP.
   f. Changed Q971, Q973 from AO3416 SOT23, NVPN 300-0329-000 to NTK3134NT1G SOT723, NVPN 300-0688-000 and changed the connection.
   g. Changed Q976 from AO3416 SOT23, NVPN 300-0329-000 to NTK3134NT1G SOT723, NVPN 300-0688-000 and changed the connection.
   h. Added R978 100K 5% 0402.
   i. Added C973 100pF 25V 0201.
   j. Removed Q972, Q974, Q975, R975.

Revision 2: 10/7/15

1. Page 41: Added D516 Zener diode at U4.A2 PS_PMIC_MONITOR to protect the damage of PMIC.
2. Page 43: Changed U526.3 from GPU_PWR_REQ_SHIFT to VDD_EXT_GPU_REG_EN_R.
3. Page 44: Changed Q977 from AO3416 SOT23, NVPN 300-0329-000 to NTK3134NT1G SOT723, NVPN 300-0688-000.
4. Page 48:
    a. Changed back Q971 and connected Q971.3 to VDD_EXT_CPU_REG_EN_R same as E3301-A01. Also changed it from AO3416 SOT23, NVPN 300-0329-000 to NTK3134NT1G SOT723, NVPN 300-0688-000.
    b. Changed back Q973 and connected Q973.3 to VDD_EXT_GPU_REG_EN_R. Also changed it from AO3416 SOT23, NVPN 300-0329-000 to NTK3134NT1G SOT723, NVPN 300-0688-000.
    c. Changed Q971 to Q975 for VDD_CPU_AP discharge to keep A01 placement.
    d. Changed Q973 to Q974 for VDD_GPU_AP discharge to keep A01 placement.

Revision 3: 10/13/15

1. Page 18:
    a. Changed R784.1 from ADC_INT_R to LANWAKEB_1V8_R.
    b. Changed R784.2 from ADC_INT to LANWAKEB_1V8.
2. Page 26:
    a. Added U29, C222, C223 level translator for LANWAKE implementation.
    b. Added “NS” at R582.
3. Page 41:
    a. Replaced D516 Zener diode from BZT52C3V9T SOD523, NVPN 090-0212-000 to MM3Z4V7ST1G SOD323, NVPN 0900224-000.
    b. Replaced R871 from 0 ohm 0402 to 0 ohm 0201.
4. Page 49: Removed U529, R1523, C876, C884 for ADC.

Revision 4: 10/15/15

1. Page 48:
    a. Added Q978, R981 for VDD_1V8 discharge circuit.
    b. Added Q979, R982 for VDD_DDR_1V1_AP discharge circuit.

Revision 5: 10/16/15

1. Page 48: Changed Q979.3 from VDD_1V8_DISCHARGE to VDD_DDR_1V1_DISCHARGE.

Revision 6: 10/22/15

1. Page 42: Changed R902 from 0 ohm 0201 to 470 ohm 5% 0201, NVPN 195-2116-000.
2. Page 43: Changed R795 from 0 ohm 0201 to 470 ohm 5% 0201, NVPN 195-2116-000.
3. Page 44:
    a. Replaced C530, C531 from CAP POLY 100uF 20% 6.3V 3216 to Kemet, T520B337M006ATE040 CAP POLY 330uF 20% 6.3V 3528, NVPN 032-0696-000.
    b. Added C532, C533 Kemet, T520B337M006ATE040 CAP POLY 330uF 20% 6.3V 3.5X2.8X1.9mm, NVPN 032-0696-000.
    c. Changed R977 from 56 ohm 5% 0603 to 10 ohm 5% 0805, NVPN 195-1592-000.
    d. Added R976 10 ohm 5% 0805, NVPN 195-1592-000 parallel to R977 for VDD_3V3 discharge.
4. Page 48:
9. Added R983 Q980 for AVDD_1V05_PLL_AP.
10. Changed R981, R982 from 56ohm 5% 0805, NVPN 195-1605-000 to 10 ohm 5% 0805, NVPN 195-1592-000.
11. Added R984 10 ohm 5% 0805, NVPN 195-1592-000 parallel to R981 for VDD_1V8 discharge.
12. Added R985 10 ohm 5% 0805, NVPN 195-1592-000 parallel to R982 for VDD_DDR_1V1 discharge.

Revision 7: 10/22/15

1. Corrected T210 DSC JEDEC error which netin using incomplete.ptf

Revision 8: 10/23/15

1. Page 33:
    a. Added U 74LVC1G07GW open drain buffer for VIN_PWR_BAD*.
    b. Added C1210 0.1uF 10% 0201.
2. Page 35: Added R564 0 ohm 0201 to connect to USB_VBUS_EN1.

Revision 9: 10/28/15

1. Page 41: Added "NS" at D516.

Revision 10: 11/26/15

1. Page 41: Removed R871 0 ohm 0201, NVPN 195-1636-000 in the SKU schematic.

Revision 11: 12/17/15

1. Page 6: (Select the right trip point for voltage comparator, http://nvbugs/1697393)
    a. Removed R57.
    b. Replaced R58 from 44.2K 1% 0402 to 34K 1% 0402, NVPN 195-0260-000.
    c. Replaced R50 from 100K 1% 0402 to 110K 1% 0402, NVPN 195-0026-000.
    d. Replaced R56 from 25.5K 1% 0402 to 49.9K 1% 0402, NVPN 195-0340-000.
2. Page 44: (To change 5.0V pre-regulator output to 4.8V and adjust compensation values)
    a. Removed C526, C1205, R517, R518.
    b. Replaced R519 from 13.7K 1% 0402 to 30.9K 1% 0402.
    c. Replaced R520 from 100K 1% 0402 to 95.3K 1% 0402.
    d. Replaced C527 from 6.8nF 50V 10% 0402 to 33nF 16V 10% 0402, NVPN 036-0111-000.
13. Replaced U503 TPS54335DRCT, NVPN 316-0420-000 to TPS54335ADRCT, NVPN 316-0460-000.

Revision 12: 12/18/15

1. Page 44:
    a. Replaced U503 TPS54335DRCT, NVPN 316-0420-000 to TPS54335ADRCT, NVPN 316-0460-000.
    b. Replaced R976, R977 from 10 ohm 5% 0805 to 20 ohm 5% 0805, NVPN 195-1948-000.
2. Page 48: Removed R984, R985 10 ohm 5% 0805.

Revision 13: 4/12/16

1. Change J1 NVPN 080-1277-000 (Samtec PN: REF-186137-01) to NVPN 080-1337-000 (Samtec PN: REF-186137-03) in the Variant Editor.

Summary of P2180 Fab 4 Schematic and Layout Change History 6/2/16

P2180 Fab 4 Schematic & BOM Change History

14. No schematic and BOM changes in the A04 compared with A03
    The LATEST versions of P2180-A03 and P2180-A04 are the same besides the alternate U7 part.

On 12/10/15 and 12/27/15, ECO216436 and ECO216818 were released to implement the changes to P2180-A03 you see mentioned below.

ECO216818 (12/22/2015)

15. Updated the BOM to select the right trip point for voltage comparator, http://nvbugs/1697393, change 5.0V pre-regulator output to 4.8V and adjust compensation values
    a. Removed R57, NVPN 195-0005-000.
    b. Changed R58 from NVPN 195-0315-000 to 34K 1% 0402 NVPN 195-0260-000.
    c. Changed R50 from NVPN 195-0005-000 to 110K 1% 0402 NVPN 195-0026-000.
    d. Changed R56 from NVPN 195-0200-000 to 49.9K 1% 0402 NVPN 195-0340-000
    e. Removed C526 NVPN 035-0017-000.
    f. Removed C1205 NVPN 035-0212-000.
    g. Removed R517 NVPN 195-0475-000.
    h. Removed R518 NVPN 195-0210-000.
    i. Changed R519 from NVPN 195-0070-000 to 30.9K 1% 0402 NVPN 195-0240-000.
    j. Changed R520 from NVPN 195-0005-000 to 95.3K 1% 0402 NVPN 195-0475-000.
    k. Changed C527 from NVPN 036-0141-000 to 33nF 16V 10% 0402 NVPN 036-0111-000.

ECO218277 (2/11/16)

16. Changed Y5 25MHz from 085-0277-000, TXC 7M25070081 to 085-0290-000, TXC 7M25070100 with 105C operation temperature.

ECO219139 (3/9/16)

17. List of cap changes from X5R to X6S, X7S or X7R to meet 95C requirement at caps. //syseng/WMP/Projects/T210/Embedded/Design/P2180/A04/P2180-A04_ X5R Alternatives.xlsx.
18. ~~Added Alt crystals with 105C operation temperature~~ (Removed item 4 and updated y by item 7-9)
    ~~a. Y1 32.768KHz: 085-0293-000 TXC 9H03270062~~
    ~~b. Y2 38.4MHz: 085-0294-000, TXC 8Z38470012~~
    ~~c. Y4: 37.4MHz 085-0303-000, Siward XTL901190-N64-145~~
19. Removed R974 10M 5% 0402 which is not required to divide the VDD_MUX_CAP voltage.

ECO220315 (4/15/16)

20. Changed Y1, 32.768KHz primary Epson FC-12M32.7680KA-A3 (085-0174-000) to alternate and alternate TXC 9H03270062 (085-0293-000) to primary.
21. Changed Y2, 38.4MHz primary Epson Q24FA20H0028100 (085-0180-000) to alternate and alternate TXC 8Z38470012 (085-0294-000) to primary.

22. Changed Y4 37.4MHz primary Siward XTL901100-B63-172 (085-0203-000) to alternate and alternate Siward XTL901190-N64-145 (085-0303-000) to primary.
23. Deleted J1 alternate NVPN 080-1277-000 (Samtec PN: REF-186137-01).

ECO220947 (4/28/16)

24. Changed C111, C115 from 22pF 5% 0201 to 27pF 5% 0201, NVPN 035-0257-000.

ECO222172 (5/17/16)

25. Added NVPN 032-0810-000 as an alternate at C48.
26. Changed LB25 from 0 ohm 0201, NVPN 195-1636-000 to 0 ohm 0402, NVPN 195-2655-000 because of mismatching 0402 PAD size.

ECO222312 (5/22/16)

27. Added alternate P/N 032-0947-000 for C45,C104,C108,C114,C119-C120,C129,C134,C563-C564,C836.

ECO222606 (5/26/16)

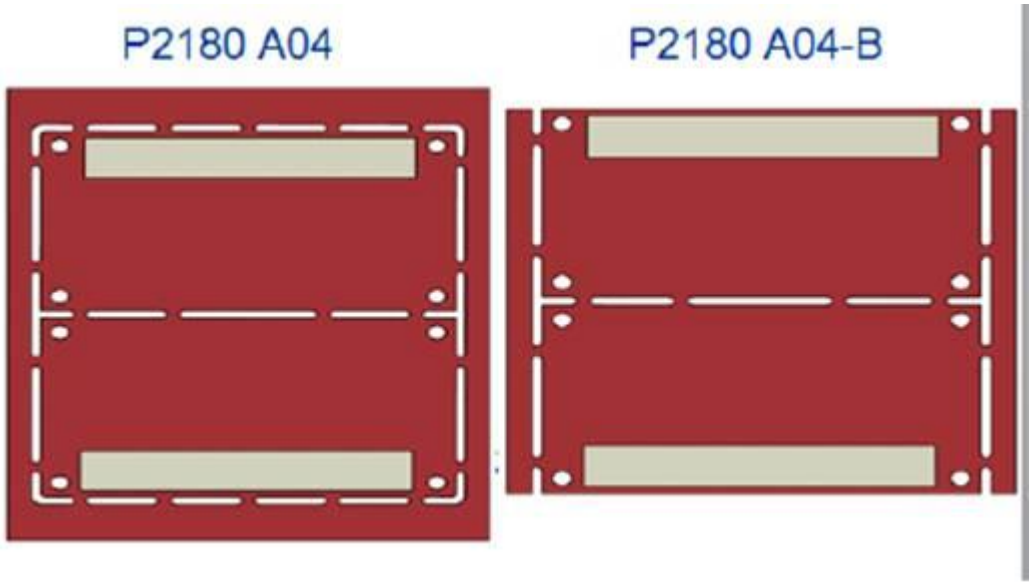
28. Added 032-0653-000 as a second alternate to 032-0564-000.
29. Changed the Find Number for 032-0857-000 from 550 to 505.

ECO222878 (6/2/16):

30. P-Release for 685 SBOM.

P2180 Fab 4 Layout Change History

The A04 is exactly the same electrical BOM and PCB design as the A03, it is just the panelization that changes as shown below


P2180 A04
P2180 A04-B

Detail P2180 Fab 4 Schematic Change History

Revision 1: 12/17/15

1. Released latest P2180-A04 schematic cloned using P2180-A03 Rev 11 schematic.

Revision 2: 12/17/15 (Missed to update the schematic for the unconditional power down sequence)

5. Page 44:
   c. Replaced U503 TPS54335DRCT, NVPN 316-0420-000 to TPS54335ADRCT, NVPN 316-0460-000
   d. Replaced R976, R977 from 10 ohm 5% 0805 to 20 ohm 5% 0805, NVPN 195-1948-000Page 48:
6. Page 48: Removed R984, R985 10 ohm 5% 0805. Added R818 0 ohm 0201.

Revision 3: 3/9/16

1. Updated P2180-A04 schematic as listed changes of X5R caps to X6S, X7S or X7R caps as per internal document "P2180-A04_ X5R Alternatives.xlsx"

Revision 4: 4/4/16

1. Missed to replace C574, C106 1uF 6.3V 10% X5R 0402 to 1uF 6.3V 10% X7R 0402, NVPN 032-078r3-000.
   BOM was updated, but missed to update in the schematic.

Revision 5: 4/28/16 (Changed in the Variant Editor at item 1-4)

1. Changed Y1, 32.768KHz primary Epson FC-12M32.7680KA-A3 (085-0174-000) to alternate and alternate TXC 9H03270062 (085-0293-000) to primary.
2. Changed Y2, 38.4MHz primary Epson Q24FA20H0028100 (085-0180-000) to alternate and alternate TXC 8Z38470012 (085-0294-000) to primary.
3. Changed Y4 37.4MHz primary Siward XTL901100-B63-172 (085-0203-000) to alternate and alternate Siward XTL901190-N64-145 (085-0303-000) to primary.
4. Changed J1 NVPN 080-1277-000 (Samtec PN: REF-186137-01) to NVPN 080-1337-000 (Samtec PN: REF-186137-03).
5. Changed C111, C115 from 22pF 5% 0201 to 27pF 5% 0201, NVPN 035-0257-000.

Revision 6: 5/13/16 (Changed in the Variant Editor)

1. Released Added alt NVPN 032-0810-000 at C48 which has primary NVPN 032-0564-000.
2. Changed LB25 from 0 ohm 0201, NVPN 195-1636-000 to 0 ohm 0402, NVPN 195-2655-000 because of mismatching 0402 PAD