International

Hardware Specification

ConnectCore 9W

NS9360

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Revision History

Revision	Date	Section	Change
1			Initial Release

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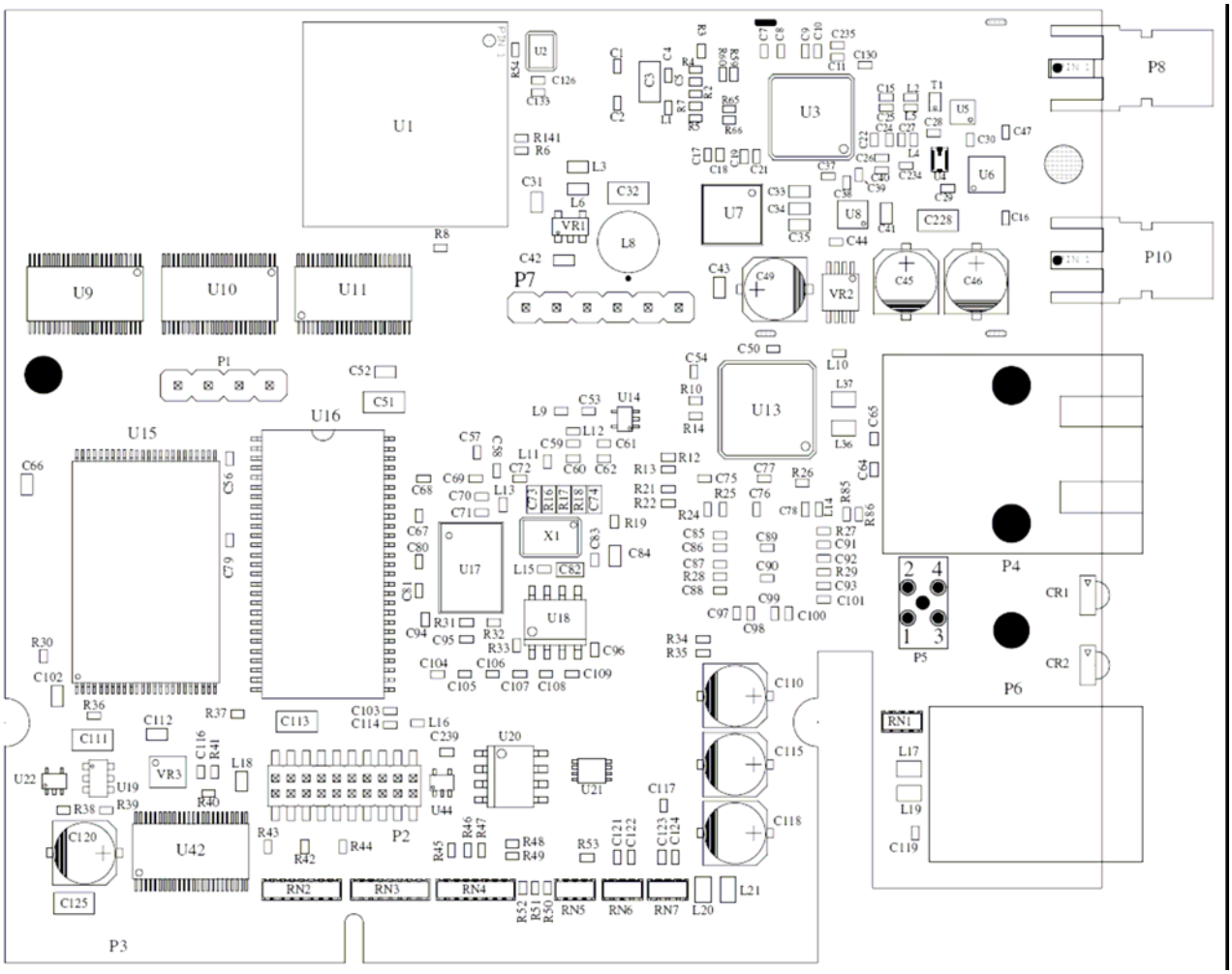


Figure 1 CC9W -- Top View

1.0 Related Documents

Digi Schematic 30006471-02 REV A
Digi – 16050802 NetSilicon NS9360 Hardware User's Manual
Digi 16050798 ISC 1893BKILF (3.3-V 10Base-T/100Base Ethernet PHY) Hardware User's Manual
Digi 42000811M29DW323DB 70ns (2M x 16) Flash Data Sheet (48 pin TBGA)
Digi 16050482 Micron MT48LC4M16A2 (4M x 16 bit) SDRAM Memory Data Sheet (54 pin TSOP)
Digi 16050830 TUSB2046BI 4-Port USB HUB Data Sheet (32 pin LQFP)
NetSilicon NS9360 Programmers Reference Manual
Ubec uw 2453 data sheet

2.0 Overview

This document contains the hardware specification for the Digi Connect Core 9W 10/100baseT Ethernet to serial/SPI or USB product.

3.0 Architecture

The Digi Connect Core 9W is an intelligent communication bridge between a 10/100 Ethernet port. a serial/SPI port, 4 USB ports, and a 802.11b/g radio. The Digi Connect Core 9W features:

NetSilicon NS9360 Communication controller

NOR Flash Memory (16M x 16 Bit max)

NAND Flash Memory (64/128Mbyte)

SDRAM (2x 16M x 16 Bit max)

4 port USB interface

4 serial port

Serial data rates up to: 230Kb/s Async in either mode.

10/100 Ethernet auto-negotiation

802.11 b/g radio

Input Voltage: 3.3 VDC, 5V for use with external peripheral USB devices only.

4.0 Block Diagram

Figure 1.0 shows a functional block diagram. The following sections describe each block separately.

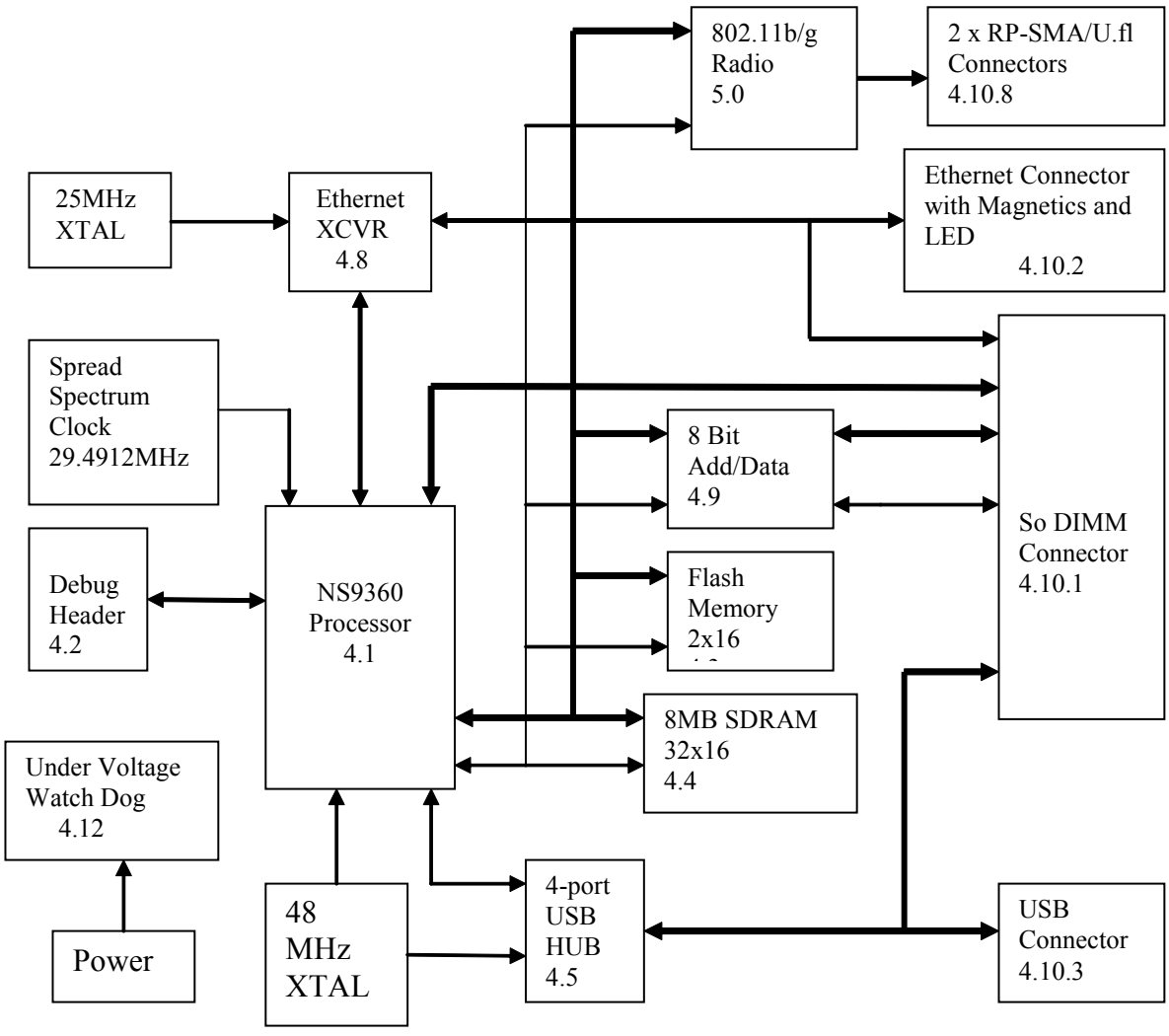


Figure 2 Connect Core 9W Block Diagram

4.1 Net Silicon NS9360 ARM9TDMI Controller

The NS9360 can support almost any networking scenario, and includes a 10/100 BaseT Ethernet MAC, USB ports, flexible LCD controller, I2C port, 1284 parallel peripheral port and multiple independent serial ports (which can run in UART, HDLC, or SPI mode).
The CPU is an ARM926EJ-S core (ARM9) 32-bit RISC processor core with a rich complement of support peripherals and memory controllers, including:
Glueless connection to different types of memory for example: flash, SDRAM, EEPROM, and others.
Various DMA channels for peripheral bus and external peripheral support
Up to 72 shared general-purpose I/O (GPIO) pins
NET+ARM is the hardware foundation of the NET+Works family of integrated hardware and software solutions for device networking. These comprehensive platforms include drivers, popular operating systems, networking software, development tools, APIs, and complete development boards.
All user signals that drive or load NS9360 GPIO pins must be placed in a high impedance state when ever the /UBUFFEN (SO-DINN connector pin 8) is high. Driving or Loading the NS9360 GPIO pins during power up or re-boot can cause either damage to the NS9360 or mis-configure it at boot time. /UBUFFEN will be set high (inactive) by the power dropping to <2.93V or whenever RS-DONE goes low due to hard, soft, or watch dog resets. /UBEFFEN is enabled (goes low) when the software toggles io66 (yellow led signal) hi for >5uS then low for >20nS. these times can be any length longer beyond the 5uS and 20nS minimum requirement and multiple toggling has no effect after the first toggle.

4.1.1 Processor External Memory Map

The NS9360 has up to 8 external buss chip selects; /CS0-/CS3 are driven by the dynamic memory controller and S_CS0-S_CS3 can be programmed to be active low or active high and are driven by the static memory controller. Each chip select can be mapped into the 32 bit memory space with a minimum addressing size of 4KBytes and a maximum addressing size of 4GBytes.

ConnectCore 9W Memory Map

Description	Address	Length
SDRAM memory (CS0	0x000 0000	16MByte (expandable to 128Mbytes)
SPI boot errata (CS1)	0x????	tests for proper SPI boot operation (SPI boot errata)
User 8 bit data buss (/S_CS0)	0x????	1KBytes (D0-D7,A0-A7) -- repeats in 4KByte min space
Flash memory (/S_CS1)	0x500 0000	16Mbyte NOR or 128Mbyte NAND
802.11 FPGA data (/S_CS2)	0x????	1Kbytes (A0-A7+A20) -- repeats in 4KByte min space
FPGA program strobe (/S_CS3)	0x????	strobes FPGA "PROG" pin -- repeats in 4KByte min space

4.1.2 ID Strapping Pins

The NS9360 has 8 populated resistors which can be used to identify the ConnectCore 9W product ID. Eight data lines have pull up/down resistors on them, specifically D24-31.

4.2 NS9360 JTAG/BDM Port

The NS9360 provides full support for 1149.1 JTAG boundary scan testing. (The NS9360BSDL file is available at www.netsilicon.com.) All NS9360 pins can be controlled using the JTAG interface port. The JTAG interface provides access to the ARM926EJ-S debug module when the appropriate combination of PLLTST_, BISTEN_, and SCANEN_ are selected. PLLTST, BISTEN, and SCANEN are three pins used to configure the NS9360 upon boot-up to work with either a PLL or Oscillator, and with JTAG mode enable or disabled. The JTAG signals are made available on a 20 pin header, P2

JTAG HEADER P2 PINOUT

Pin Number	Function		Pin Number	Function
1	+3.3V	2	+3.3V	
3	/TRST	4	GND	
5	TDI	6	GND	
7	TMS	7	GND	
9	TCK	8	GND	
11	RCLK	9	GND	
13	TDO	14	GND	
15	SRST	16	GND	
17	NC	18	GND	
19*	/BISTEN	20	GND	

* Pin 19 = low = boundary scan mode (default mode) , pin 19 = high = debug mode. The debugger adapter jumpers pin 19 high for the debug mode.

4.3 Flash

There are two ways to boot the module: NOR flash memory and serial SPI flash memory. The boot method is selected by either pulling the NS9360 RS_DONE signal low (R13 populated) or allowing RS_DONE to float (R13 not populated) at power up or hard reset. If RS_DONE is detected as a low, the serial SPI flash is used as the booting memory. In this mode, the NS9360 reads the setup code in the Serial SPI flash and uses this code to configure the memory controller to read the NAND flash memory. The NAND flash contains the actual boot loader and operating system. If RS_DONE is detected as a high, the NOR flash is used to boot the module. In this mode, the NS9360 reads the code stored in the NOR flash memory starting at address 0. The NOR flash contains the boot loader and compressed operating system. The manufacturing header (J1 pin 1) can apply 12v to the NOR flash RESET pin to unlock the protected areas of the flash memory. This allows the memory to be reprogrammed in circuit.
Both boot methods load the operating system into the SDRAM for execution.

Manufacturing header P1 pinouts

Pin Number	Function
1	RB apply +12v to unlock locked sectors
2	MFGO
3	MFGI
4	GND

4.4 SDRAM Memory

The memory size of 16MByte is currently supported and could be expanded up to 128 MBytes. The 32-bit byte/word accessible memory is implemented with two 1M x16 x 4 banks SDRAM. The SDRAM uses an auto refresh command every 15.625µs that is analogous to "CAS before RAS" in conventional DRAM. See NS9360 manual and SDRAM specification for additional details.

4.5 USB Interface

The Digi Connect Core 9W provides a means to transmit data via USB port. A 4-port HUB is used on the board with capabilities to be connected to up to 4 USB devices. Currently two of the USB channels connect to 2 external USB devices through a dual type A (host) connector (P6) and the remaining two channel are available at the user SO-DIMM connector. P6 also will provide 5V@.5A for each of the 2 ports. P6 foot print can be populated as a single type A connector. Population options allow for all 4 USB ports to brought out through the SO-DIMM connector (no P6 population) or the 4 port hub can be removed and the native NS9360 USB channel can be brought to P6 or to the SO-DIMM connector. The Digi Connect Core 9W supports full speed devices, which are capable of communicating at a speed of 12 Megabits per second.

4.7 Serial Line Interface

The Digi Connect Core 9W product has 4 serial interface port supporting EIA 232 and SPI. The ports are capable of data rates of 230Kbits/sec (all modes) and supports full modem control when in the EIA232 mode. The user access to the signals is provided through the 144 pin So DIMM edge connector.

The Digi Connect Core 9W provides 3.3V on all outputs and accepts 3.3V levels on all inputs to the Digi Connect Core 9W as well. The Connect Core 9W does not provide, nor tolerates 5V levels.

The Digi Connect Core 9W also provides a means of transmitting/receiving Serial Peripheral Interface (SPI) data. For this method of data transfer only 4 signals are used. These 4 signals are described in the connectors section.

4.8 Ethernet Interface

The Digi Connect Core 9W hardware architecture supports an Integrated Circuit Systems, ICS1893BKILF 3.3-V 10Base-T/100Base Ethernet PHY. The ICS1893BKILF is a high-performance Local Area Network Transceiver (PHY). It implements the CSMA/CD access method and supports existing IEEE 802.3 standards 10Base-T and 100Base-T. It connects to the NS9360 using the glue-less MII interface. The device can communicate over 100 meters of category 5 cable in 100BaseTX and 100 meters of category 5 cable in 10BaseT (distance depends on signal loss and impedance match). The interface provides transformer isolation integrated in the RJ45 Connector, P4. The Ethernet Link and Activity status LED are driven by the ICS1893BKILF. The Ethernet RX and TX signals are pinned out at connector P4 (see section **4.10** for pin outs).

During the auto-negotiation process, the ICS1893BF exchanges capability data with its remote link partner by using a pre-defined Link Code Word. The Link Code Word is embedded in the Fast Link Pulses exchanged between PHYs when the ICS1893BF has its Auto-Negotiation sub-layer enabled. The value of the Link Control Word is established based on the value of the bits in the Auto-Negotiation Advertisement Register (register 4 [0x04]).
See ICS1893BFData Sheet for more details.

4.9 Use 8 bit Data Buss

The Connect Core 9W provides the user access to the NS9360's data buss through an buffered 8 bit address/data buss. This user 8 bit buss is mapped into the NS 9360's chip select 0 (CS0) memory space. It is recommended that the accesses to the 8 bit buss be kept slow to allow for buss delays and settling time. The 8 bit data buss uses NS 9360 A0-A7 and D0-D7 and is available on the user 144 pin SO-DIMM connector P3. the signals provided are:/ IOCS (active low chip select), /IOOE (active low output enable), /IOWE (active low write enable), IOD0-IOD7 (8 bit data), and IOA0-IOA7 (8 bit address). Accesses are typical SRAM accesses with /IOCS and IOOE going low for read cycles into the Connect Core 9W. Data is strobed into the NS9360 on the rising edge of the/ IOOE. Write cycles drive /IOCS and /IOWE low, data is written on the rising edge of the /IOWE. The specific timing can be seen in the NS9360 hardware manual.

4.10 Connectors

4.10.1 So DIMM, 144 pin Connector P3

Connectors P3 is So DIMM, 144 pin edge connector. This connector provides the user connection to the Digi Connect Core 9W's serial, Ethernet, USB, I2C , LCD interfaces as well as a +3.3V, +5V power and ground connections for the board. The pin outs for P3 is given below.

DIMM Pin	Signal	UART	SPI	I2C	USB	LCD	IEEE 1284	PWM	Timer	IRQ	Bootstrap	Notes
1	GND											
2	GND											
3	+3.3V											
4	+3.3V											
5	+3.3V											
6	+3.3V											
7	/Wakeup											Wake from sleep mode
8	/BUFFENR											Output (Active LOW); Hold user buffers off during power up/down until signal active
9	IOData(0)											User 8 bit data buss
10	IOData(1)											"
11	IOData(2)											"
12	IOData(3)											"
13	IOData(4)											"
14	IOData(5)											"
15	IOData(6)											"
16	IOData(7)											"
17	IOAdd(0)											User 8 bit address buss
18	IOAdd(1)											"
19	GND											
20	GND											
21	IOAdd(2)											User 8 bit address buss
22	Reserved											No connect MFGI
23	IOAdd(3)											User 8 bit address buss
24	GPIO[71]			SDA								Output Drive: 8mA SDA: Primary on GPIO[35]
25	IOAdd(4)											User 8 bit address buss
26	GPIO[70]			SCL								Output Drive: 8mA SCL: Primary on GPIO[34]
27	IOAdd(5)											User 8 bit address buss
28	GPIO[69]									IRQ1		Output Drive: 8mA IRQ1:

DIMM Pin	Signal	UART	SPI	I2C	USB	LCD	IEEE 1284	PWM	Timer	IRQ	Bootstrap	Notes
												Primary on GPIO[7]
29	GND											
30	GND											
31	GPIO[27]	DCD D	ENBL D			CLD3			TIMER4			
32	Reserved											No connect
33	GPIO[26]	RI D	CLK D			CLD2			TIMER3			
34	GPIO[67]											MFGO Output Drive: 8mA
35	GPIO[25]	DSR D				CLD1						
36	GPIO[66]											Output Drive: 8mA
37	GPIO[24]	DTR D				CLD0					CS1_MSB	
38	GPIO[23]	DCD C	ENBL C			CLLE						
39	GND											
40	GND											
41	GPIO[47]	CTS D			RXD-		PINIT					USB: RXD- only used for unidirectional PHY
42	GPIO[22]	RI C	CLK C			CLAC						
43	GPIO[46]	RTS D			RXD+		PAFD					USB: RXD+ only used for unidirectional PHY
44	GPIO[21]	DSR C				CLFP						
45	GPIO[45]	RXD D	DIN D		RCV		PSTB					
46	GPIO[20]	DTR C				CLCP					CS1_LSB	Output Drive: 8mA
47	GPIO[44]	TXD D	DOUT D		OE		PSELO				Endian	Endian: Pull down for Big Endian
48	GPIO[43]	CTS C			DATA-		PDIR					
49	GND											
50	GND											
51	GPIO[38]					CLD14	PD7	PWM2				PWM2: Duplicate on GPIO[13]
52	GPIO[42]	RTS C			DATA+							
53	GPIO[36]					CLD12	PD5	PWM0				PWM0: Duplicate on GPIO[10]
54	GPIO[41]	RXD	DIN C			CLD17						

DIMM Pin	Signal	UART	SPI	I2C	USB	LCD	IEEE 1284	PWM	Timer	IRQ	Bootstrap	Notes
		C										
55	GPIO[34]			SCL		CLD10	PD3					I2C: Duplicate on GPIO[70] CLD10: Primary on GPIO[30]
56	GPIO[40]	TXD C	DOUT C			CLD16				IRQ3		IRQ3: Duplicate on GPIO[18]
57	GPIO[32]					CLD8	PD1			IRQ2		CLD8: Duplicate on GPIO[28] IRQ2: Duplicate on GPIO[11]
58	GPIO[39]					CLD15	PD8	PWM3				PWM3: Duplicate on GPIO[14]
59	GND											
60	GND											
61	GND											
62	GND											
63	GPIO[30]					CLD6 (CLD10) [1]			TIMER6			CLD10: Primary on GPIO[34]
64	GPIO[37]					CLD13	PD6	PWM1				PWM1: Duplicate on GPIO[12]
65	GPIO[28]					CLD4 (CLD8)[1]				IRQ1		CLD8: Primary on GPIO[32] IRQ1: Primary on GPIO[7]
66	GPIO[35]			SDA		CLD11	PD4					SDA: Duplicate on GPIO[71] CLD11: Primary on GPIO[31]
67	GPIO[15]	DCD A	ENBL A			LCDCLKI			TIMER2			
68	GPIO[33]					CLD9	PD2					CLD9: Duplicate on GPIO[29]
69	GPIO[14]	RI A	CLK A					PWM3	TIMER1			TIMER1: Duplicate on GPIO[0] PWM3: Primary on GPIO[39]
70	GPIO[31]					CLD7 (CLD11) [1]			TIMER7			CLD11: Primary on

DIMM Pin	Signal	UART	SPI	I2C	USB	LCD	IEEE 1284	PWM	Timer	IRQ	Bootstrap	Notes
												GPIO[35] TIMER7: Duplicate on GPIO[6]
71	GND											
72	GND											
73	GPIO[13]	DSR A						PWM2		IRQ0		IRQ0: Primary on GPIO[1] PWM2: Primary on GPIO[38]
74	GPIO[29]					CLD5 (CLD9) [1]			TIMER5			CLD9: Primary on GPIO[33]
75	GPIO[12]	DTR A						PWM1			ND3	PWM1: Primary on GPIO[37]
76	GPIO[07]	DCD B	ENBL B							IRQ1		IRQ1: Duplicate on GPIO[28]
77	GPIO[11]	CTS A							TIMER0	IRQ2		TIMER0: Primary on GPIO[2] IRQ2: Primary on GPIO[32]
78	GPIO[06]	RI B	CLK B				PFAULT		TIMER7			PFAULT:: Primary on GPIO[16] TIMER7: Primary on GPIO[31]
79	GPIO[10]	RTS A						PWM0			ND2	PWM0: Primary on GPIO[36]
80	GPIO[05]	DSR B					PERR					
81	GND											
82	GND											
83	GPIO[09]	RXD A	DIN A									
84	GPIO[04]	DTR B					PBUSY				ND0	
85	GPIO[08]	TXD A	DOUT A								ND1	
86	GPIO[03]	CTS B					PACK					
87	GPIO[19]					HSYNC					PLL_BYP	
88	GPIO[02]	RTS B							TIMER0		FS1	TIMER0: Duplicate on GPIO[11]
89	GPIO[18]					CLPOWER				IRQ3		IRQ3: Primary on

DIMM Pin	Signal	UART	SPI	I2C	USB	LCD	IEEE 1284	PWM	Timer	IRQ	Bootstrap	Notes
												GPIO[40]
90	GPIO[01]	RXD B	DIN B							IRQ0		IRQ0: Duplicate on GPIO[13]
91	/IOOE											User 8 bit data buss /OE
92	GPIO[00]	TXD B	DOUT B						TIMER1		FS0	TIMER1: Primary on GPIO[14]
93	GND											
94	GND											
95	/IOWE											User 8 bit data buss/WE
96	GPIO[49]				SPD		PLH				CS_POL	
97	/IOCS											User 8 bit data buss /CS
98	GPIO[48]				SUSP		PSELI					
99	Reserved											Ethernet TXB+R[3]
100	Reserved											Ethernet TXA+R[3]
101	GND											
102	GND											
103	Reserved											Ethernet TXB-R[3]
104	Reserved											Ethernet TXA-R[3]
105	/ MODRST											Hardware reset (Input; Active LOW; minimum pulse width 10µs)
106	Reserved											/ACTIVITY LED[3]
107	Reserved											BOOTMUX
108	Reserved											LINK LED[3]
109	GPIO[16]				/OVRH		PFAULT	PWM0				/OVRH: USB Overcurrent[2] PFAULT: Primary on GPIO[6] PWM0: Duplicate on GPIO[10]
110	IOAdd(6)											User 8 bit address buss
111	GPIO[17]				/ PONH							/PONH: USB Power-On[2]
112	IOAdd(7)											User 8 bit address buss

DIMM Pin	Signal	UART	SPI	I2C	USB	LCD	IEEE 1284	PWM	Timer	IRQ	Bootstrap	Notes
113	/OVR3											USB Port 3 Overcurrent[3]
114	/OVR4											USB Port 4 Overcurrent[3]
115	/PON3											USB Port 3 Power-On[3]
116	/PON4											USB Port 4 Power-On[3]
117	/OVR1											USB Port 1 Overcurrent[3]
118	/OVR2											USB Port 2 Overcurrent[3]
119	/PON1											USB Port 1 Power-On [3]
120	/PON2											USB Port 2 Power-On[3]
121	GND											
122	GND											
123	DM4											USB Port 4 Data (-)[3]
124	DP4											USB Port 4 Data (+)[3]
125	GND											
126	GND											
127	DM3											USB Port 3 Data (-)[3]
128	DP3											USB Port 3 Data (+)[3]
129	GND											
130	GND											
131	DM2											USB Port 2 Data (-)[3]
132	DP2											USB Port 2 Data (+)[3]
133	GND											
134	GND											
135	DM1											USB Port 1 Data (-)[3]
136	DP1											USB Port 1 Data (+)[3]
137	GND											
138	GND											
139	+5V											Power to USB, if used[4]
140	+5V											Power to USB, if used[4]
141	+5V											Power to USB, if used[4]
142	+5V											Power to USB, if used[4]
143	GND											
144	GND											

[1] Duplicate
[2] Available as GPIO on module w/on-board USB and module w/Ethernet-only if USB is not used
[3] Reserved for future use; no connect
[4] Module w/on-board USB

Some signals are muxed to two different GPIO pins, to maximize the number of possible applications. The primary/duplicate signals are marked as such in the Notes column of the table with a corresponding reference to each other. Selecting the primary GPIO pin and the duplicate GPIO pin for the same function is not recommended.

Please refer to the NS930 Hardware Reference for detailed information about pinouts and GPIO mux related options.

4.10.2 Ethernet 10/100 BaseT Connector P4

P4 serves as the Ethernet 10/100BaseT interface for the Digi Connect Core 9W. It is an eight position RJ-45 meeting the requirements of ISO 8877. The signal pinouts for P4 are as follows:

Signal Name	Mnemonic	Pin Number
Transmit Data+	TXA+	1
Transmit Data-	TXA-	2
Receive Data+	TXB+	3
Mid Span POE+	DC+	4
Mid Span POE+	DC+	5
Receive Data-	TXB-	6
Mid Span POE-	DC-	7
Mid Span POE-	DC-	8

Note that End Span POE(+) power is derived from the Tx line side transformer winding center tap and the End Span POE(-) power is derived from the Rx line side transformer winding center tap.

4.10.3 USB Connector P6

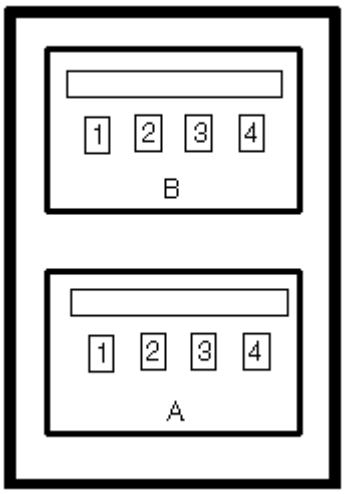


Figure 3 Dual USB connector P6

Pin Number	Function
A1	A+5V
A2	AD-
A3	AD+
A4	AGND
B1	B+5V
B2	BD-
B3	BD+
B4	BGND

4.10.4 JTAG Header P2

JTAG HEADER P2 PINOUT

Pin Number	Function	Pin Number	Function
1	+3.3V	2	+3.3V
3	/TRST	4	GND
5	TDI	6	GND
7	TMS	7	GND
9	TCK	8	GND
11	RCLK	9	GND
13	TDO	14	GND
15	SRST	16	GND
17	NC	18	GND
19*	/BISTEN	20	GND

* Pin 19 = low = boundary scan mode (default mode) , pin 19 = high = debug mode. The debugger adapter jumpers pin 19 high for the debug mode.

4.10.5 Manufacturing header P1

Manufacturing header P1 pinouts

Pin Number	Function
5	RB apply +12v to unlock locked sectors
6	MFGO
7	MFGI
8	GND

4.10.6 POE Pass Through Connector P5

POE Pass Through connector P5 pinouts

Pin number	Function
1	End Span (+)
2	Mid Span(-)
3	End Span(-)
4	Mid Span(+)

End Span(+) connects to the P4 Tx transformer line side winding center tap, End Span(-) connects to P4 Rx transformer winding center tap.
Mid Span(+) connects to pair 4/5, Mid Span(-) connects to pair 7/8.

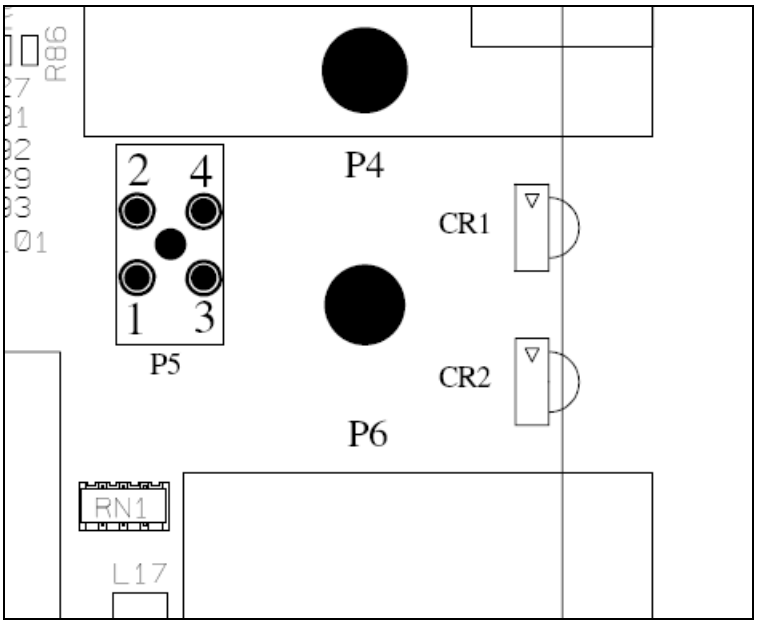


Figure 4 user POE Pass Through Connector P5 -- Top View

4.10.7 FPGA JTAG Header P7

FPGA JTAG header P7 pinouts

Pin Number	Function
1	+2.5V
2	GND
3	TCK
4	TDO
5	TDI

6 TMS

4.10.8 Antenna Connectors P8 and P10

The ConnectCore 9W uses two reverse polarity SMA (RP-SMA) antenna connectors. These connectors are designed with a male center pin which prevents a standard SMA connector from being mated to the ConnectCore 9W.

Antenna connectors P8 and P10 are reverse SMA connectors

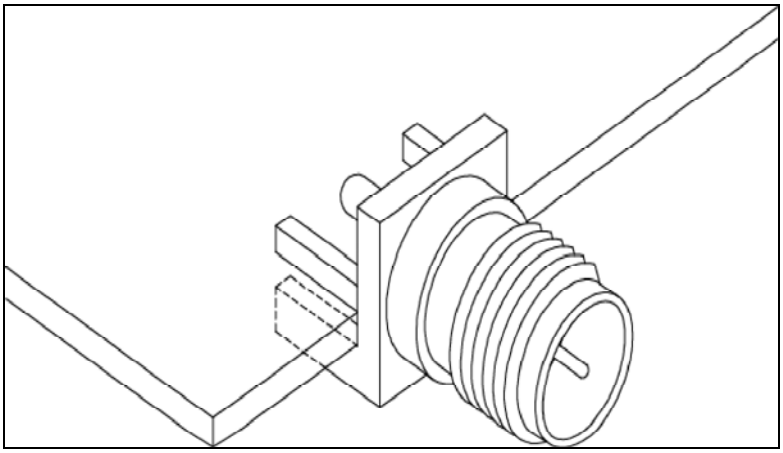


Figure 5 RP-SMA Antenna Connector

4.12 Under Voltage Supervisor

An ADM811S Under voltage lock out supervisor is provided to reset the Digi Connect Core 9W at power on, user triggered hard reset or any time the power browns out. If the +3.3 volt power supply dips to < 2.93 volts, the ADM811S will assert and hold the reset signal. The ADM811S asserts the hard reset signal which causes a total system reset. A manual reset input is wired to the ADM811S from the SoDIMM connector. (P3-pin 105).

4.14 LEDs

4.14.1 Power On/Diagnostic LED – Green (Bottom Left)

A power on/diagnostic LED is provided and is located between the Ethernet connector P4 and USB connector P6. This Green LED is lit any time the unit is powered

4.14.2 Ethernet Link and Activity Status – GREEN and YELLOW

A green Ethernet link status LED is lit when a good Ethernet link has been established. This LED is paired with the Ethernet Receive Activity LED and both are visible on the Ethernet connector, P4. The LED are controlled by the PHY and can not be controlled by the user. However, both LEDs are accessible to the user through the SoDimm connector when no-ETHERNET board module is used.

***Note- For all cases of the LEDs listed above (with the exception of the Ethernet Link Status) a "0" written to the appropriate GPIO pin where the LED resides will cause the LED to light.**

4.14.3 LED U15, NS9360

Signal Name	Mnemonic	Pin Number
User defined Yellow LED	IO66	H19
User/Manufacturing defined Green LED	IO67_MFGO	E18

4.15 Power Over Ethernet (POE)

PoE 4-pin header, P5
802.3af PoE (Power over Ethernet) pass-through socket: AMP, HDR, STR Dual Row p/n: 103186-2 and 103240-2
P5 provides a POE pass through from P4 (Ethernet RJ45 connector) to the user.

POE Pass Through connector P5 pinouts

Pin number	Function
1	End Span (+)
2	Mid Span(-)
3	End Span(-)
4	Mid Span(+)

End Span(+) connects to the P4 Tx transformer line side winding center tap, End Span(-) connects to P4 Rx transformer winding center tap.
Mid Span(+) connects to pair 4/5, Mid Span(-) connects to pair 7/8.

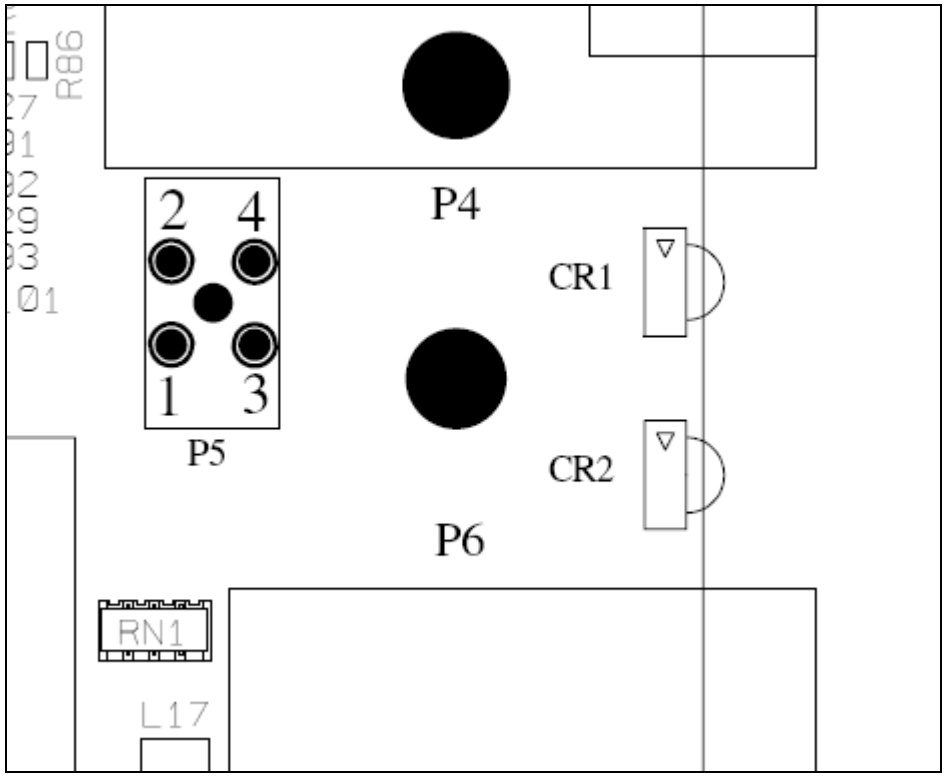


Figure 6 P5 user POE Pass Through Connector --- Top View

5.0 802.11b/g Radio

The Digi Connect Core 9W contains a full featured 802.11b/g WiFi radio transceiver based on a Ubec uw2453 802.11b/g zero IF (direct conversion) transceiver IC.

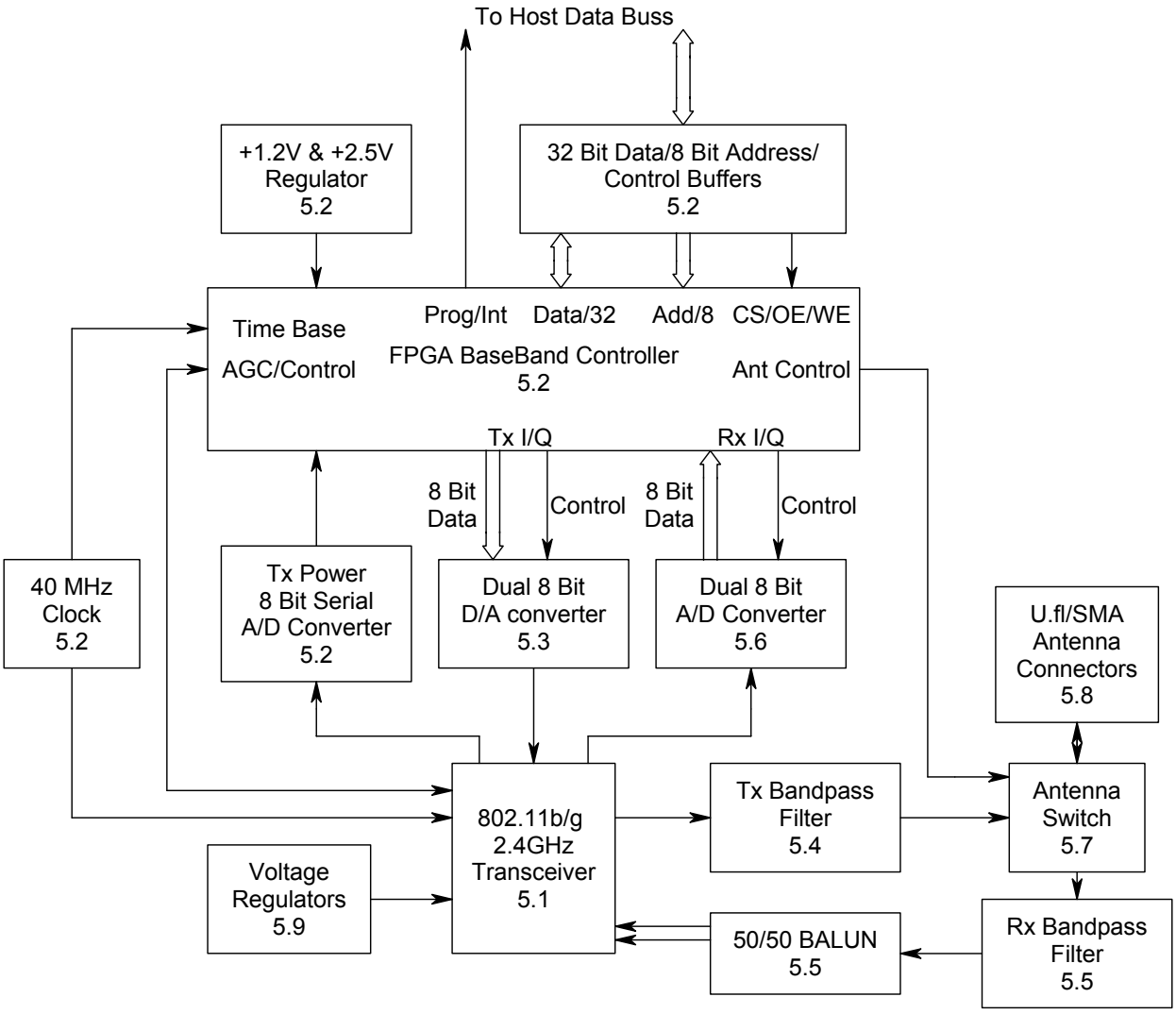


Figure 7 802.11b/g Transceiver Block Diagram

5.1 Ubec uw2453 802.11b/g radio transceiver

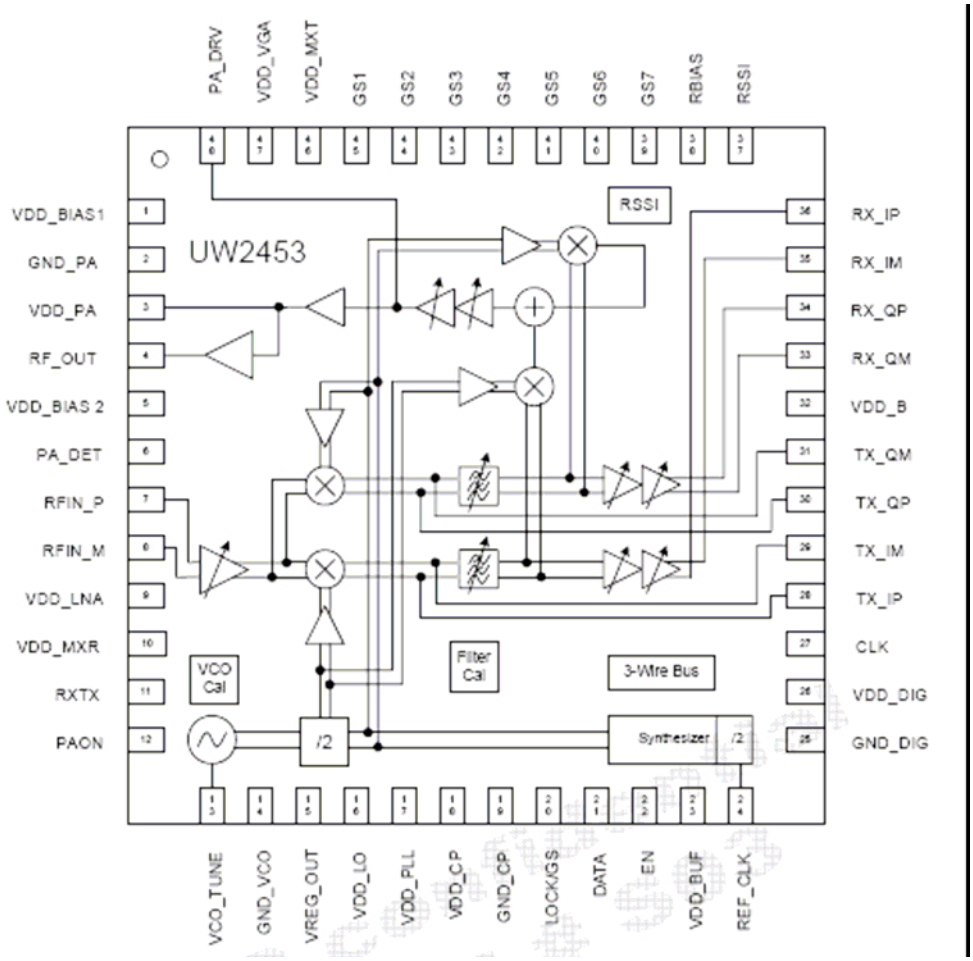


Figure 8 Ubec uw2453 802.11b/g radio block diagram

The UW2453 (U3) receiver consists of a LNA, a pair of down-conversion mixers, I&Q channel filters, I&Q variable gain amplifiers (VGA), RSSI and programmable DC blocking cancellation blocks. The LO generation circuits (VCO, PLL and buffers) are shared with the receiver and transmitter. The LNA features a differential input for high performance. An external balum matching network is required. The LNA has 2 stepped gains. Along with one stepped gain inside the channel filter, three stepped gains are achieved in the receive chain from the LNA to the channel filters and they are controlled by two digital I/O pins, GS1 and GS2. The additional receive gain is realized by the RX VGA. The RX VGA has a gain resolution of 2 dB and the gain is set by Pins GS3~GS7. Pin GS7 sets a two dB change. Since the RX gain is set by the digital I/O pins, fast gain settling is realized. The RX gain can also be set by the regular or 3-wire bus in addition to the pins GS1~GS7.

The UW2453 features a patented DC blocking circuit and the DC blocking circuit settles the receive DC offset for less than 10 mV at the RX outputs within 400 ns for any gain size change. To have a better control over the DC settling process, the settling time is programmable.

To set a proper RX gain without a prior knowledge of the received signal strength, the UW2453 only needs a maximum of three times of gain adjustment with the help of the high dynamic range RSSI output. When the input signal is below –41 dBm, only two times of gain adjustment is required thanks to the high dynamic range of the RSSI circuit.

The UW2453 also supports antenna diversity. However, antenna diversity requires a total settling time equivalent to a maximum of four times of gain adjustment. That means if in no diversity case, the worst total gain settling time is 2.4 us, it is 3.2 us with diversity.

Before the receiver properly demodulates the signal, filter and VCO calibration are needed. The filter and VCO calibration finds the correct filter corner frequency and VCO sub-band respectively, amid process, supply and temperature variation. The VCO and filter calibration are self-contained and no support from DSP side is

required.
One unique feature is the receiver and transmitter share a pair of I&Q channel filter in order to minimize the die size and cost. However, the filter bandwidth in RX and TX mode can be independently programmed, thanks to the innovative design.
The switch between receive and transmit is controlled by Pin RXTX in the RXTX_EN chip mode. This pin also determines the filter bandwidth in conjunction with other register settings.
The transmitter features direct conversion architecture with +18 dBm output power with OFDM signal and +21 dBm output power with CCK signal with the integrated power amplifier for the UW2453. The output power adjustment range is 16 dB in one dB step. Pins GS1 to GS4 are used to set the TX front end gain (16 dB range). Like the receiver, the TX front end gain can also be programmed by the regular 3-wire bus.
The LO generation scheme of the UW2453 employs a divided by 2 scheme to minimize pulling effect and to get a better phase imbalance. The VCO operates at the twice of the channel frequency. Additional feature is the ΣΔ frequency synthesizer having a fine frequency resolution. The wider loop bandwidth allowed by the ΣΔ frequency synthesizer is also helpful in tracking the VCO pulling and pushing effect. The VCO has a switched band design such that low phase noise, low VCO gain factor and high stability are realized. The advanced VCO calibration scheme makes it possible that the carrier frequency is always in the middle of one of the VCO bands. After reprogramming the channel frequency, a VCO calibration action is required. The PLL charge pump current is programmable so that the VCO gain variation for different bands can be compensated.
The UW2453 has a power-up reset to set the registers to their default values. There is also a reset mode to allow the 3-wire bus to reset the IC at any time. After a reset, the UW2453 automatically enters the sleep mode.
Pin 20 (LOCK/GS) is a special input/output pin. It can be programmed as the PLL lock detector output or as an enable pin for Pin GS1~GS7. If Pin 20 is configured as the GS1~GS7 enable pin, when Pin 20=1, any change on GS1~GS7 will cause RX or TX gain change. When Pin 20=0, any change on GS1~GS7 has no effect on RX/TX gain and the receiver or transmitter uses the last GS1~GS7 values when Pin 20=1. That is a high to low transition will latch the GS1~GS7 value. This feature is useful so that multiple of the UW2453 is used in a MIMO configuration without doubling or tripling the parallel control pins.
The 1, 2, 5.5, and 11 Mbit/s data rates use DSSS and CCK types of modulation. The 6, 9, 12, 24, 36, and 54 Mbit/s data rates use OFDM modulation.

5.2 Base Band Controller FPGA

The base band controller controls the basic radio functions such as receiver agc, receive/transmit switching, antenna switching, channel selection, transmitter I/Q data generation and receiver I/Q data demodulation. The base band controller is implemented in a Xilinx XC3S1000 FPGA (U1) using Digi's propriety FPGA base band software. The FPGA is mapped into the NS9360's Static Chip Select 2 (S_CS2) memory space and uses 32 bit data and 8 bit address busses to pass data between itself and the NS9360. The address and data bits are buffered by U9, U10, and U11. The FPGA must be configured after every power cycle. This accomplished is by the NS9360 by way of loading configuration data from the lower 8 bits of the memory data buss into the FPGA. To configure the FPGA the NS9360 Static Chip Select 3 (/S_CS3) drives the /FPROG signal low for >300nS, waits for the FINTB signal to go high (FPGA memory cleared), loads the configuration data bytes into the FPGA on the rising edge of the /WE signal. The actual clocking of the configuration bytes into the FPGA occurs when the negative AND combination of /CS2 and /WE goes inactive (high) with the rising edge of /WE at the end of the NS9360 write cycle. This signal is fed into the FPGA's configuration clock input. A second configuration method loads the configuration data into the FPGA through the JTAG port (P7). The JTAG port uses 2.5V signaling.
The FPGA generates the transmit I/Q data as two 8 bit bytes that are muxed onto an 8 bit data buss such that they are loaded into the Tx dual digital to analog converter (ADC) (U23) on every other clock. The transfer clock runs at 40MHz so the actual I/Q bytes of Tx data are transferred at a 20MHz rate.
The receive data is converted into two 8 bit bytes by a dual Analog to digital converter (ADC) (U7) from the uw2453's (U3) Rx I/Q analog outputs. Like the transmitter data, the two converted receiver I/Q data bytes are muxed by the ADC and transferred to the FPGA on an 8 bit data buss on ever other clock. the ADC clock also runs at 40MHz so the Rx I/Q data transfer rate is at a 20MHz rate.
The FPGA monitors the magnitude of the Rx I/Q data at the beginning of a receive transaction and will adjust the uw2453 Rx gain in an effort to keep the converted Rx magnitude at ~1V. As implemented in this design, the Ubec uw2453 transceiver Rx gain is controlled by the binary value driven onto the uw453's 7 AGC control lines (AGC1-AGC7) by the FPGA.
As implemented in this design, Tx power out is adjusted by the binary value driven onto the uw2453 AGC control line AGC1-AGC4 by the FPGA.

The uw2453's internal registers are configured by the FPGA through a 3 wire write only interface which consists of an enable, clock, and I/O data signals. Register configuration data is loaded into the uw2453 when the /3WEN signal goes low and the 3WCLK signal goes high. The configuration word is 24 bits low: 4 bits of register address data and 20 bits of configuration data.
The base band functions also include the ability to switch either the Tx and Rx signals between the two antenna ports. This feature allows the base band controller pick the antenna that provides the best signal performance.
The base band controller can monitor the Tx power by way of a serial 8 bit ADC (U8). This serial 8 bit ADC converts the analog Tx power detect signal provided by the uw2453 into an 8 bit byte that can be read by the FPGA. The Tx power detect signal varies from ~.4V at a Tx power out of 5dbm to ~2v at a Tx power out of 20dbm.
All base band and u2453 timing is derived from +/- 25ppm 40MHz oscillator (U2).
The FPGA operates on three voltages: 3.3v derived directly from the system 3.3v and is used to power the I/O drivers, 2.5V regulated from the system 3.3V by VR1 and is used to power the JTAG and configuration functions, and 1.2V regulated from the system 3.3V by switching regulator VR24 and used to power the FPGA core logic.

FPGA JTAG header P7 pinouts

Pin Number	Function
7	+2.5V
8	GND
9	TCK
10	TDO
11	TDI
12	TMS

5.3 Transmit I/Q digital to analog converter AD9709 (U23)

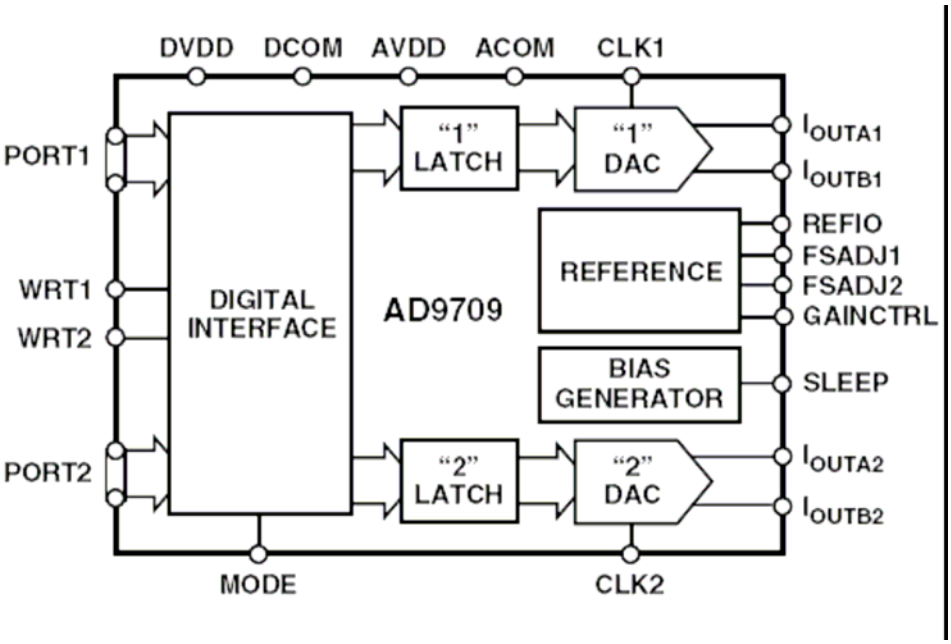


Figure 9 DAC block diagram

The Ubec uw2453 transceiver requires base band analog I and Q signals to drive the transmitter's up converter mixer. The I/Q signals are applied to the uw2453 as differential signals to keep system noise from contaminating the up conversion. The FPGA generates the transmit I/Q data as two 8 bit bytes that are muxed onto an 8 bit data buss such that they are loaded into the Tx dual digital to analog converter (ADC)

(U23) on every other clock. The transfer clock runs at 40MHz so the actual I/Q bytes of Tx data are transferred at a 20MHz rate. The timing of the DAC data transfer from the FPGA to the DAC is illustrated below.

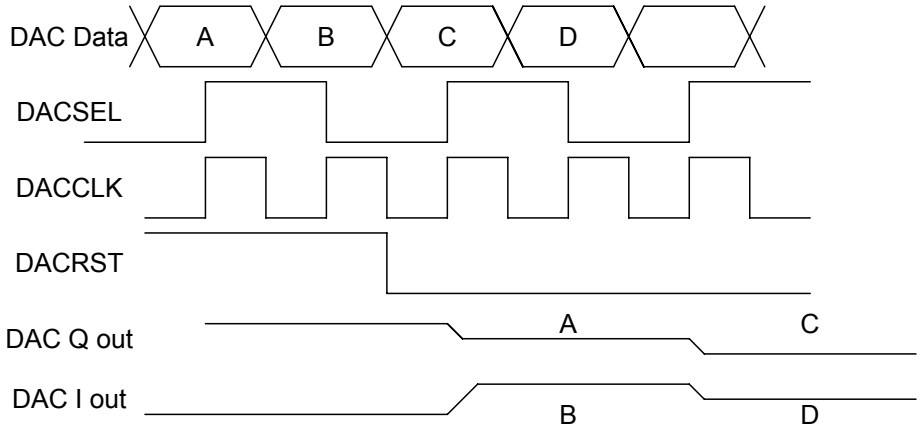


Figure 10 DAC data timing

Note that this timing is for the first bytes loaded into the DAC at the beginning of radio initialization. The first byte of the DAC data (Tx Q data) is latched into the DAC latch 1when the DACSEL goes high and the second byte of DAC data (Tx I data) is latched into the DAC latch 2 when the DACSEL goes low. The DACRST signal is used to synchronize the byte data. When DACRST is high, the data latched into DAC latches 1 and 2 is not transferred to the DAC output latches. When DACRST goes low, the next rising edge of the DACCLK will transfer the byte data from latches 1 and 2 to the output latches and to the output current sources. Once synchronized, the output will be updated every other rising edge of the DACCLK. The data loaded into each channel of the DAC is used to set on output current for that channel. The max current out is set by R2 (2.8K) to be 13.7mA. These output currents are converted to a voltage and level shifted by R5, R66, R7, R65 and R3, R59, R4, R60 and applied to the uw2453 Tx I/Q analog inputs.

5.4 Transmit out RF signal path

The Ubec uw2453 (U3) transceiver mixes the Tx I/Q analog signals with an internally generated local oscillator signal to directly convert the Tx I/Q inputs to a modulated 2.4 GHz signal that is amplified and output as a single ended 50 ohm ~20bdm RF signal on uw2453 pin 4. Power is provided for the uw2453 Tx output stage from the 3.3 V source by RF choke L4. The Tx signal is impedance matched and filtered by C22, C24, and C27 before it is applied to the ceramic 2.445GHz band pass filter (U4). The filtered Tx signal is switched between the two antenna ports by the DPDT antenna switch U6 under base band FPGA control. Capacitors C28, C29, C16, and C 47 are dc blocking coupling capacitors. All Tx RF PCB traces are 50 ohm microstrip lines.

5.5 Receive RF signal path

The received signal enters the radio by way of one of the two antenna ports. The specific antenna port is selected by the DPDT antenna switch, U6 under base band FPGA control. The Rx signal passes through a 2.445GHz SAW band pass filter (U5) to reduce out of band interference and is converted to a 50 ohm differential signal by BALUN, T1. The differential Rx signal is impedance matched to the uw2453 Rx (U3) inputs by L2, L5, C15, and C25. The uw2453 mixes a internally generated local oscillator signal and directly converts the received modulated 2.4GHz RF signal down to the Rx I/Q base band signals. The down converted analog Rx I/Q base band signals are output as a pair of differential signals and applied to the Rx dual ADC (U7). The normal I/Q differential output voltage is 1Vpp.

5.6 Receive analog to digital converter (U7)

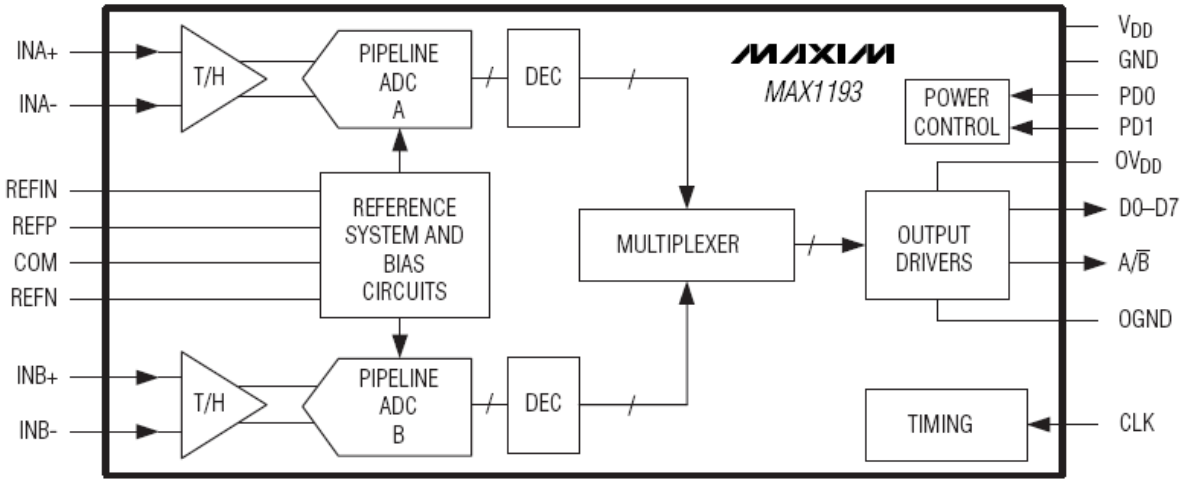


Figure 11 MAX1193 dual ADC block diagram

The Ubec uw2453 receiver outputs down converted base band I/Q analog signals that must be digitized and demodulated by the base band FPGA. A MAX1193 dual high speed 8 bit ADC is used for this conversion. The 1Vpp differential I/Q analog signals are converted into two 8 bit bytes which are multiplexed onto a single 8 bit data buss. Channel A Data (digitized I data) is read by the FPGA on the rising edge of the ACDCLK with ADCA/B high and channel B data (digitized Q data) is read on the rising edge of the ACDCLK with ADCA/B low. The ADCCLK runs at 40MHz so the two I/Q bytes are read at a 20MHz rate. In this design, the ADC's internal 0.512v reference is used which gives the LSB (0000 0001) a converted value of 4mV and a full scale output of 1.04V (1111 1111 >>> 256 x .004= 1.024V).

5.7 Antenna Switch U6

The antenna switch U6 is a 50 ohm low loss 6 GHz DPDT pin diode based antenna switch. It has two control pins that are used to switch the Rx and Tx pins between the two antenna ports. The base band controller FPGA drives the control pins based on the desired mode of operation. The table below shows the antenna switch's port connection possibilities.

Control Vc1	Control Vc2	ANT 1 - Rx	ANT 1 - Tx	ANT 2 - Tx	ANT 2 - Rx
1	0	On	Off	On	Off
0	1	Off	On	Off	On
1	1	Off	Off	Off	Off
0	0	Off	Off	Off	Off

Figure 12 Antenna switch control truth table

Since the data exchange between the ConnectCore 9W and the Access point is a half duplex exchange, the antenna (s) must be switched between the radio's receiver input and transmitter output. When Vc1 = 1 and Vc2 = 0 then the Rx signal port is connected to antenna 1 (P10) and the Tx signal port is connected to antenna 2 (P8). When Vc1 = 0 and Vc2 = 1, then the Rx signal port is connected to antenna 2 (P8) and the Tx signal port is connected to antenna 1 (P10). Antenna 1 is considered to be the "primary" antenna and as such it defaults as the first antenna used when antenna diversity is enabled or is the only antenna used in the single antenna configuration.

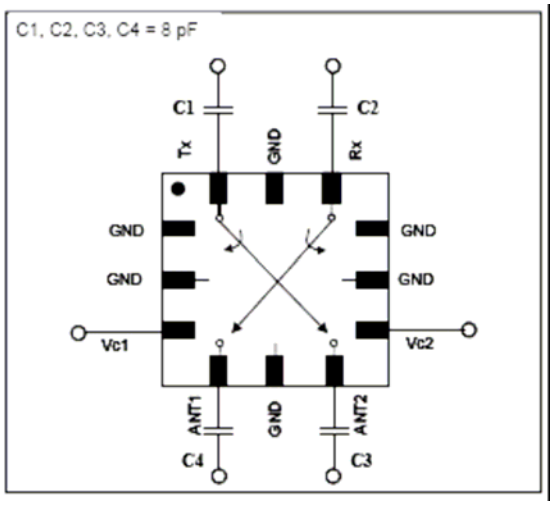


Figure 13 Antenna switch diagram

5.8 RP-SMA Antenna connectors P8 and P10 and Antennas

The antenna connectors used on the ConnectCore 9W are reverse polarity SMA connectors. The two antennas allow for an antenna diversity feature which, when enabled, can improve radio performance by selecting the antenna that gives the best signal reception. The base band controller FPGA controls the antenna selection.

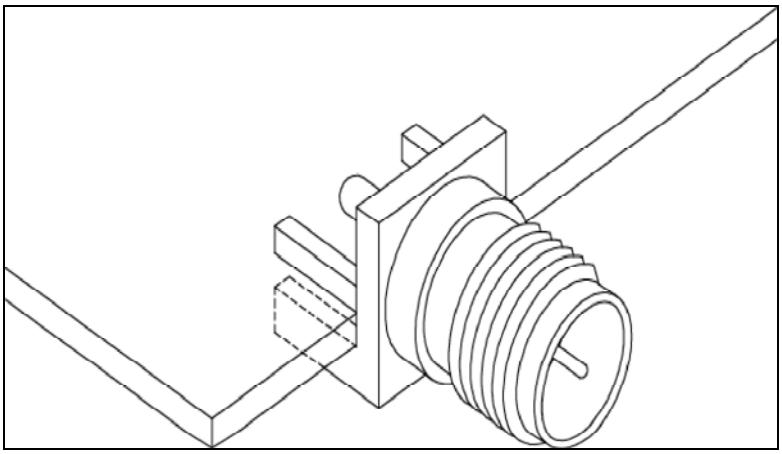


Figure 14 RP-SMA Antenna connector

The ConnectCore 9W is presently designed to use several detachable antennas. Two antenna types are specified: a 2dbi dipole that connects directly to the RP-SMA connectors and a 5dbi dipole that connects directly to the RP-SMA connectors. A version of the 2dbi dipole antenna comes with a 30cm extention cable

5.9 Radio power supply regulation

The critical sections of the Ubec 2453 are powered by locally regulated 2.85V +/-5% low drop out regulators. These regulators are supplied from the system +3.3V power and are capable of maintaining a 2.85V +/-5% output with an input voltage of < 2.93V. The Connect Core 9W will be forced into a hard reset if the system +3.3V falls to 2.93V and will cease to operate.

5.10 802.11b/g band frequency allocations

802.11b channel allocations

Channel	Center Frequency	Frequency Spread	
1	2412Mhz	2399.5Mhz - 2424.5Mhz	
2	2417Mhz	2404.5Mhz - 2429.5Mhz	
3	2422Mhz	2409.5Mhz - 2434.5Mhz	
4	2427Mhz	2414.5Mhz - 2439.5Mhz	
5	2432Mhz	2419.5Mhz - 2444.5Mhz	
6	2437Mhz	2424.5Mhz - 2449.5Mhz	
7	2442Mhz	2429.5Mhz - 2454.5Mhz	
8	2447Mhz	2434.5Mhz - 2459.5Mhz	
9	2452Mhz	2439.5Mhz - 2464.5Mhz	
10	2457Mhz	2444.5Mhz - 2469.5Mhz	
11	2462Mhz	2449.5Mhz - 2474.5Mhz	
12	2467Mhz	2454.5Mhz - 2479.5Mhz	
13	2472Mhz	2459.5Mhz - 2484.5Mhz	Europe
14	2484Mhz	2471.5Mhz - 2496.5Mhz	Japan

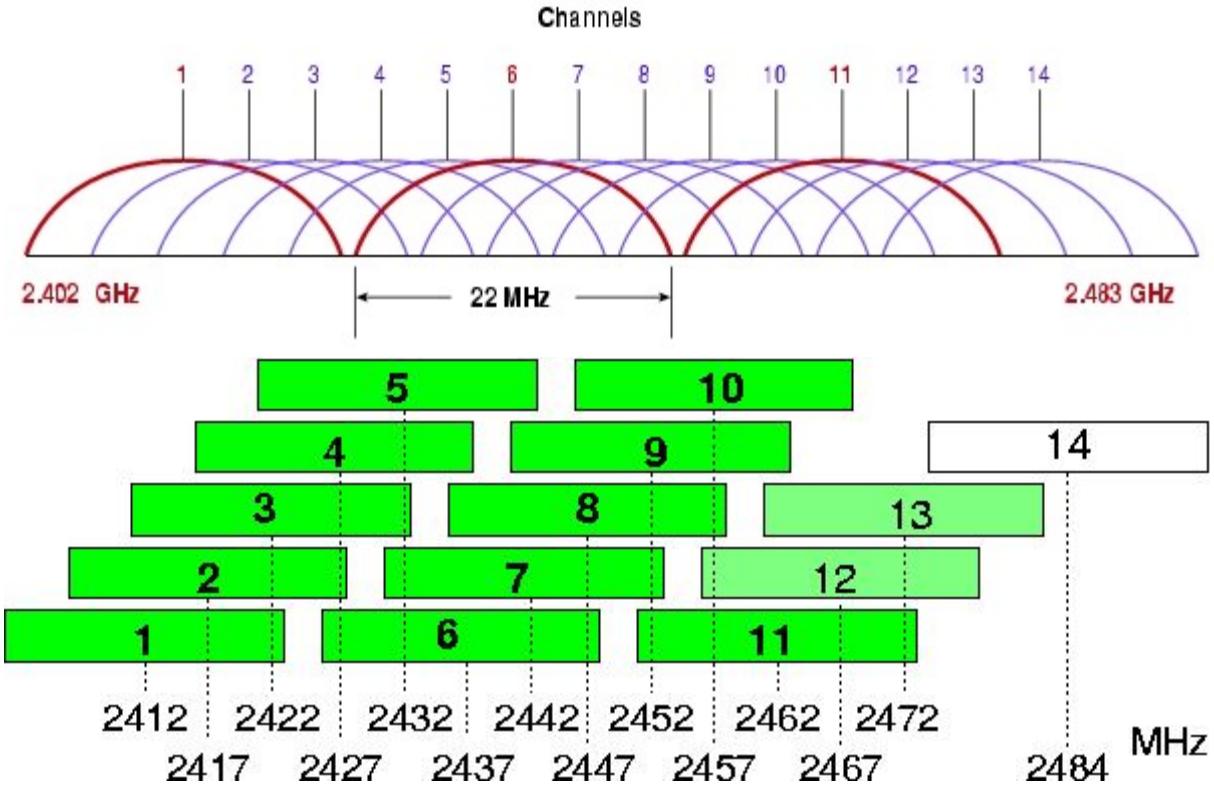


Figure 3 ---- 802.11b channel overlap

6.0 Power Requirements

The Digi Connect Core 9W requires 3.3Vdc for operation and 5V dc for USB (only). The 3.3Vand 5.5 are supplied from external source through SoDIMM connector, P3. The Digi Connect Core 9W draws the following current from 3.3V (with the NS9360 running with an 29.4912 MHz input crystal and a CPU_CLK of 154.8288 MHz).

Note: Spread spectrum clock system, Cypress FS781 is used to eliminate jitter generated by the LCD. External clock driver (29.4912MHz) is used to drive the spread spectrum clock system

3.3V @ 710mA typical during receive
3.3V @ 910 mA during transmit at max Tx power
5V @ 1A max, for USB devices connected to the module with on-board USB support

7.0 Environmental

The Digi Connect Core 9W board assembly shall meet all functional requirements of this Specification when operating in the environment listed below.

Operating temperature: -30° C to +85° C (-22° F to +185° F)
Storage temperature: -40° to +125°

Relative humidity: 5% to 95% (non-condensing)
Altitude: 12,000 ft (3657.6 m)

8.0 Mechanical

Length: 3.5 inches (88.9 mm)
Width: 2.1 inches (53.34 mm)
Height: 0.8 inches (20.32 mm) with RJ-45 Ethernet connector

9.0 Approvals

The Digi Connect Core 9W shall be certified to meet the following emissions, safety and immunity standards.

Emissions:
AS/NZS CISPR 22:2002 class B
ICES-003
EN 55022: 1998/FCC class B Emissions
FCC Part 15 Subpart C Section 15.247
IC (Industry Canada) RSS-210 Issue 5 Section 6.2.2(o)
EN 300 328
EN 301 489-3

Safety:
UL/CUL 60950-1
IEC/EN 60950-1

Immunity
EN 55024:1998

10.0 DVT PLAN: SCOPE

This document is the Digi International Engineering Design Verification Test procedure. It provides an outline of the tests and parameters to be analyzed on the Digi Connect Core 9W 10/100baseT Ethernet to Serial Port or USB The following paragraphs list the functional blocks of the board and include the signals analyzed in each block. The electrical Design Verification test includes all nets on the board.

11.0 COMPONENTS OF THE PRODUCT

Digi P/N 55001167-01	Dig Connect Core 9W NS9360 Assembly Parts List
Digi P/N 30006531	Printed Circuit Schematic
Digi P/N 30006532	Printed Circuit Board Drawings
Digi P/N 30006534	Placement Drawing

12.0 REFERENCE MATERIALS

ISC 1893BKILF (16050798)	Component specification
TUSB2046BI (16050830)	Component Specification
8MX32 SDRAM (16050482)	Component Specification
4MX16 FLASH (42000811)	Component Specification

13.0 TESTING ENVIRONMENTS

The Electrical Design Verification Tests starts with a paper analysis of access, hold, setup and other timing parameters for devices on the board. It also includes the measurement of timing on the board at room temperature; verifying power and ground connection to the devices, and ensuring conformance to the relevant standards. Any violations will be noted in the design notebook, corrected, and re-verified.

Several functions will be analyzed, including the NS9360 bus interfaces (Digi P/N 16050802), SDRAM timing (Digi P/N 16050482), USB and ETHERNET interfaces. The complete assembly (Digi P/N 55001164-01) will be tested for EMC (EN550024), Immunity (55024:1998) and Safety (EN60950). All tests listed in this section will be performed or supervised by a design engineer. In certain cases (as defined below) independent test facilities will be used to confirm conformance.

13.1 Test Environment

The following list of equipment is necessary to perform the DVT on the Connect Core 9W module. All equipment used must be recorded in the design notebook.

a) Diagnostic Software
b) Digi 55001166-01 Carrier board
c) Applicable test equipment (Loop back Cables, DVOM, logic analyzer, digital oscilloscope)
e) Design Notebook

13.2 SDRAM Memory

The SDRAM memory has several possible operating modes and all have to be verified. Including single reads and writes plus burst reads and writes (DMA). For all cases, control signal pulse widths, address set-up and holds, ready timing, and access will be verified. The reset and operational characteristics of all

signals related to these accesses will be verified. Arbitration between refresh and processor accesses will also be verified. Any violations will be noted, fixed and re-verified.

13.3 Interrupt Test

NA

13.4 Peripheral Accesses

NA

13.5 Serial Interface

The Serial interface will be verified with loop back cable. Signal polarity, levels, and rise/fall times will be measured.

13.6 Power Measurements

This test also is used to measure upper and lower cutoffs for 3.3V.
The upper and lower cutoffs were defined by +/- 10% of 3.3V and are 3.63V and 2.97V respectively.

Power in will be measured:

V in	I in	
2.97	.350A	Lower cutoff
3.63	.420A	Upper cutoff

13.7 Signal Integrity

Control signal, clocks, and busses (address and data) will be examined with a high-speed scope for signal integrity. Undershoot more than -2V or overshoot greater than +2V for the pulse width ≥ 3ns (see Digi 16050482, SDRAM HW spec page 35, note 22)and discontinuities in clock edges will be considered failures and will be fixed and re-verified. Note that probing issues are critical in these measurements. Use of FET probes and minimal ground leads is necessary.
Figures 1 - 5 are of various high speed signals. All of these signals meet the above criteria.

13.8 PASS/FAIL Criteria

The above verifications tests are measures of design margin and any parameters that verify as marginal or affect the reliable operation will be corrected before the final release.

14.0 PASS/FAIL CRITERIA FOR THE TEST RESULTS

Diagnostic Testing and Verification:

In this section the Connect Core 9W will be tested in the lab environment. The tests will verify functionality of the Ethernet, USB and SDRAM signals (i.e. correct bus operation and passing data). The diagnostics will be tested in this section to verify that they can catch all significant signals on the product.

14.3 Test Entry Criteria

a) Completion of hardware testing

14.2 Ethernet Interface Signal Integrity Test
The Digi Connect Core 9W Ethernet signals will be tested, recorded and verified. All abnormalities will be corrected and retested. The following signal were tested and recorded:

Signal Name	Mnemonic	Point of measurement
Ethernet Transmit CLK	ETCLKR	R37
Ethernet Receive CLK	ERCLKR	R36
Receive Data 0	RxD0	U10, pin31
Receive Data 1	RxD1	U10, pin30
Receive Data 2	RxD2	U10, pin29
Reference CLK OUT 25 MHz	REF_OUT	U10, pin46
Reference CLK IN 25 MHz	REF_IN	U10, pin47
Ethernet Data 0 Transmit	TxD0	U10, pin39
Ethernet Data 1 Transmit	TxD1	U10, pin40

Figure 1.1 – 1.6

14.3 SDRAM Signal Integrity Test
The Digi Connect Core 9W SDRAM signals will be tested, recorded and verified. All abnormalities will be corrected and retested. The following signal were tested and recorded:

Signal Name	Mnemonic	Point of measurement
Chip Select	/CS	U4, pin 19
Row Access Select	/RAS	U4, pin 18
Column Access Select	/CAS	U4, pin17
Write Enable	/WE	U4, pin 16
SDRAM CLK (77 MHz)	CLKOUT2	U4, pin 38
Address line 0	A(0)	U4, pin 23
Address line 4	A(4)	U4, pin 29
Data Line 0	D(0)	U4, pin 2
Data Line 5	D(5)	U4, pin 10

NOTE: Undershoot above -2V or overshoot less than +2V for the pulse width ≤ 3ns is acceptable according to SDRAM HW spec (see Digi 16050482) page 35, note 22.
Figure 2.1 – 2.9

14.4 USB Signal Integrity Test
The Digi Connect Core 9W USB signals will be tested, recorded and verified. During this test Upper USB connector was used and was connected to the optical mouse. All abnormalities will be corrected and retested. The following signal were tested and recorded:

USB DM2 (Data Minus port 2) signal was captured at C75.

- Rise time (10% - 90%) was measured and recorded, Δtr = 140 ns.
- Fall time (10% - 90%) was measured and recorded, Δtf = 148 ns.
- For Full Speed Mode (12Mb/s) Ration between rise and fall time is (Δtr/ Δtf) x 100% = 95% within the spec.

Figure 3.1 -3.6

14.7 Serial Interface Hardware Compatibility Test

The Digi Connect Core 9W will be tested with all possible line configurations, using a variety of serial communication devices (modems, DSU/CSU). Product management will provide a list of devices to the Systems Assurance group. All failures will be corrected and the system re-tested.

14.8 Test Exit and PASS/FAIL Criteria

Upon completion of all tests in the software section, the results will be reviewed. If the reviewed results are error free, the software test will be considered successful and the test will pass. If there are errors in the reviewed results, appropriate corrective action will be taken and the tests repeated.

Product conforms.

System Verification:

The objective of the system verification is to test the Digi Connect Core 9W product with other adapters to verify operation in a customer setting. These tests will also verify the installation and operation of the drivers FEP/OS and BIOS. System verification will also include the testing of the field diagnostics and production diagnostics.

14.9 Test Entry Criteria

a) Completion of hardware testing
b) Completion of diagnostic testing and verification
c) Digi Connect Core 9W boards (55001164-01).

14.10 EMC Test Environment & Standards

The Digi Connect Core 9W will be tested to FCC part 15 Class B, ICES-003 Class B, and EN55022 Class B limits for EMC with a margin goal of -3 dB. See the hardware Specification (30048703) for EMC standards revisions. The testing will be done by connecting via telnet to a remote device in a shield room and invoking the FCC or immunity test option. The RS232 cables will be looped back, and Ethernet traffic will flow to the remote device. Using this approach will maximize emissions in a system test.

The Digi Connect Core 9W will also be certified to immunity standard IEC 55024:1998. This testing will be done as noted above.

14.10.1 Serial Interface ESD Testing

The product will be tested to meet the 55024:1998 ESD requirements. Failures will be noted, fixed, and re-verified.

14.11 Safety Test Environment & Standards

The Digi Connect Core 9W will be tested to EN60950, UL1950, and CSA 22.2 No. 950 safety requirements. See the hardware Specification (30048700) for EMC standards revisions.

14.12 Guard band and Environmental Test Environment & Standards

14.12.1 Guard band testing

Operating the board under low and high voltage conditions until a failure occurs will perform guard band verification. The voltage at which the failure occurs will be recorded. A failure of the product, when the voltage is raised or lowered within the normal operating voltage of the product, will be considered a FAIL and will be noted in the design notebook, fixed, and re-verified.

14.12.2 Operating Temperature

The board will be operated in the system at maximum and minimum ambient operating temperatures. Typically, the tests will be performed from -40 deg. C to +85 deg. C. Operation at the elevated temperature will be confirmed over a 72-hour period. Operation while cycling from high to low temperature will be confirmed. A failure of the product, when the temperature is raised or lowered within the normal operating temperature of the product, will be considered a FAIL and will be noted in the design notebook, fixed, and re-verified.

14.13 Interoperability Test Environment & Standards

The Digi Connect Core 9W will be tested with a variety of serial communication devices (modems and DSU/CSUs). This will verify interoperability with other I/O vendor peripherals. Product management will identify EMC cards. A problem with the diagnostics or Drivers when the Digi Connect Core 9W is installed with other servers will be noted and documented. If the Digi product caused the failure, the problem will be corrected and re-verified. If the failure is caused by another adapter card the failure will be noted.
This testing was done by SA. Product passed.

14.14 Test Exit and PASS/FAIL Criteria

Upon completion of all tests in the system section, the results will be reviewed. If the reviewed results are error free the system test will be considered successful. If there are errors in the reviewed results, appropriate corrective action will be taken and the tests repeated. A summary of DVT results will be generated on test exit.

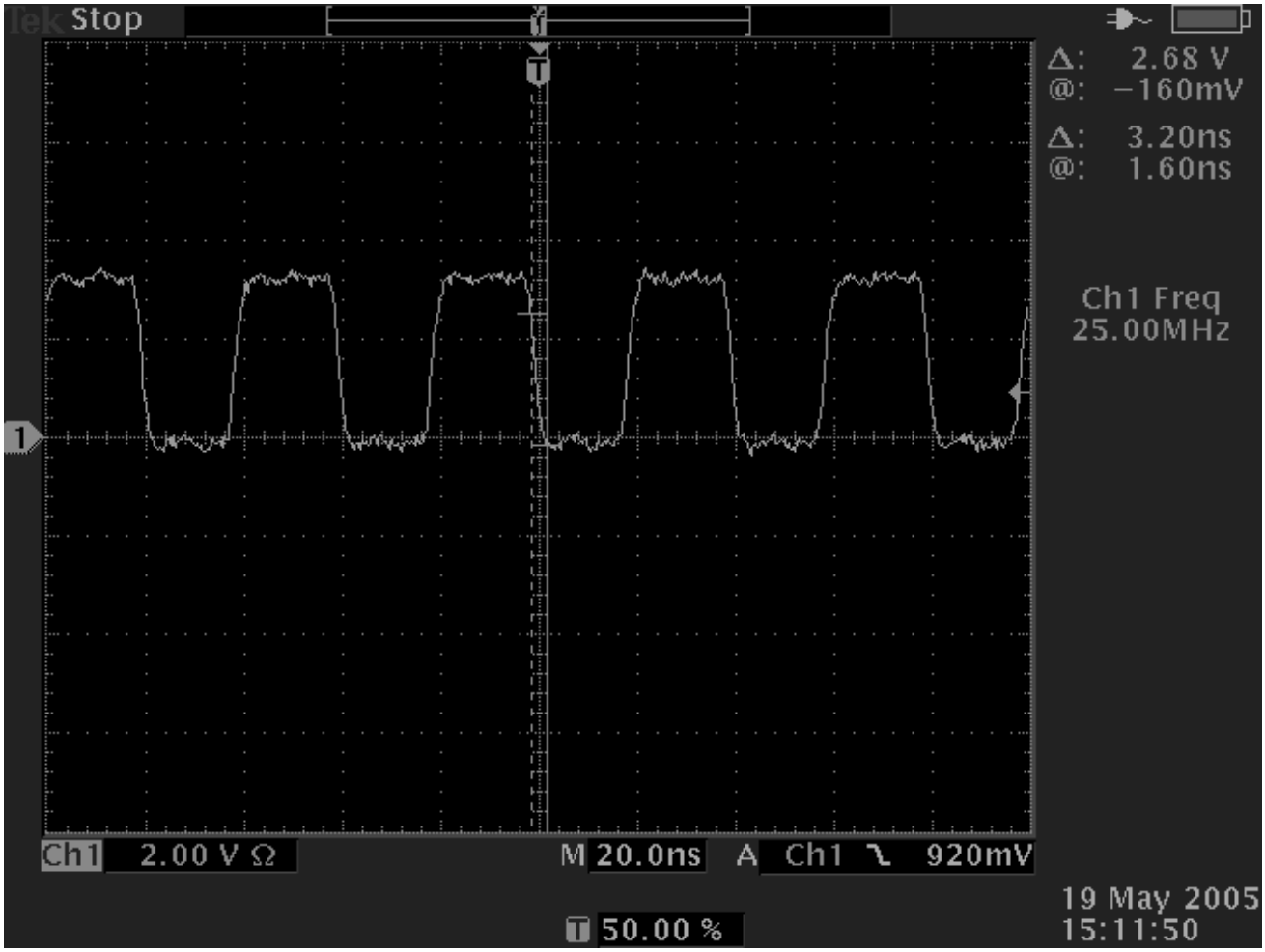
DVT PLAN SCOPE SHOTS

The following scope shots illustrate the signal integrity as well as the basic timing of the important signals on the Digi Connect Core 9W.

Signal Plots

Figure 1

The above scope shots are of the Digi Connect Core 9W Ethernet Related signals
Amplitude and frequency of the signals are displayed in the top right corner of the oscilloscope display.



2
Figure 1.1 - Ethernet Transmit CLK

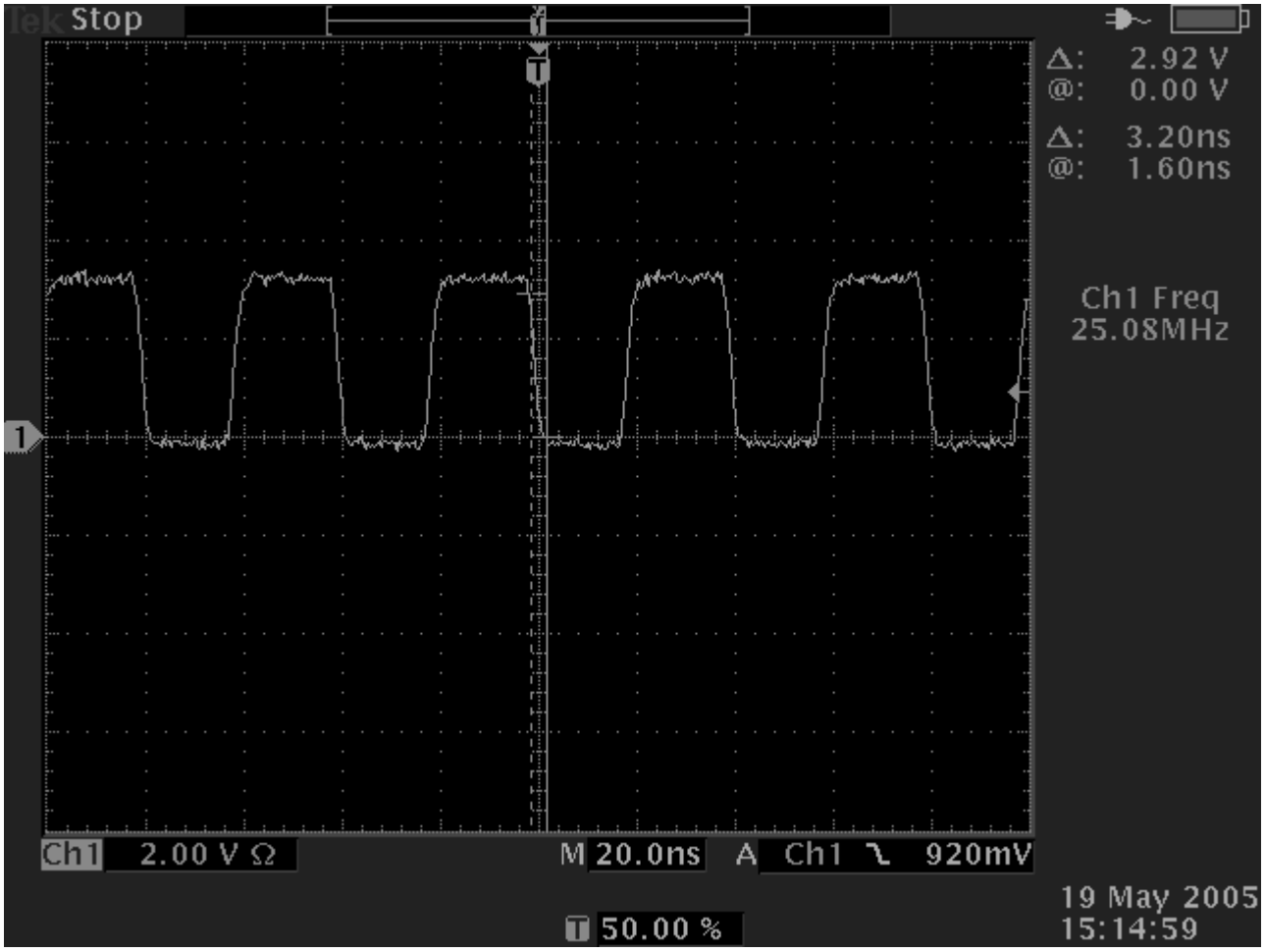


Figure 1.2 - Ethernet Receive CLK

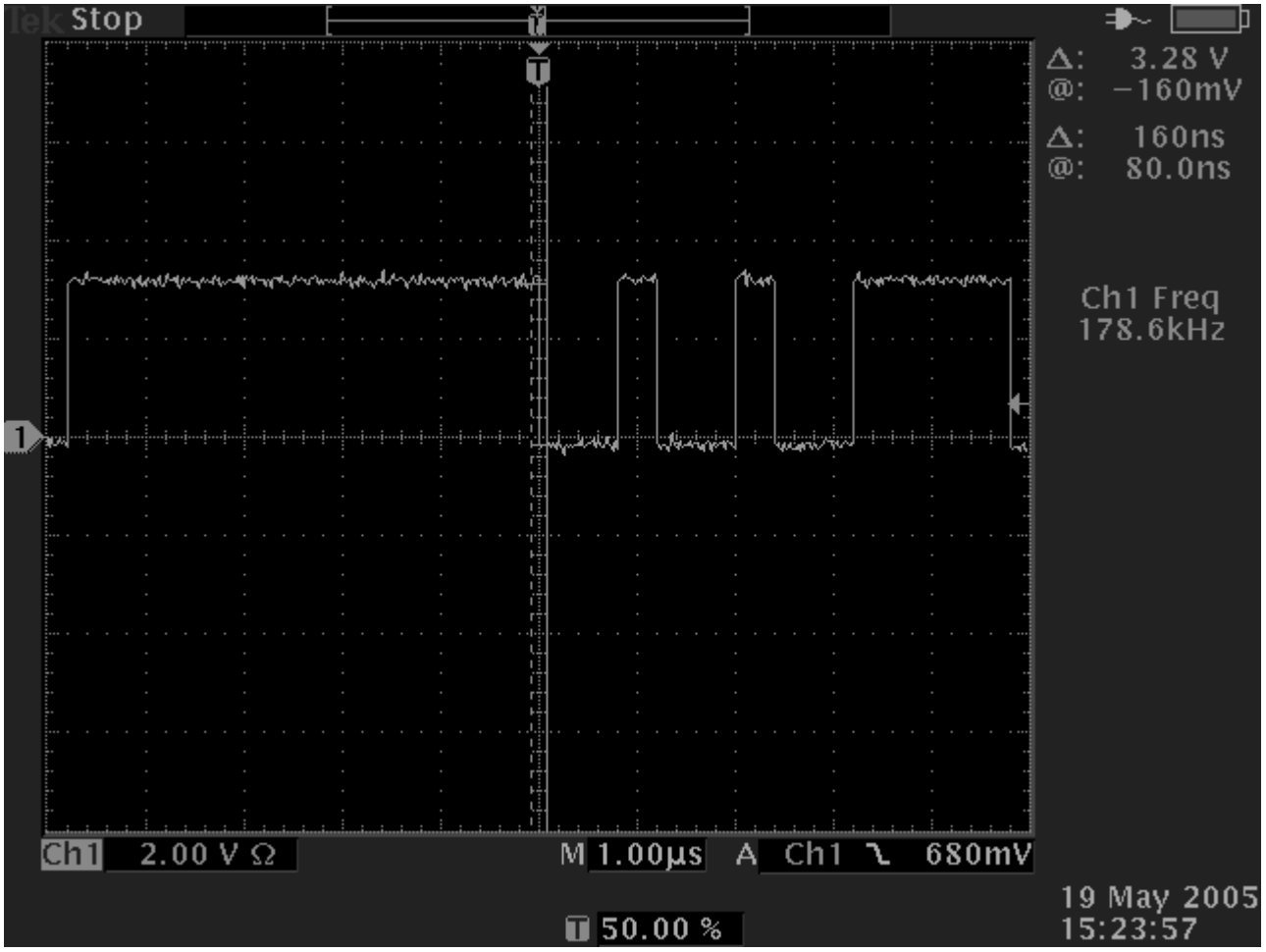


Figure 1.3 - Receive Data 0

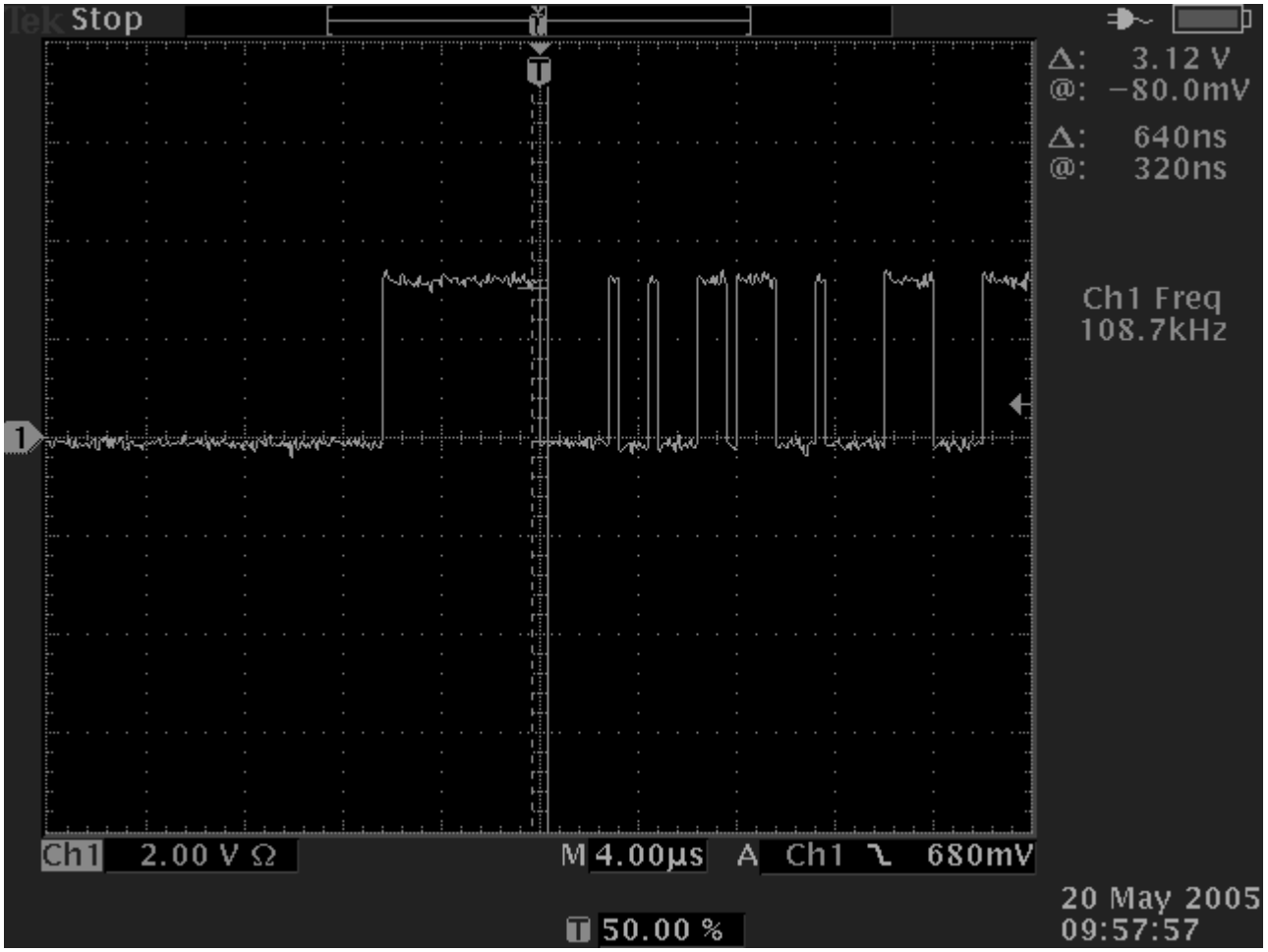


Figure 1.4 - Ethernet Data 0 Transmit

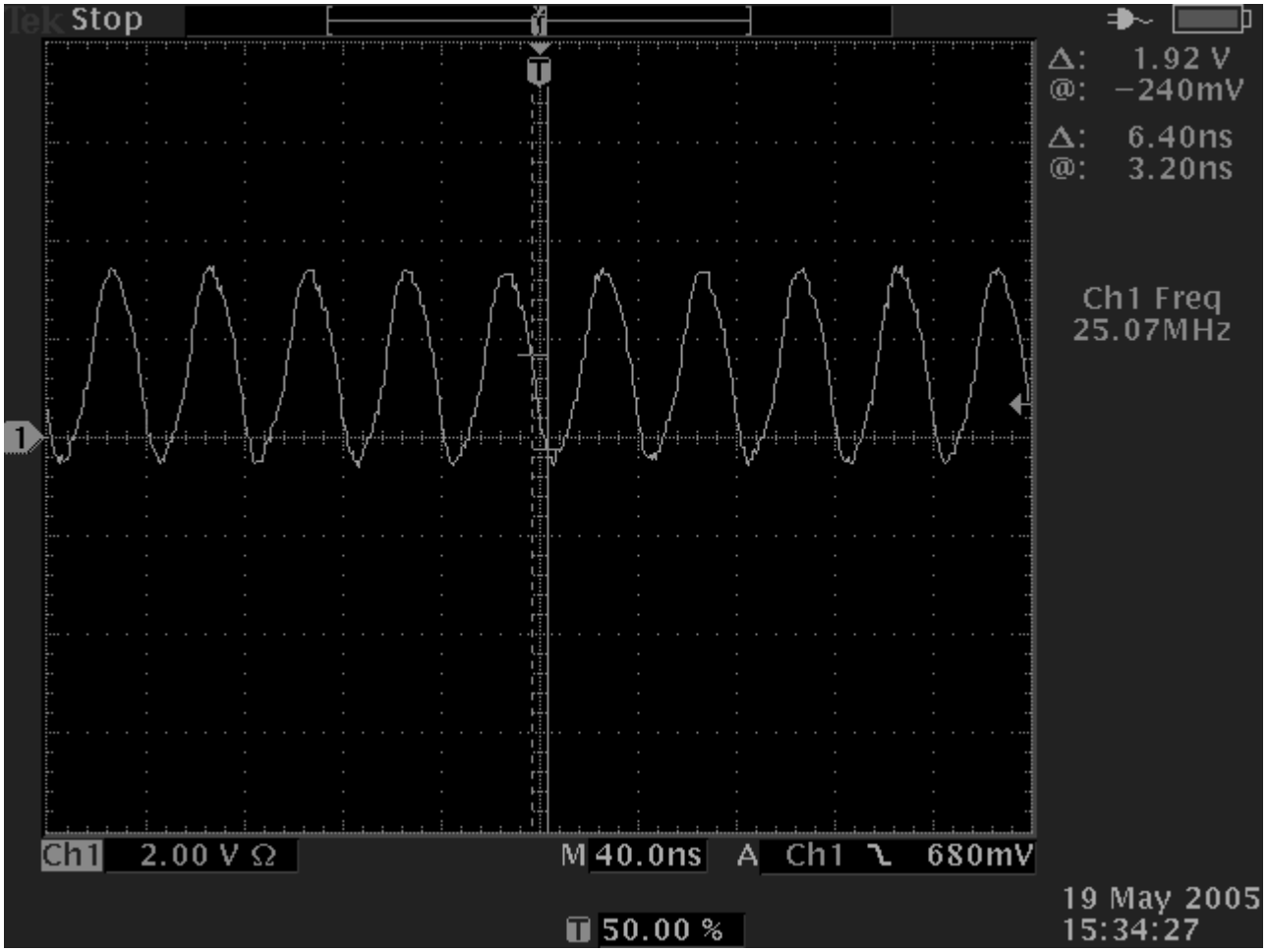


Figure 1.5 - Reference CLK OUT 25 MHz

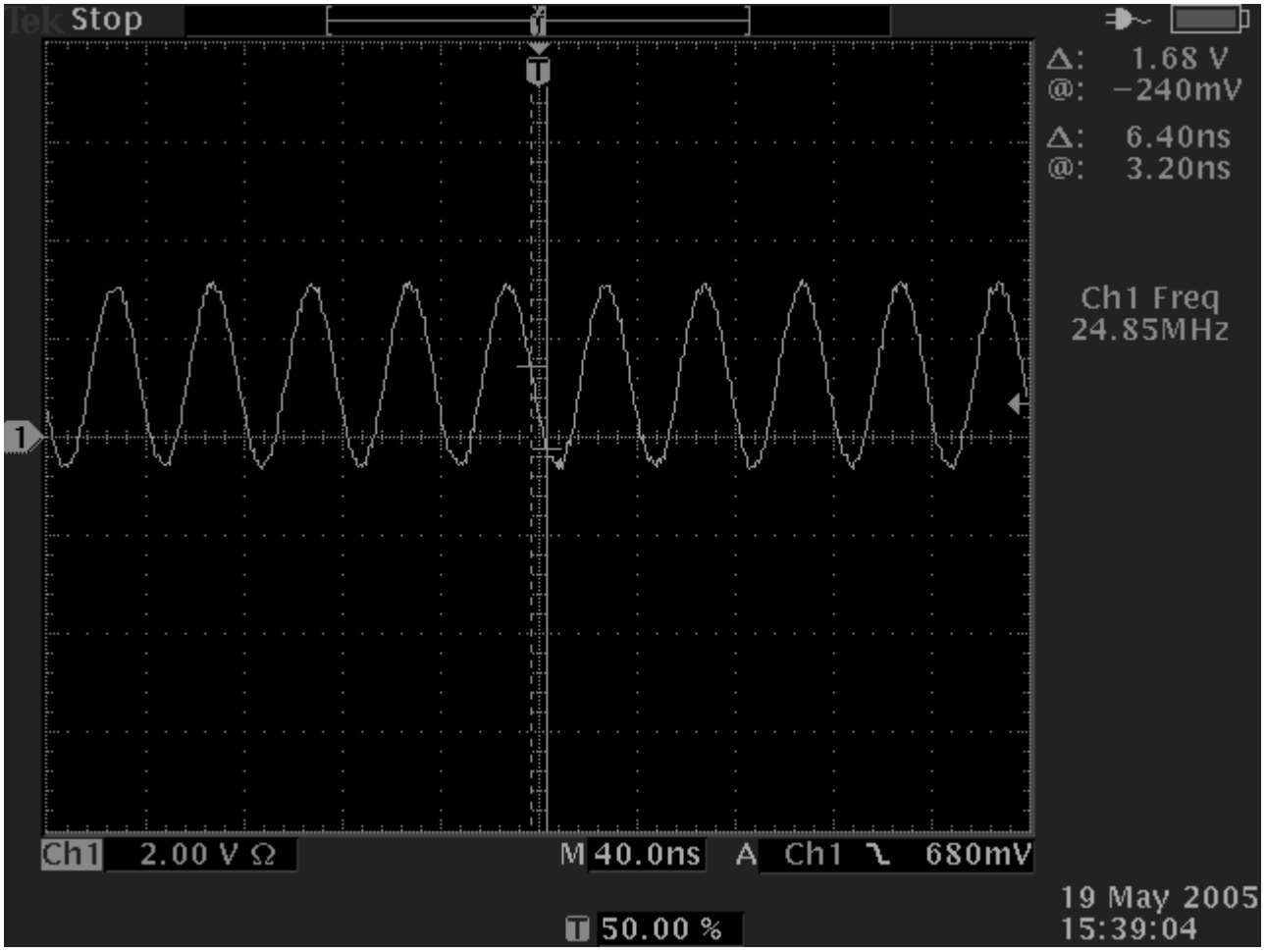


Figure 1.6 - Reference CLK IN 25 MHz

Figure2
SDRAM related plots

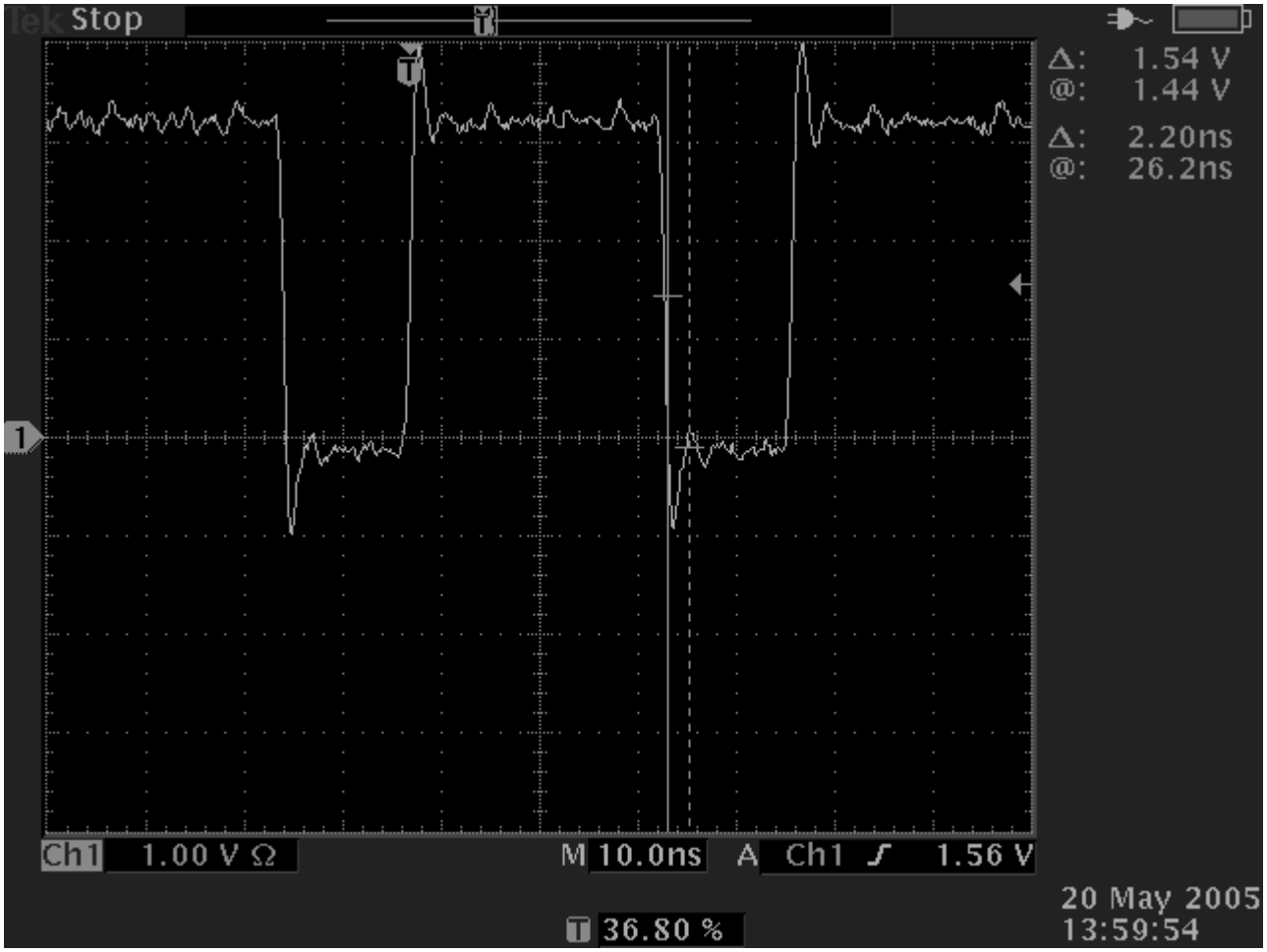


Figure 2.1 - Chip Select (/CS)

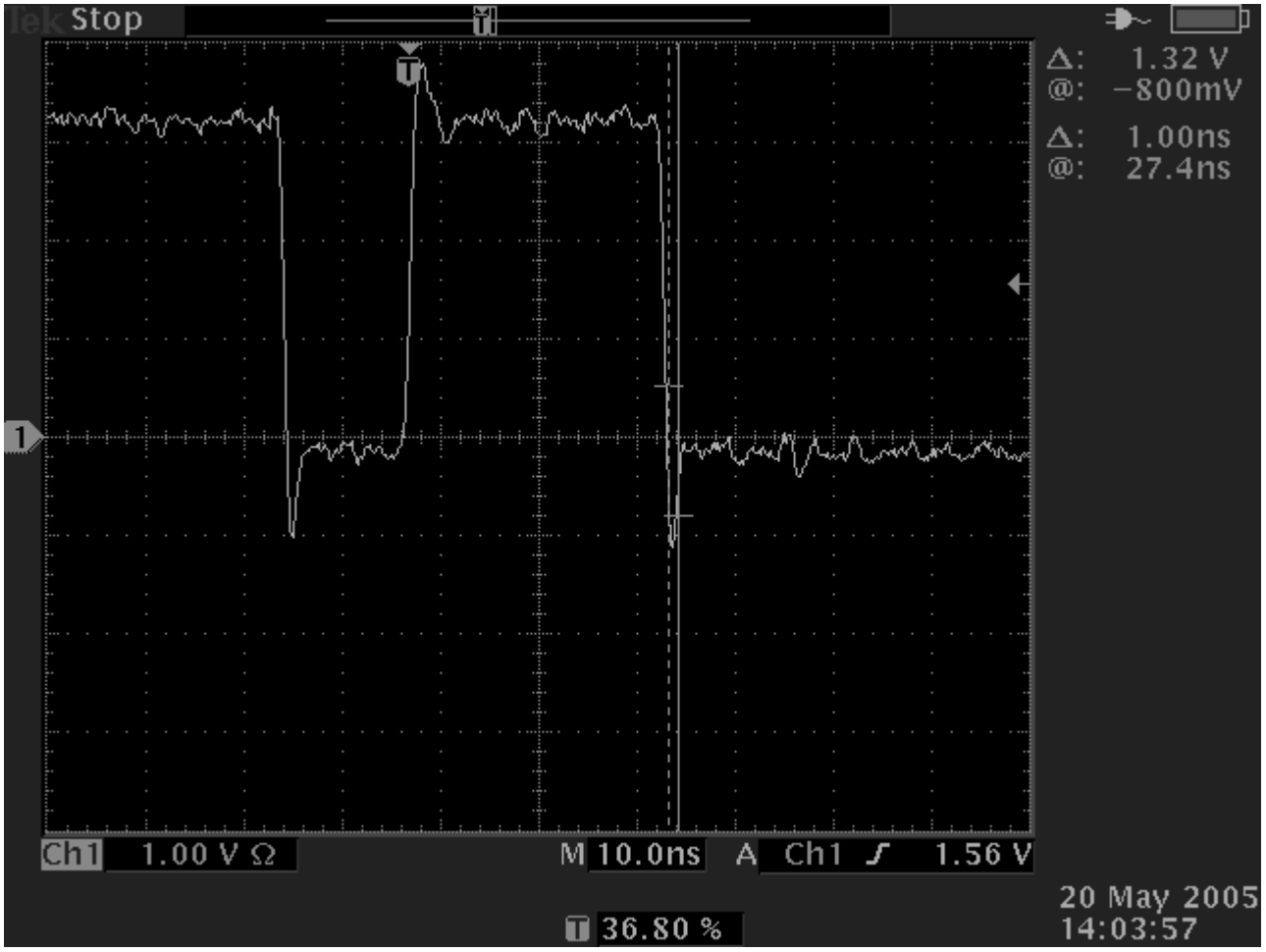


Figure 2.2 - Row Access Select (/RAS)

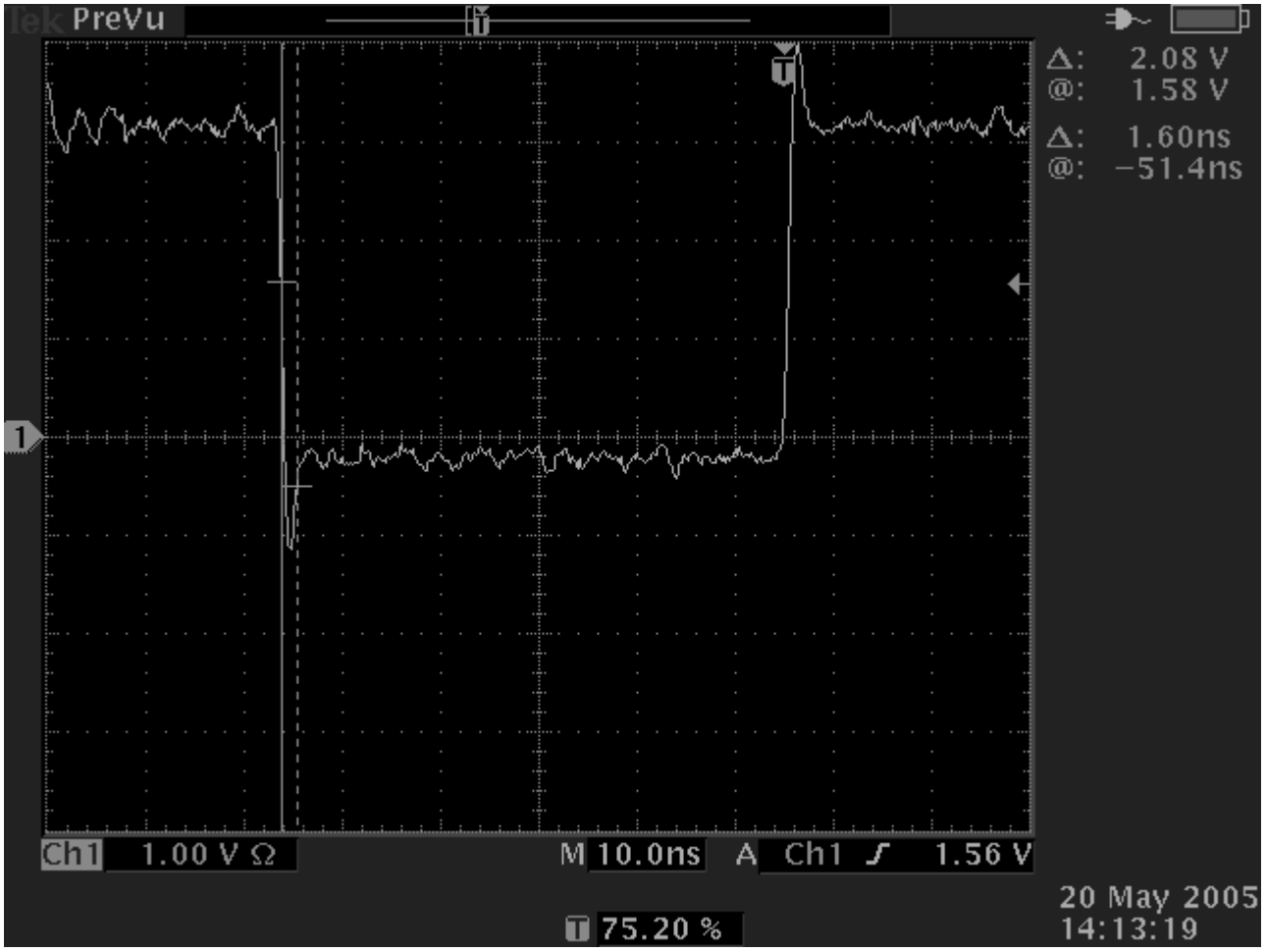


Figure 2.3 - Column Access Select (/CAS)

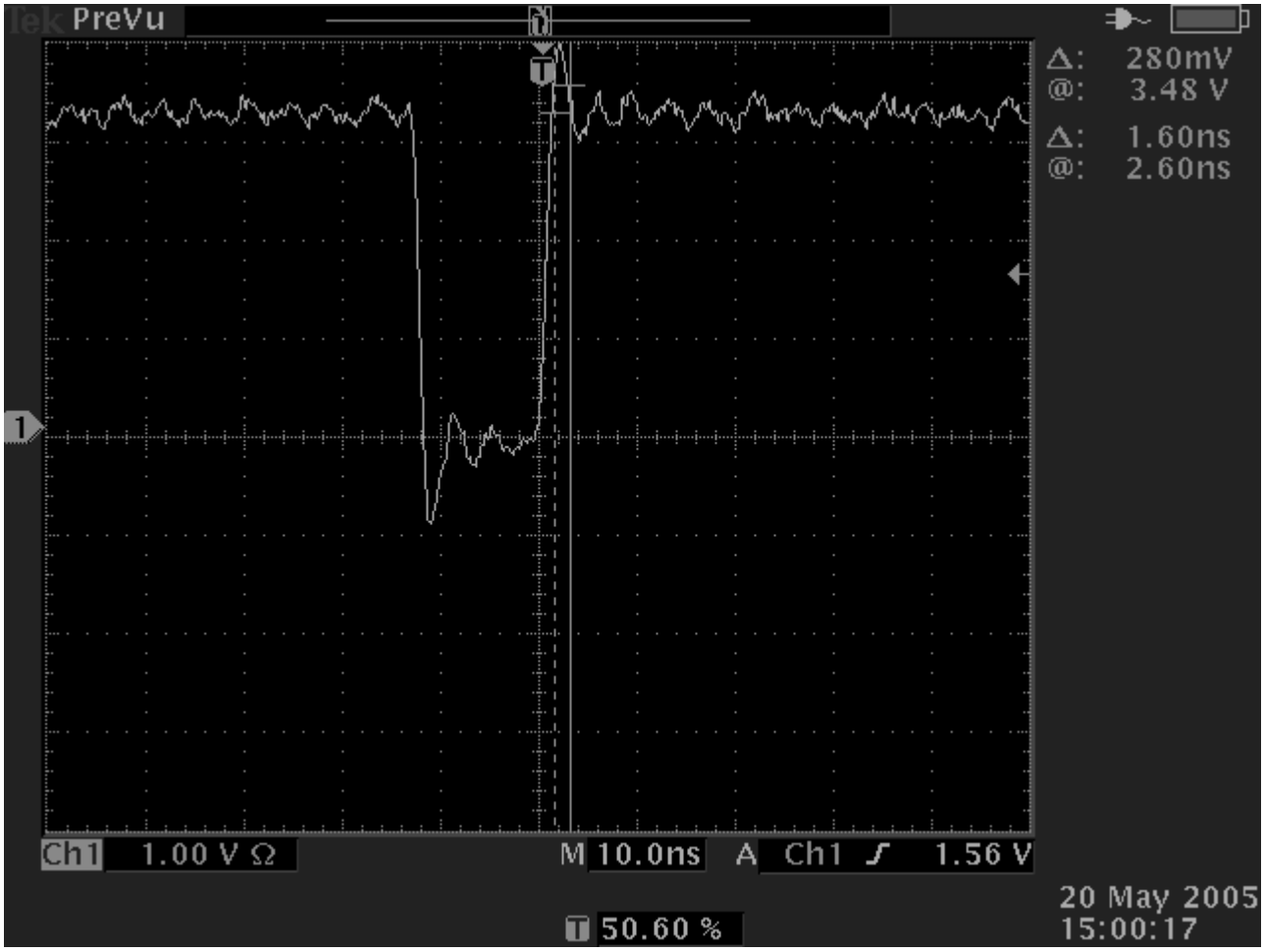


Figure 2.4 - Write Enable (/WE)

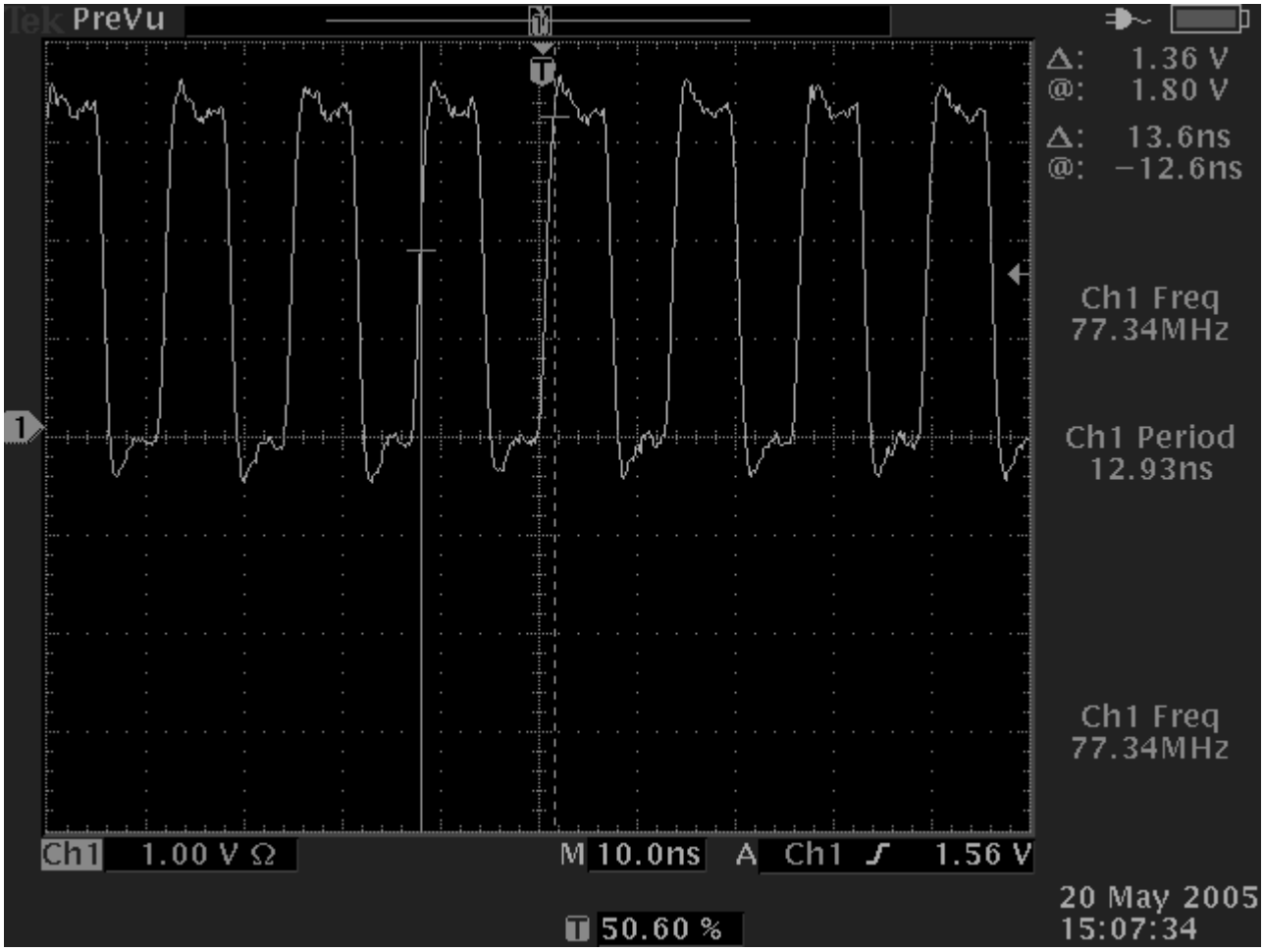


Figure 2.5 - SDRAM CLK (77 MHz)

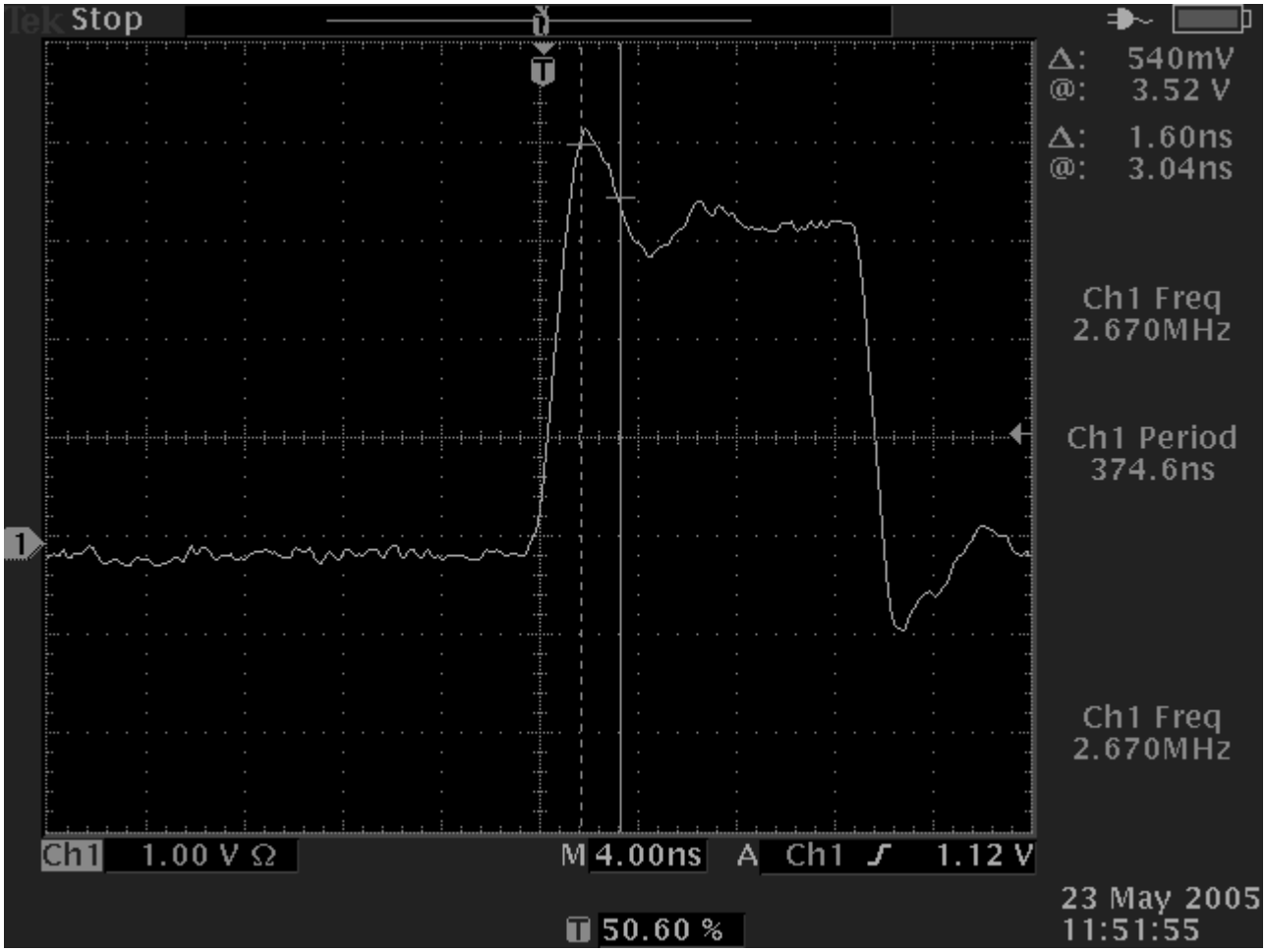


Figure 2.6 - Address line 0, A(0)

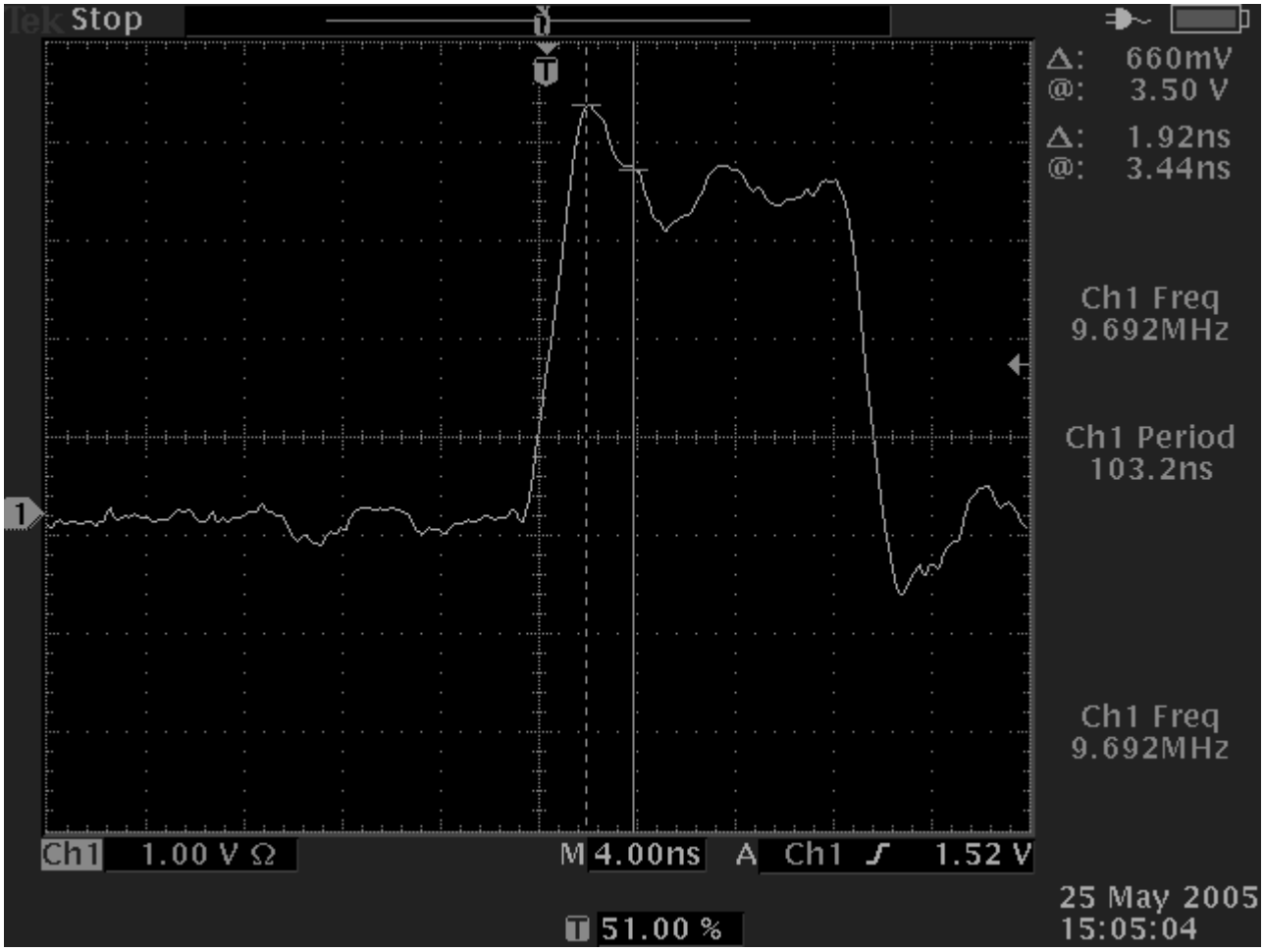


Figure 2.7 - Data Line 0, D(0)

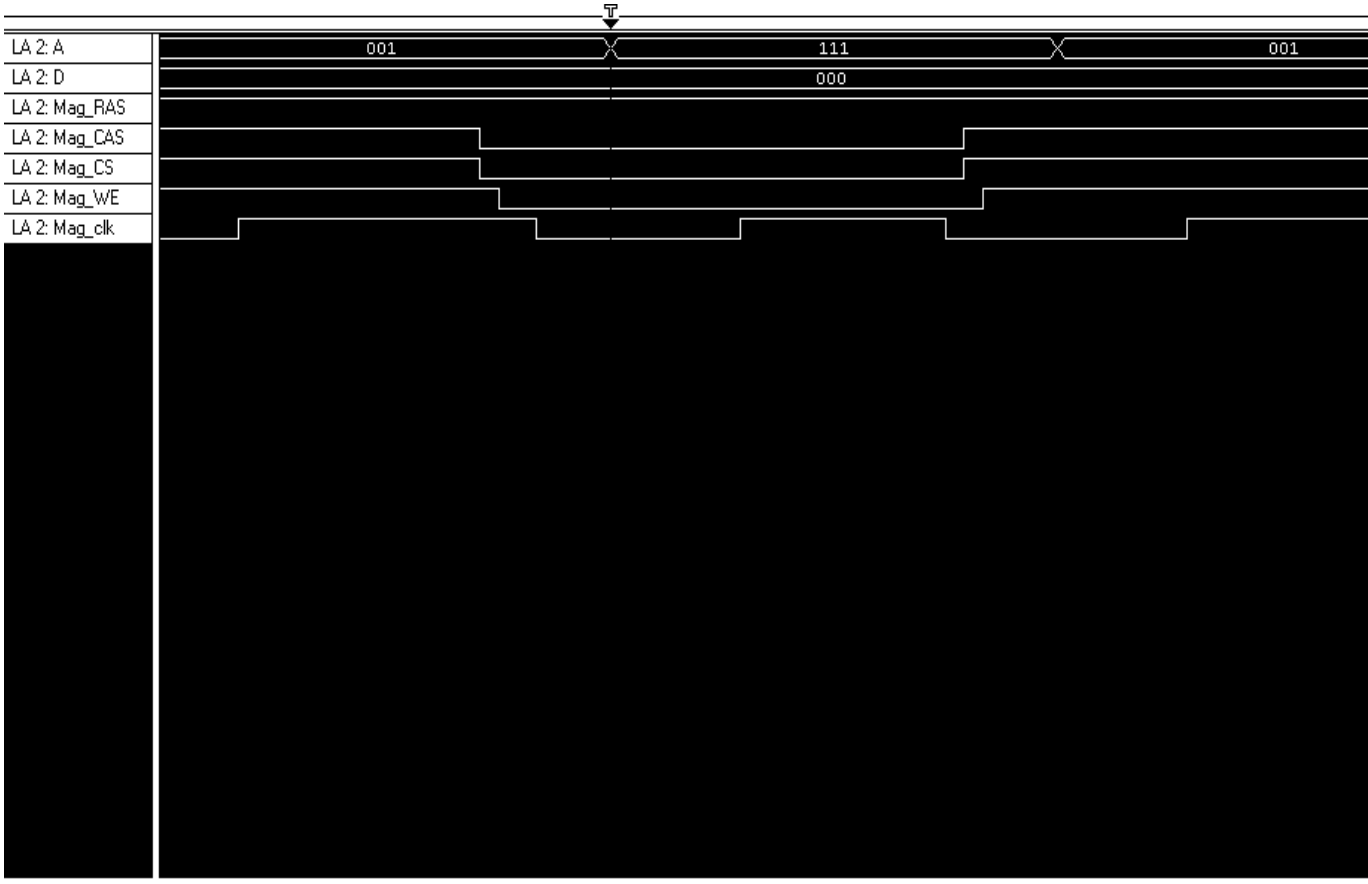


Figure 2.8 – SDRAM Write Cycle
The above scope shot is of a complete write cycle to SDRAM. The Address line, Data Line, Chip Select, RAS, CAS, SC, WE and CLK are all displayed in the order. (Used for illustration to show when data changes in relation to other signals).

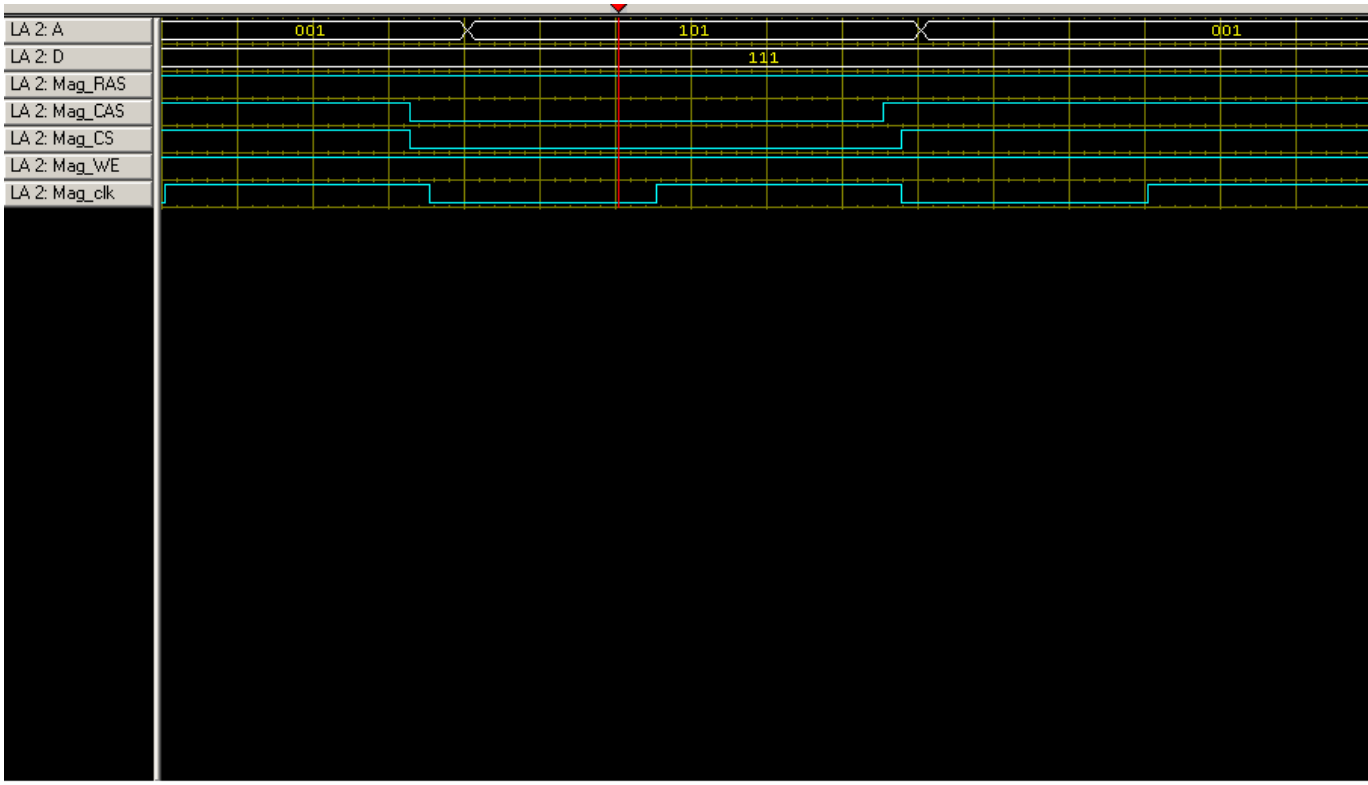


Figure 2.9 – SDRAM Read Cycle
The above scope shot is of a complete read cycle from SDRAM. The Address line, Data Line, Chip Select, RAS, CAS, SC, WE and CLK are all displayed in the order. (Used for illustration to show when data changes in relation to other signals).

Figure 3.
USB related plots

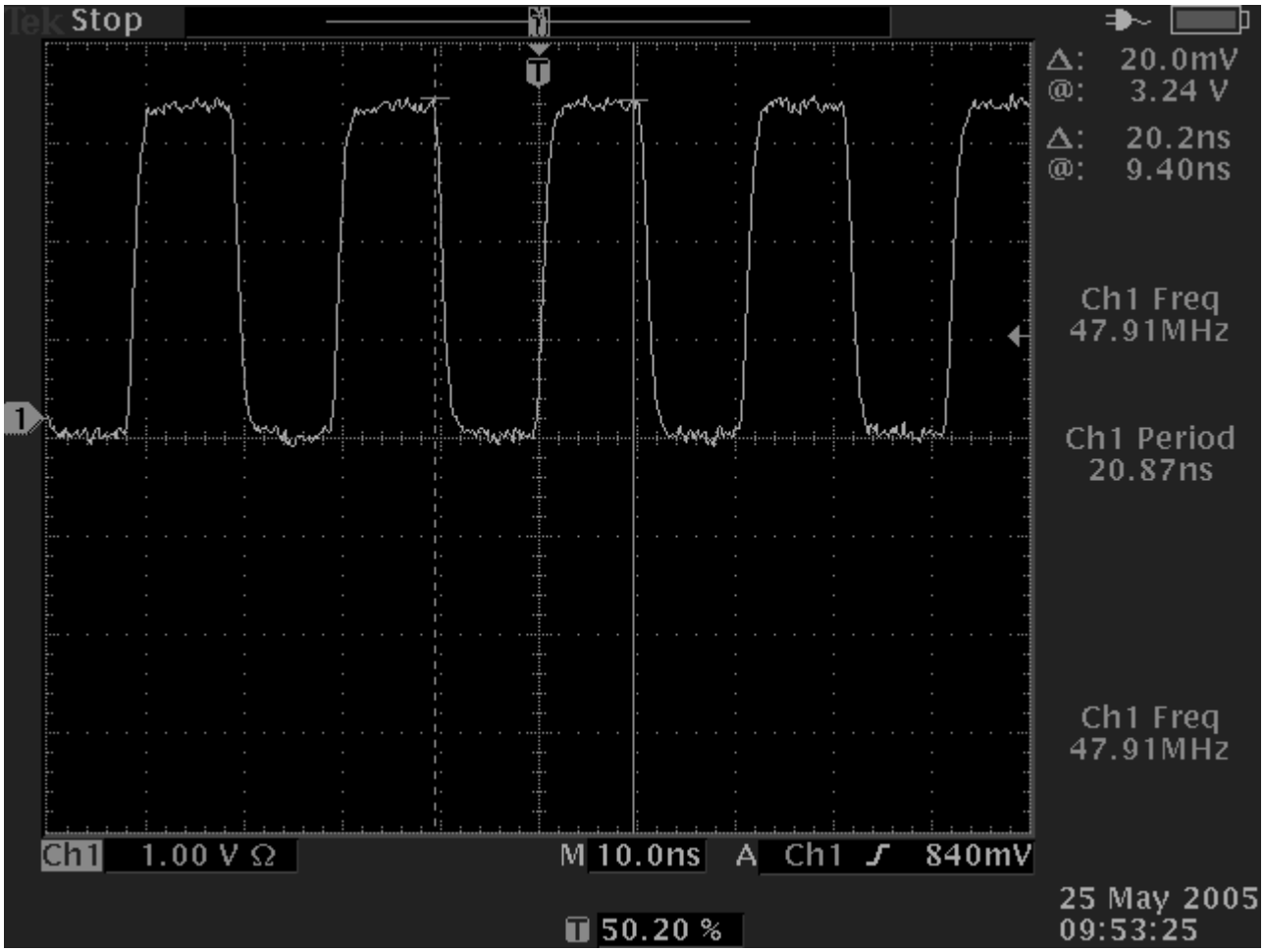


Figure 3.1 – USB CLOCK, 48MHz

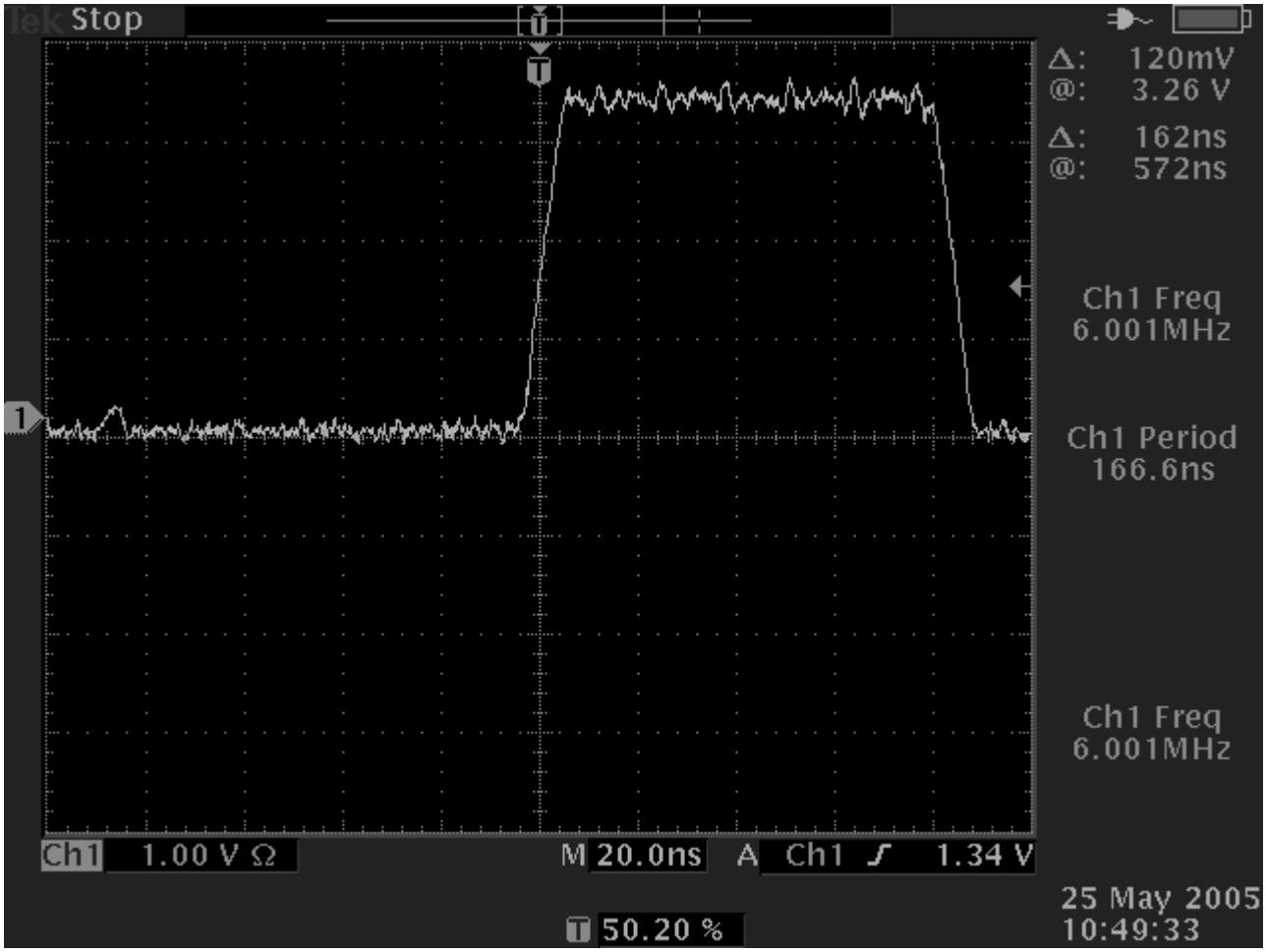


Figure 3.2 – Data Port Minus between USB HUB and NS9360

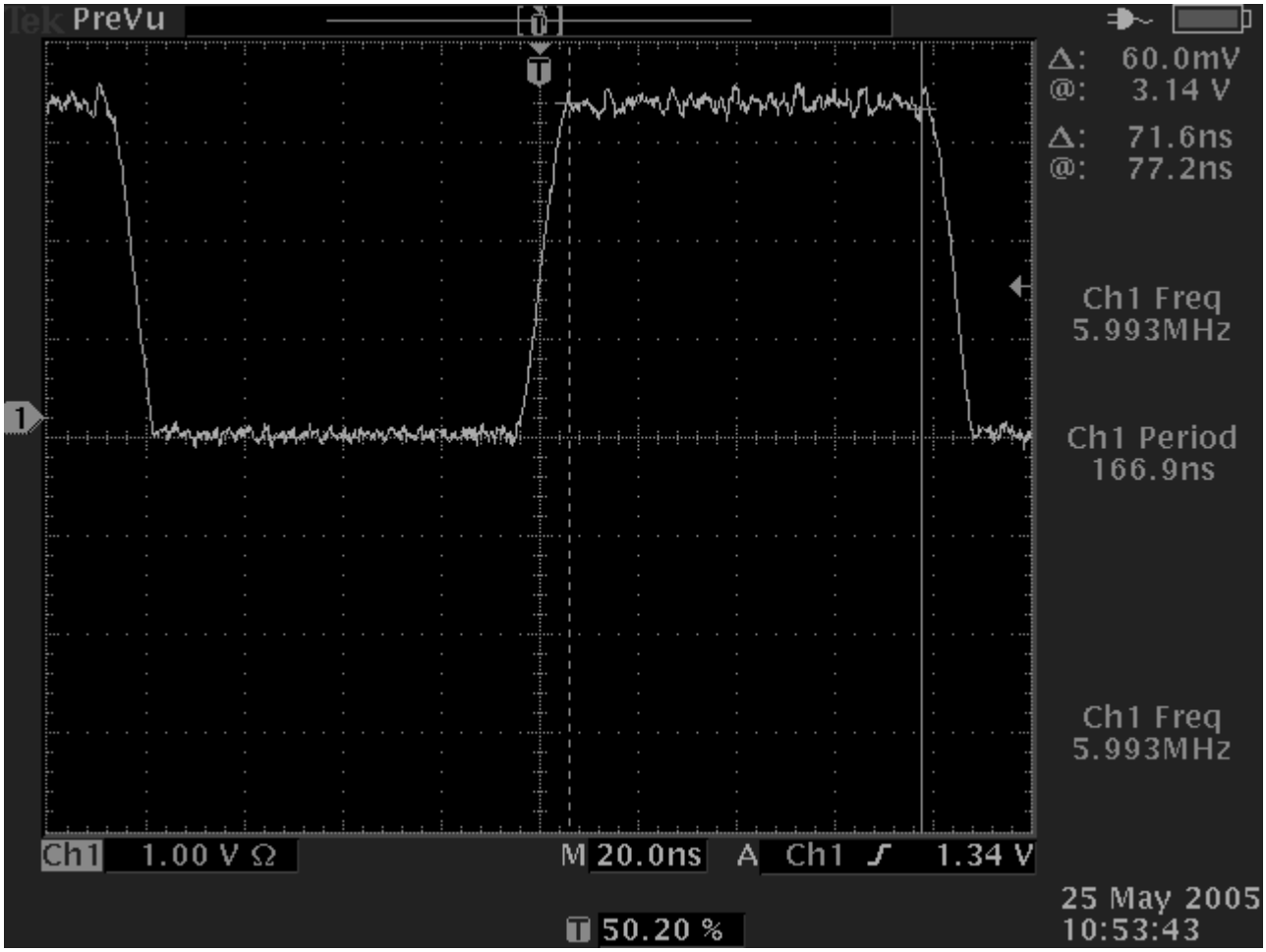


Figure 3.3 – USB, Data Port Plus between USB HUB and NS9360

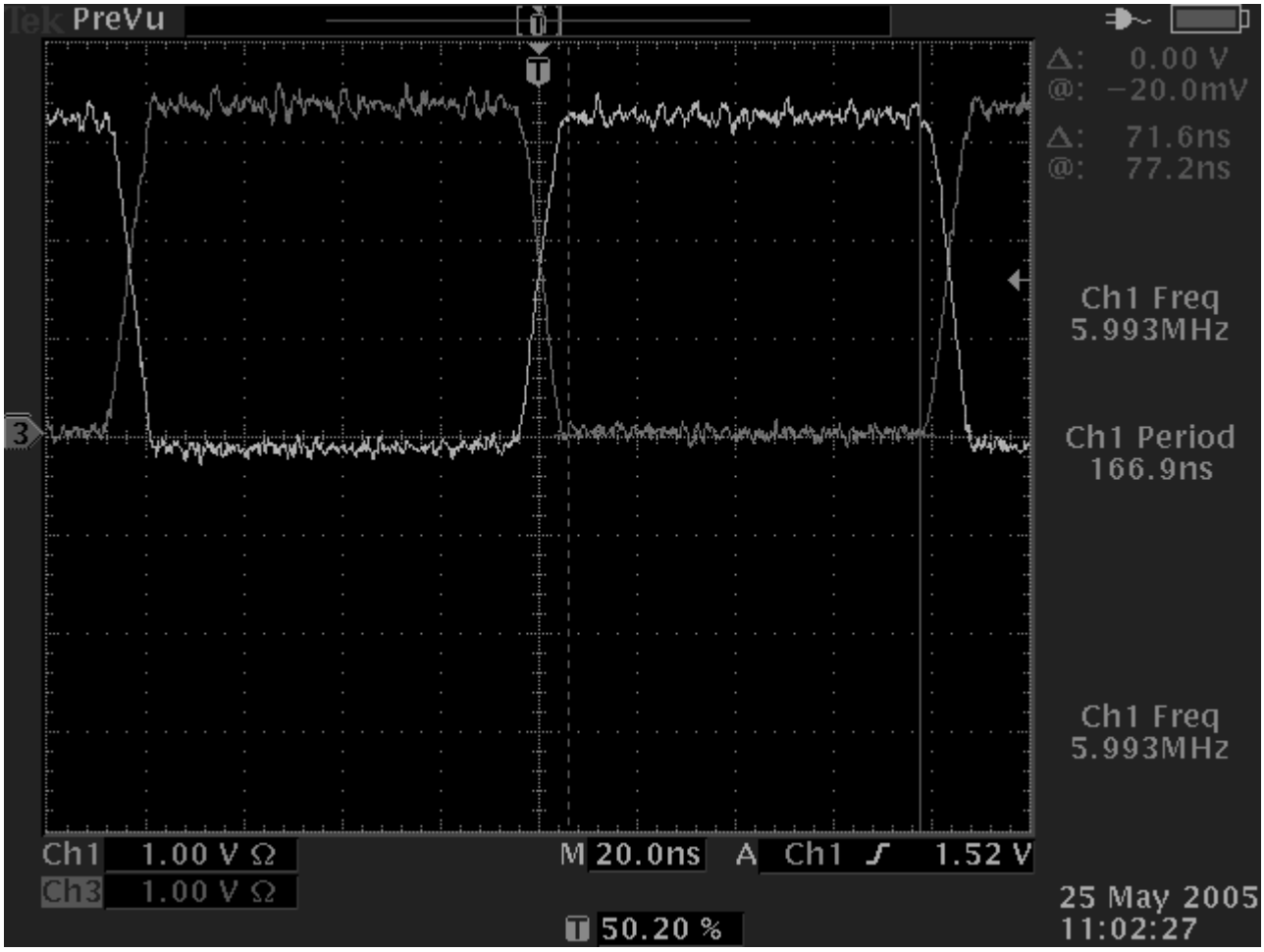
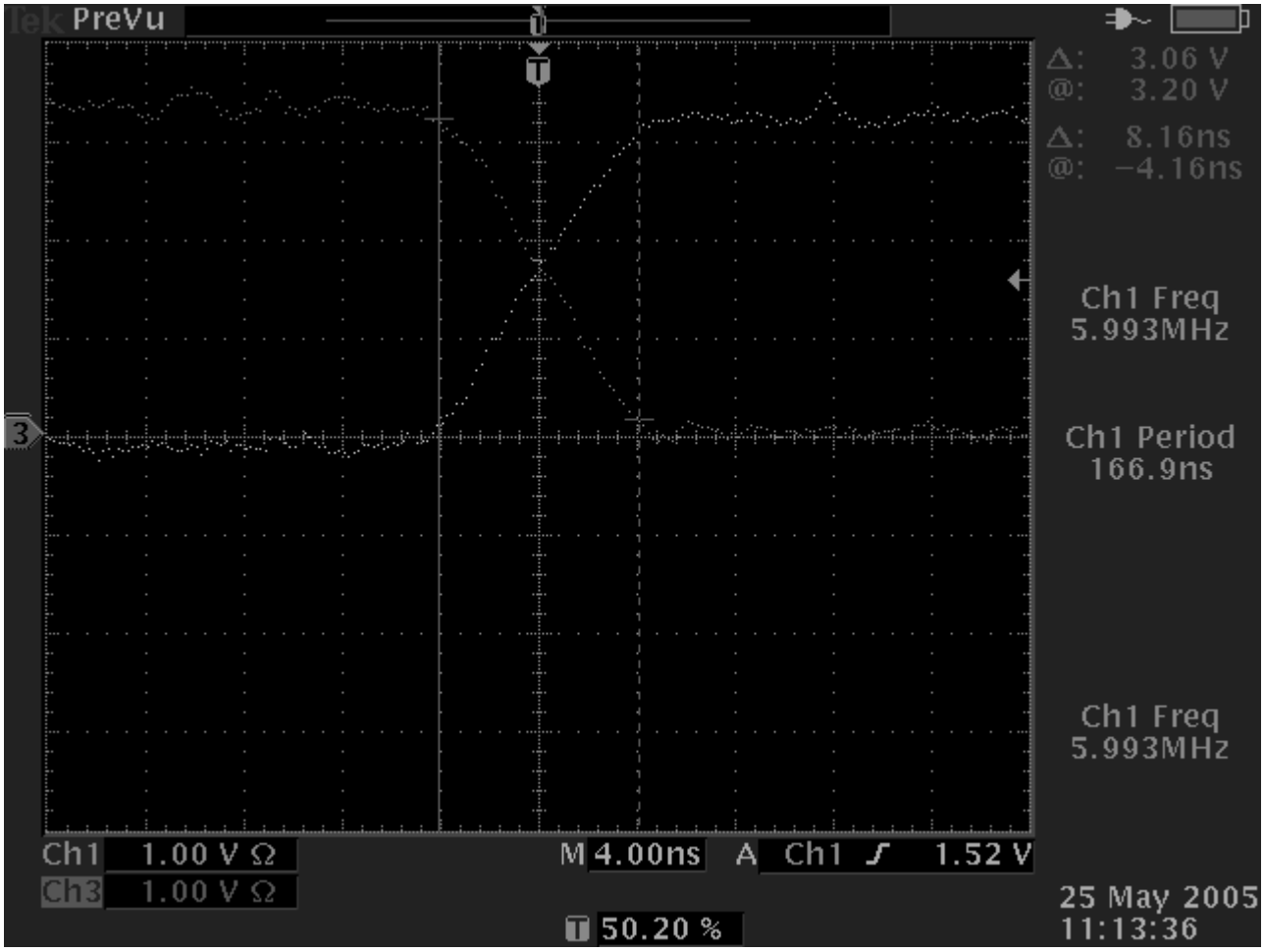


Figure 3.4 – USB, Differential EYE Diagram for Data Port Minus and Plus (DM0 and DP0)



3.4 – USB Differential driver switching Time Diagram

Figure 4.
RS232 related plots.

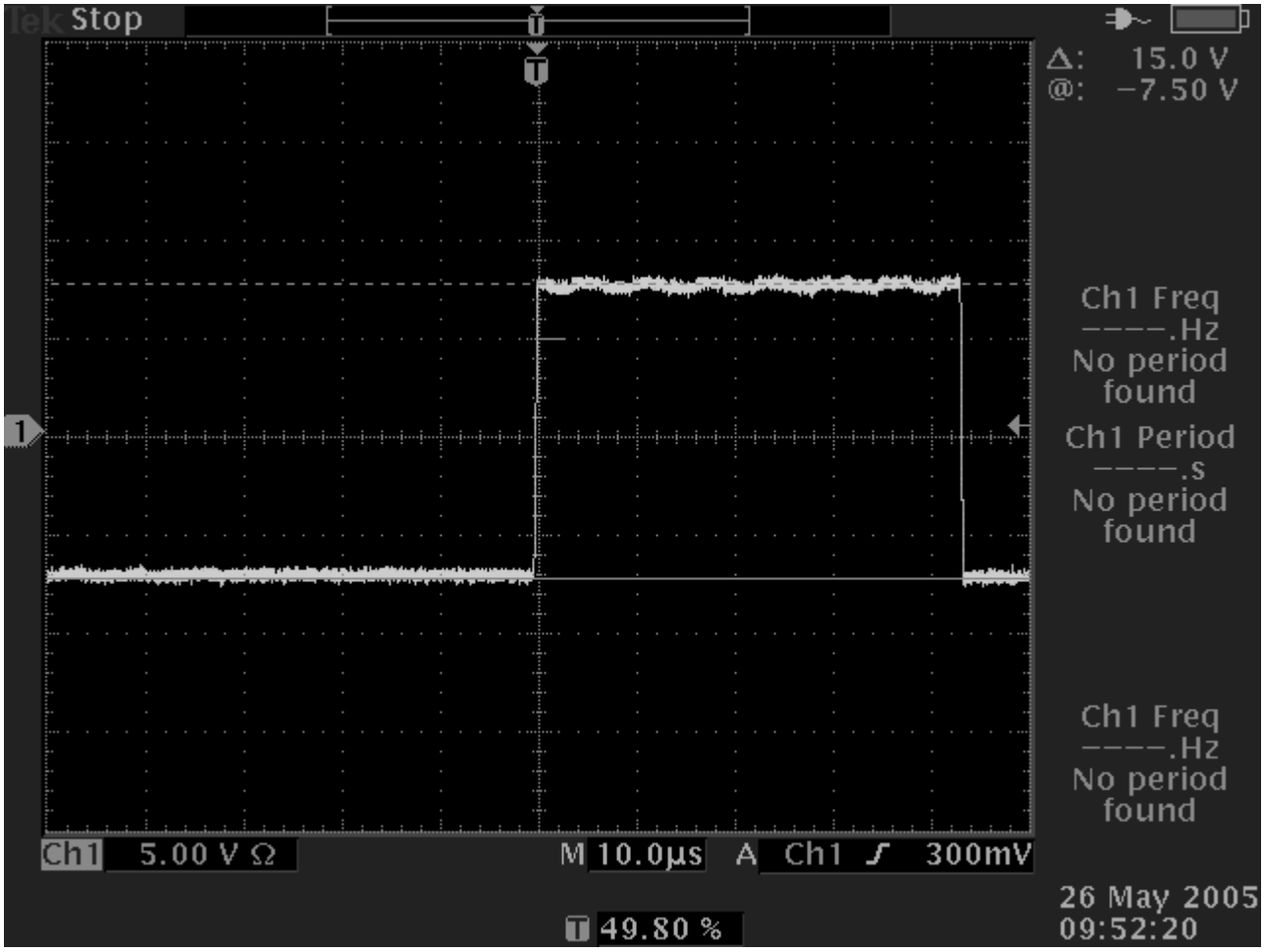


Figure 4.1 – RS232 TXD signal
The above scope shot is of the transmit data that the Digi Connect Core 9W was looping back during a test. This data is going into the development board from the 232 Transceiver.

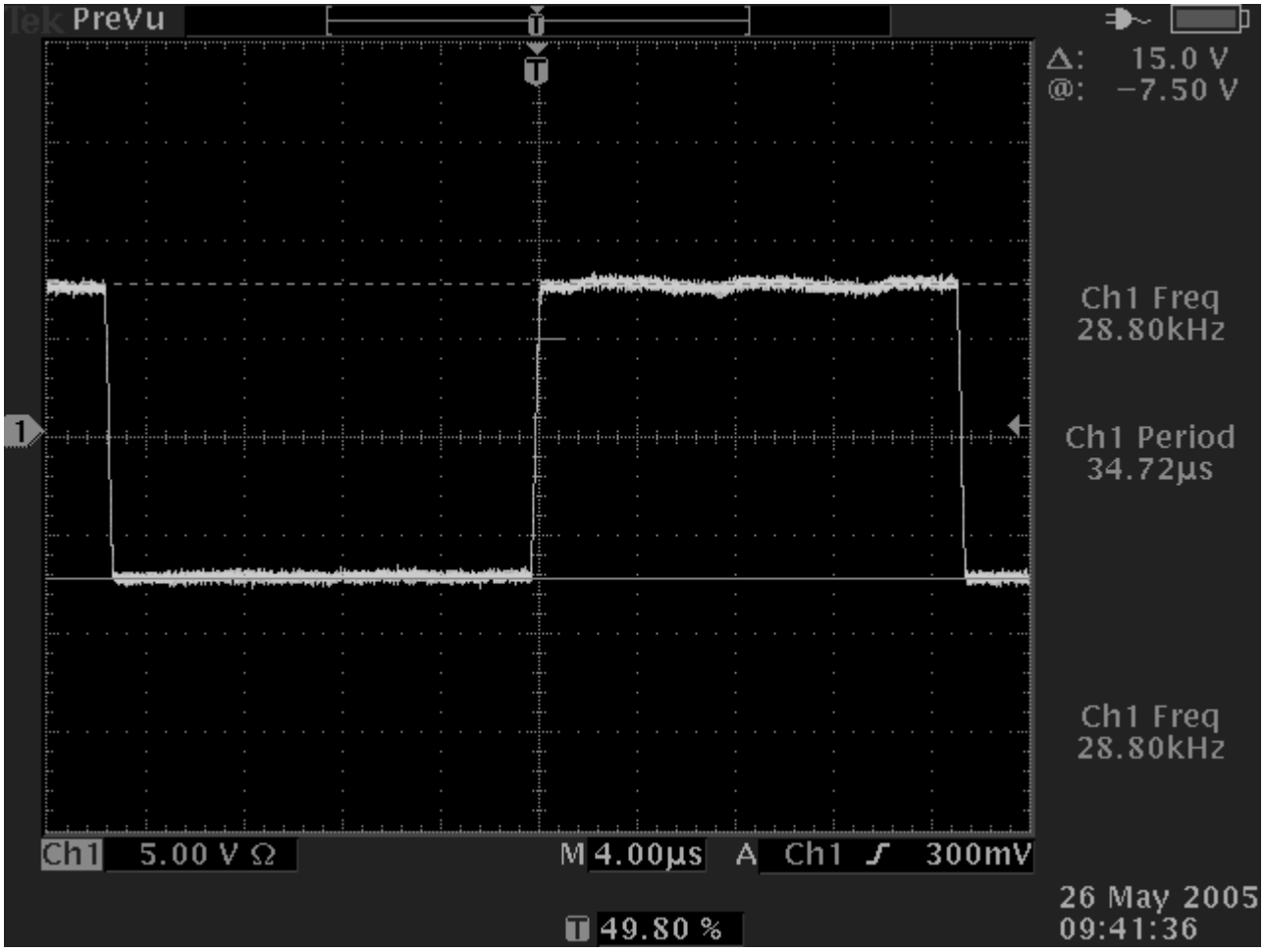


Figure 4.2 – RS232 RXD signal

The above scope shot is of the received data that the Digi Connect Core 9W was looping back during a test. This data is coming from the development board from the 232 Transceiver.