About the Development Board

CHAPTER 2

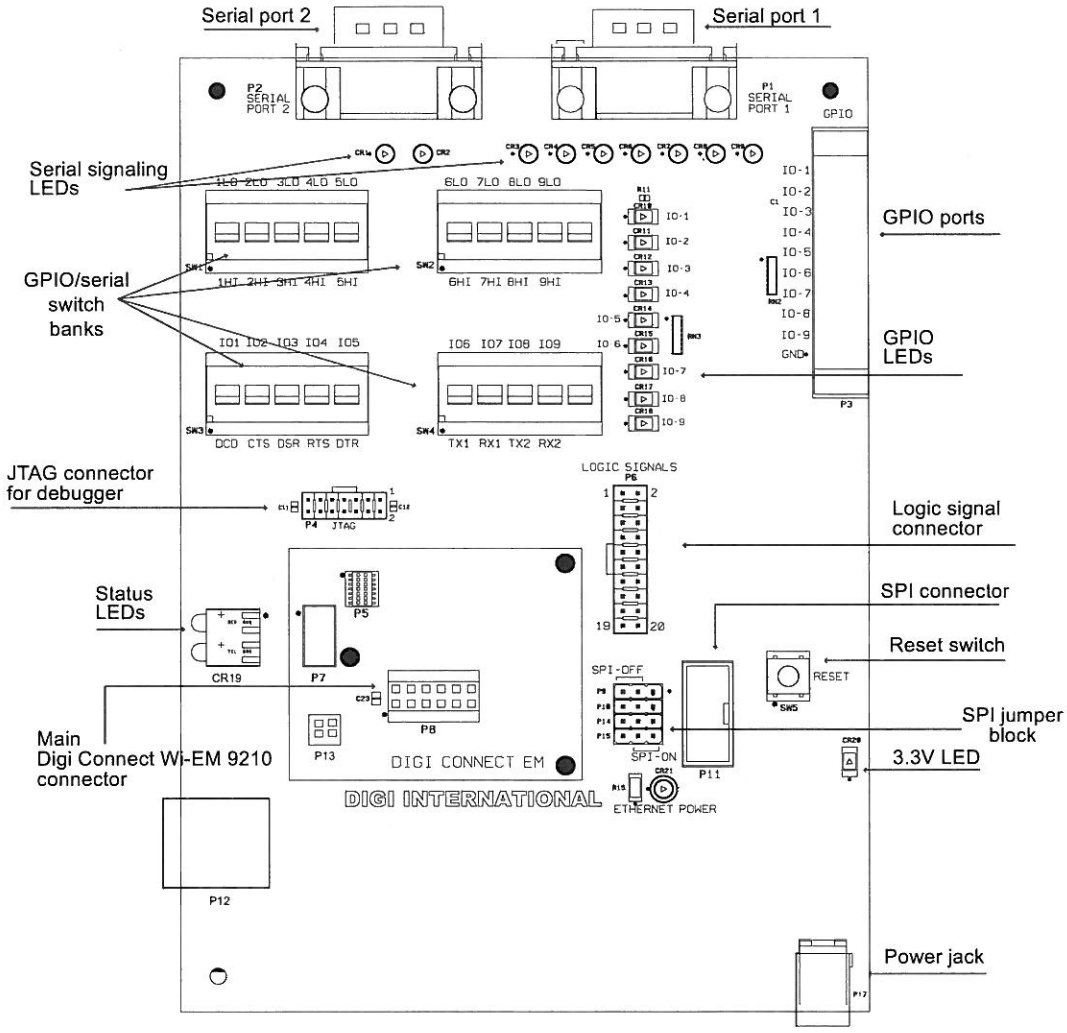
Overview

This chapter provides information on the development board, a hardware platform from which you can determine how to integrate the embedded module into your design. For additional information, see the schematic and mechanical drawings.

Basic Description

The following graphic is a layout of the development board.

Basic Description



Ports

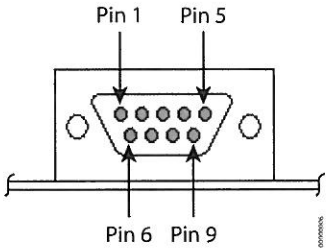
The development board provides the following ports:

- Serial Port 1 (P1) and Serial Port 2 (P2)
- Ethernet Port (P12)
- GPIO Port (P3)

Serial Port 1 (P1) and Serial Port 2 (P2)

Serial port 1 and port 2 are DB-9 male connectors labeled P1 and P2. Use the following figure and table for pin orientation and pin assignment information.

Serial Port Pin Orientation

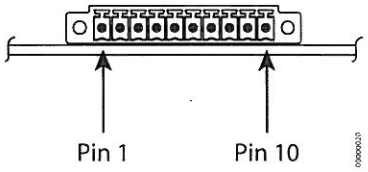


Serial Pin Assignment									
Port	**Signal Pin 1**	**Signal Pin 2**	**Signal Pin 3**	**Signal Pin 4**	**Signal Pin 5**	**Signal Pin 6**	**Signal Pin 7**	**Signal Pin 8**	**Signal Pin 9**
1	DCD	RXD	TXD	DTR	GND	DSR	RTS	CTS	Not Connected
2	Not Connected	RXD	TXD	Not Connected	GND	Not Connected	Not Connected	Not Connected	Not Connected

GPIO Port (P3)

The GPIO port is a 10-pin male right-angle connector (labeled P3). See the following figure and table for pin orientation and pin assignments.

GPIO Port Pin Orientation



GPIO Port Pin Assignments	
Pin	**Signal Name**
1	GND
2	GPIO-9
3	GPIO-8
4	GPIO-7
5	GPIO-6
6	GPIO-5
7	GPIO-4
8	GPIO-3
9	GPIO-2
10	GPIO-1

Connectors and Blocks

The development board provides the following connectors and blocks:

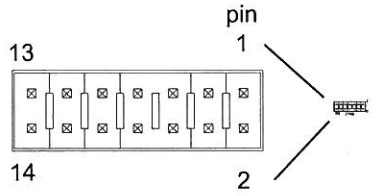
- JTAG Debugger Connector (P4)
- SPI Connector (P11) and SPI Jumper Block

- Logic Signal Analyzer Header (P6)
- Main Connector (P8)

JTAG Debugger Connector (P4)

This 14-pin male vertical header labeled P4 mates with a JTAG debugger plug (for example, a Digi JTAG Link). It is used with the development kit only. See the following figure and table for pin orientation and assignments.

JTAG Debugger Connector Pin Orientation

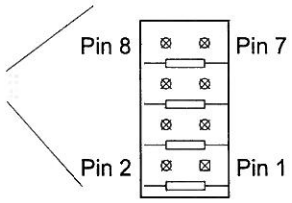


JTAG Debugger Connector Pin Assignments														
	Pin 1	**Pin 2**	**Pin 3**	**Pin 4**	**Pin 5**	**Pin 6**	**Pin 7**	**Pin 8**	**Pin 9**	**Pin 10**	**Pin 11**	**Pin 12**	**Pin 13**	**Pin 14**
Signal	VCC+	GND	/TRST	GND	TDI	GND	TMS	GND	TCK	GND	TDO	/SRST	VCC+	GND

SPI Connector (P11)

This connector is used for a Serial Peripheral Interface (SPI) connection. When enabled, signals are disconnected from serial port 1 and GPIO connectors. See the following figure and table for pin orientation and pin assignments.

SPI Connector Pin Orientation



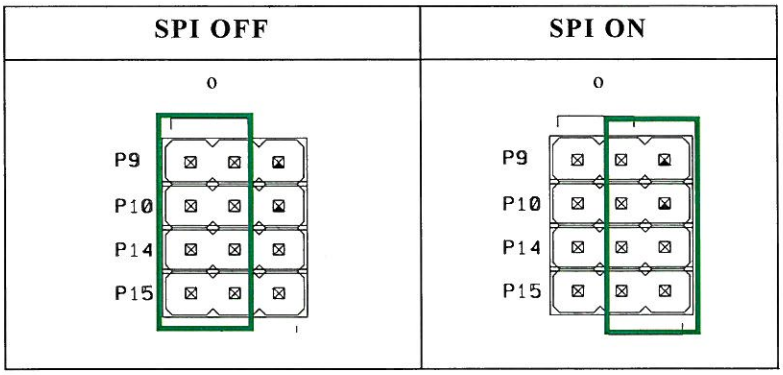
SPI Pin Assignments										
	Pin 1	**Pin 2**	**Pin 3**	**Pin 4**	**Pin 5**	**Pin 6**	**Pin 7**	**Pin 8**	**Pin 9**	**Pin 10**
Signal	SPI-EN	GND	SPI-CLK	GND	SPI-TX	GND	SPI-RX	GND	Not connected	Not connected

SPI Jumper Block

The SPI jumper block determines whether the SPI connector is connected or not. If SPI is off (the default), serial and GPIO signals are routed to switch banks 1 through 4. (See "Serial/GPIO Switch Bank 3 (SW3) and Switch Bank 4 (SW4)" on page 26 and "GPIO Switch Bank 1 (SW1) and 2 (SW2)" on page 27.) If SPI is on, SPI signals are routed to the SPI connector (P11).

The following figures demonstrate how to set the SPI jumper block

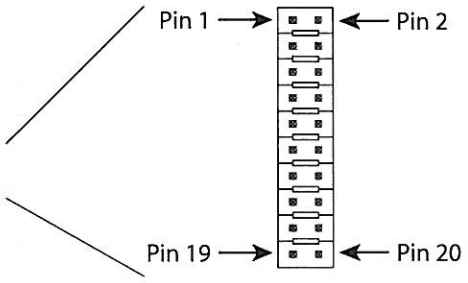
SPI Jumper Settings



Logic Signal Analyzer Header (P6)

This 20-pin male vertical header (labeled P6) connects a digital signal analyzer (for example, a logic analyzer) to the development board. It is used with the development kit only. See the following figure and table for pin orientation and pin assignments.

Logic Analyzer Header Pin Orientation



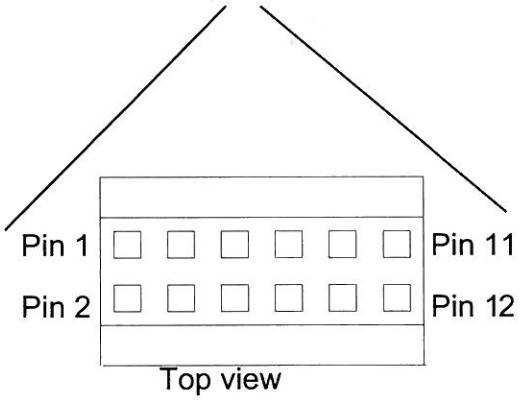
Logic Analyzer Header Pin Assignments	
Pin	**Signal**
1 - 8	Not connected

Logic Analyzer Header Pin Assignments	
Pin	**Signal**
9	/RST
10	Not connected
11	DTR/GPIO-5
12	TXD-2/GPIO-8
13	CTS/GPIO-2
14	RXD-2/GPIO-9
15	DSR/GPIO-3
16	TXD-1/GPIO-6
17	RTS/GPIO-4/SPI_CLK
18	RXD-1/GPIO-7
19	DCD/GPIO-1/SPI_EN
20	GND

Main Connector (P8)

This 12-pin connector is used to interface with the embedded module. See the following figure for pin orientation.

Main Connector Pin Orientation



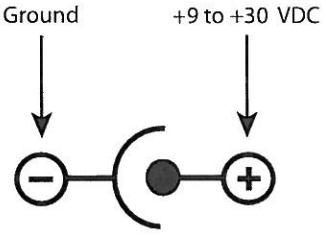
Power Jack (P17)

The Power Jack is a barrel connector that accepts 9 to 30 VDC +/- 5%. The jack is labeled P17. The following table shows the polarity of the power jack.

Power Jack Polarity	
Contact	**Polarity**
Center	+9 to +30 VDC
Outer	Ground

The following figure schematically represents the polarity of the power jack

Power Jack Polarity Schematic.



Switches

The development board provides the following switches:

- Reset Switch (SW5)
- Serial/GPIO Switch Bank 3 (SW3) and Switch Bank 4 (SW4)
- GPIO Switch Bank 1 (SW1) and 2 (SW2)

Reset Switch (SW5)

This push button switch is labeled SW5. Pressing it sets the module's /RST line low, holding the module in a hard reset until the switch is released.

Note: This is a "hard" reset using the /RST pin on the main connector, not a "soft" reset. The reset button on the embedded module performs a "soft" reset (see also "Main Connector (P8)" on page 24).

Serial/GPIO Switch Bank 3 (SW3) and Switch Bank 4 (SW4)

Each switch bank holds five slide switches that enable either serial or GPIO signaling between the development board and the module. When set for GPIO signaling, SW3 works in conjunction with SW1, and SW4 works with SW2. See "GPIO Switch Bank 1 (SW1) and 2 (SW2)" on page 27 for more information. See the following table for SW3 and SW4 switch definitions.

Note: These switches control where the development board routes a signal. They do not reconfigure the Wi-EM 9210 processor. Software should be configured to track with switch settings. See "GPIO" on page 33 for more information.

GPIO Switch Banks 3 and 4 Settings			
Switch Bank	**Switch Number**	**Left Position**	**Right Position**
SW3	1	DCD	GPIO-1
	2	CTS	GPIO-2
	3	DSR	GPIO-3
	4	RTS	GPIO-4
	5	DTR	GPIO-5
SW4	6	TXD-1	GPIO-6
	7	RXD-1	GPIO-7
	8	TXD-2	GPIO-8
	9	RXD-2	GPIO-9
	10	Not connected	Not connected

GPIO Switch Bank 1 (SW1) and 2 (SW2)

GPIO Switch Bank 1 and Switch Bank 2, labeled SW1 and SW2, are two sets of five slide switches that set GPIO inputs to logic levels of high (switch to left) or low (switch to right).

If the GPIO port is configured as an output, then the switch should always be to the left. If there is an external device connected to P3, the switch should always be set to the left.

Each GPIO port can be used independently.

Notes:

- These switches do not determine whether the GPIO is an input or output. That is determined by the module software.
- If GPIO is set to an output by software, switches must be set to the left (high).
- These switches are used in conjunction with SW3 and SW4.

Development Board LEDs

The development board contains 21 LEDs labeled CR1 through CR21. The following table lists and describes the LEDs.

LED Descriptions			
Board Label	**Description**	**Color or State**	**Indication**
CR1	TXD-2	Flickering	Serial activity
		Green	Inactive
CR2	RXD-2	Flickering	Serial activity
		Green	Inactive
CR3	CTS	Yellow	Active
		Green	Inactive
		Off	Not connected or signal not being driven
CR4	DTR	Yellow	Active
		Green	Inactive
		Off	Not connected or signal not being driven
CR5	TXD-1	Flickering	Serial activity
		Green	Inactive
CR6	RXD-1	Flickering	Serial activity
		Green	Inactive
CR7	RTS	Yellow	Active
		Green	Inactive
		Off	Not connected or signal not being driven

LED Descriptions			
Board Label	**Description**	**Color or State**	**Indication**
CR8	DCD	Yellow	Active
		Green	Inactive
		Off	Not connected or signal not being driven
CR9	DSR	Yellow	Active
		Green	Inactive
		Off	Not connected or signal not being driven
CR10 -18	GPIO-1 through GPIO-9. (CR10=GPIO-1, CR11=GPIO-2, etc. All can be used for input or output.)	On	Logic high
		Off	Logic low
CR20	3.3V Indicator	On	Power on
		Off	Power off
CR21	EPWR, Powered Ethernet Enabled	On	Ethernet power present from external powered Ethernet connector (Ethernet hub or switch)
		Off	No powered Ethernet voltage

Test Points

The development board provides 25 test points that can be identified by board label or test point number. The board labels are adjacent to each test point on the board. The test point numbers are in the development board schematic drawings. The following table lists the test point number, board label, and a brief description of each test point.

Test Point Descriptions		
Test Point	**Board Label**	**Description**
TP2	TXD	TXD-2
TP3	RXD	RXD-2
TP4	CTS	CTS
TP5	DTR	DTR
TP6	TXD	TXD-1
TP7	RXD	RXD-1
TP8	RTS	RTS
TP9	DCD	DCD
TP10	DSR	DSR
TP11	IO-1	GPIO-1
TP12	IO-2	GPIO-2
TP13	IO-3	GPIO-3
TP14	IO-4	GPIO-4
TP15	IO-5	GPIO-5
TP17	3.3V	3.3V Supply
TP20	RESET	Reset (active low)
TP21	E+	Ethernet Power +
TP22	E-	Ethernet Power -
TP23	V-IN	9-30 VDC Input
TP24	GND	Ground
TP25	GND	Ground
TP26	IO-8	GPIO-8
TP27	IO-7	GPIO-7

Test Point Descriptions		
Test Point	**Board Label**	**Description**
TP28	IO-6	GPIO-6
TP29	IO-9	GPIO-9

Test Points