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802.11a/b/g MiniPCI Module
Project Number: T60H677.03

Theory of Operations

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0. Revision History

Date	Change Note	REV Note
Feb 7, 2003	1st Rev.	0

1. Introduction

Project Name: 802.11a/b/g MiniPCI Module
Project Number: T60H677.03

This documentation describes the Theory of Operations of the 802.11a/b/g MiniPCI Module. It is a confidential document of AMBIT.

2 Function

Wireless LAN Function

- 802.11a circuit of MiniPCI Module compatible with IEEE 802.11a standard
- 802.11g circuit of MiniPCI Module compatible with IEEE 802.11g high rate draft standard to provide wireless Ethernet speeds of 54Mbps data rate
- Dynamic data rate switching with 54, 48, 36, 24, 18, 12, 9, 6Mbps
- Support wireless data encryption with 64/128/152-bit WEP standard for security
- Allows auto fallback data rate for optimized reliability, throughput and transmission range.
- Supports Ad-hoc mode (peer-peer) and Infrastructure mode (client-server) communications.
- Dual diversity antenna connectors supported for the multi-path environment. Drivers supports Windows 98SE, ME, 2000, XP

3 Functional Hardware Specifications

802.11a

Wireless LAN Compliance	IEEE 802.11a
Operating Frequency	5.15~5.25GHz (lower band) for US/Canada/Japan 5.25~5.35GHz (middle band) for US/Canada 5.725~5.825GHz (high band) for US
Modulation Schemes	OFDM, QPSK, BPSK,16-QAM and 64-QAM
WLAN Data Rate	54Mbps with fall back rates of 48, 36, 24, 18, 12, 9, and 6Mbps
Media Access Protocol	CSMA/CA with ACK

802.11b/g

Radio Technology	IEEE 802.11g draft standard compliant
Operating Frequency	2412 ~ 2484MHz ISM band
Modulation Schemes	OFDM, DQPSK, DBPSK, CCK, 64QAM, 16QAM, QPSK, BPSK
Channel Numbers	11 channels for United States 13 channels for Europe Countries 14 channels for Japan
Data Rate	54Mbps with fall back rates of 48, 36, 24, 18, 12, 9, and 6Mbps
Media Access Protocol	CSMA/CA with ACK

4 Hardware Architecture

The WLAN module design is based on the Atheros AR5001 802.11a/b/g chip set.

The Atheros WLAN chips include the AR5111 Radio-On-a-Chip(ROC), the AR2111 Radio Front End, and the AR5212 MAC/BBP. When combined with external LNA's, PA's, RF filters, and diversity switches, these chips produce an IEEE 802.11a/b/g-compliant WLAN platform.

5GHz Single-Chip Radio Transceiver (AR5111)

The AR5111 is an integrated 5GHz CMOS radio transceiver that operates in (1) the 5.15~5.35GHz and 5.725~5.825GHz U-NII frequency bands; and (2) the 5.15 to 5.35GHz and the 5.47 to 5.725GHz European bands.

It offers a fully integrated transceiver with a Power Amplifier, and eliminates the need for an external VCO & SAW Filters. The chip also supports connection to output power boosters and external LNA's for higher performance. The transceiver core, digital logic, and VCO are powered by 2.5V. The I/O's are powered by 3.3V.

2.4GHz Single-Chip Radio Transceiver (AR2111)

The AR2111 is an integrated up/down-converter that operates in (1) the 2.412 to 2.472GHz U.S. frequency bands (2) the 2.484 Japanese band. The AR2111 transmitter takes the output of the AR5111 chip, down converts it to the 2.4GHz frequency band and drives the signal off-chip. The receiver up converts the 2.4GHz incoming signal to the 5GHz frequency band for the AR5111 input. The AR2111 core is powered by 2.5V, and the I/O's by 3.3V. The chip produces two LO frequencies 3.168 and 3.136GHz for its up and down conversion functions.

MAC/Baseband Processor (AR5212)

The AR5212 chip is an IEEE 802.11a/b/g compatible, highly integrated ASIC containing a PCI interface, DMA engine, baseband processor, PLL, ADC, and DAC. The AR5212 runs on a 2.5V (digital and analog) core, and 3.3V I/O.

The functional block diagram is shown in Figure 1.

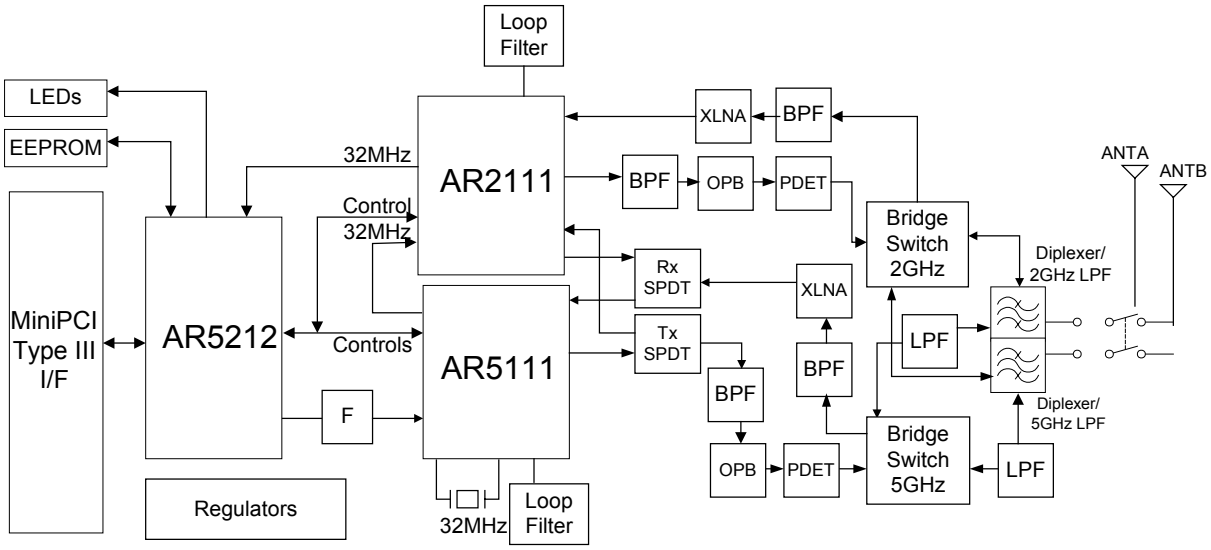

Figure 1 Functional Block Diagram

Diplexer

The diplexer is a three-port circuit designed to separate the 5GHz transceiver signals from the 2.4GHz transceiver signals. The separation is accomplished by creating a high pass filter for the 5GHz path (which effectively eliminates 2.4GHz signals), and a low pass filter for the 2.4GHz path (which effectively eliminates the 5GHz signals). There are two diplexers used in the design, one for each antenna port. The low pass section of each diplexer provides harmonic attenuation for 2.4GHz transmit operation.

Bridge Switches

The bridge switches are used to provide transmit and receive diversity operation. The 5GHz bridge switch is an off-the-shelf MMIC device. The 2.4GHz bridge switch is comprised of four pin diode switches arranged in a closed ring configuration. Four control signals from the AR5212 chip (two for each switch) are used to configure the switches for appropriate operation.

Receive Filtering

5GHz BPF: The purpose of this filter is to reject spurious and image frequency signals before they enter the 5GHz receive chain.

2GHz BPF: The purpose of this filter is to reject spurious and image frequency signals before they enter the 2.4GHz receive chain.

Low Noise Amplifiers

5GHz LNA / 2.4GHz LNA: The LNA's provide additional gain to the 5GHz and 2.4GHz receiver chains and reduce the overall system noise figure. They are powered off and on via individual control signals from the AR5212 chip.

Receive Switch (Rx SPDT)

The purpose of this switch, a standard pin diode SPDT configuration, is to choose the signal path routing for the incoming receive signal. For 5GHz receive mode, the switch is configured to route the signal from the external 5GHz LNA output to the AR5111 receive input. For 2.4GHz receive mode, the switch is configured to route the signal from the up-converted AR2111 output to the AR5111 receive input. The switch configuration is controlled via two control signals from the AR5212 chip.

Transmit Filtering

5GHz BPF: The purpose of this filter is to attenuate harmonics and LO leakage from the AR5111 chip.

5GHz LPF: The purpose of this filter (one in each diversity path) is to reject harmonics and other spurious emissions from the output power booster.

2.4GHz BPF: The purpose of this filter is to attenuate harmonics and LO leakage from the AR2111 chip.

Output Booster

5GHz OPB / 2.4GHz OPB: The output power boosters provide additional amplification for their respective transmit chains. These devices permit the output power levels of the integrated AR5111 and AR2111 power amplifiers to be reduced, thereby improving the overall linear output power capability of the system. Each booster is powered off and on via individual control signals from the AR5212 chip.

Coupler Detector

The 5GHz Tx path and the 2.4GHz Tx path each have their own printed power coupler and discrete-component detector circuits. During normal transmit operation, the couplers sample a small amount of the transmit energy (approximately -20dBc). These sampled signals are then envelope detected by a schottky diode and filtered to create a dc feedback voltage that is proportional to the system output power. The dc signals from the 2.4GHz and 5GHz detectors are summed together and fed to the AR5111 chip where they are used for power leveling and control.

Transmit Switch (Tx SPDT)

The purpose of this switch, an off-the-shelf MMIC device, is to choose the signal path routing for the AR5111 transmit signal. For 5GHz transmit mode, the switch is configured to route the AR5111 output to the external 5GHz transmit path. For 2.4GHz transmit mode, the switch is configured to route the AR5111 output to the AR2111 chip, where it is down-converted to 2.4GHz, and directed to the 2.4GHz transmit path. The switch configuration is controlled via two control signals from the AR5212 chip.

Loop Filter

The AR5111 and AR2111 each have external loop filters for their respective LO synthesizers. The loop filter components set the PLL bandwidths for optimum reference spur rejection, phase noise, and switching speed.

32MHz Crystal

The 32MHz crystal provides the core clock for the AR5111, AR2111, and AR5212. The crystal is attached to the AR5111, which has an on-chip oscillator. The AR5111 provides the oscillator output to its internal frequency synthesizer, and also provides a buffered version to the AR2111 chip. The AR2111 uses this 32MHz signal for its internal timing requirements and synthesizer reference, buffers the signal again, and directs it to the AR5212 where it serves as the system reference clock.

EEPROM

The EEPROM stores the AR5001 configuration information, PC Card tuples, and any OEM-specific data.

Voltage Regulators

Two voltage regulators are used to provide 2.5Vdc for the core voltages of the AR5111, AR2111, and AR5212.

DAC Filter (F)

External reconstruction filters are used between the AR5212 DAC outputs and the AR5111 inputs. The filters are a low-pass topology with a 20MHz cutoff frequency.