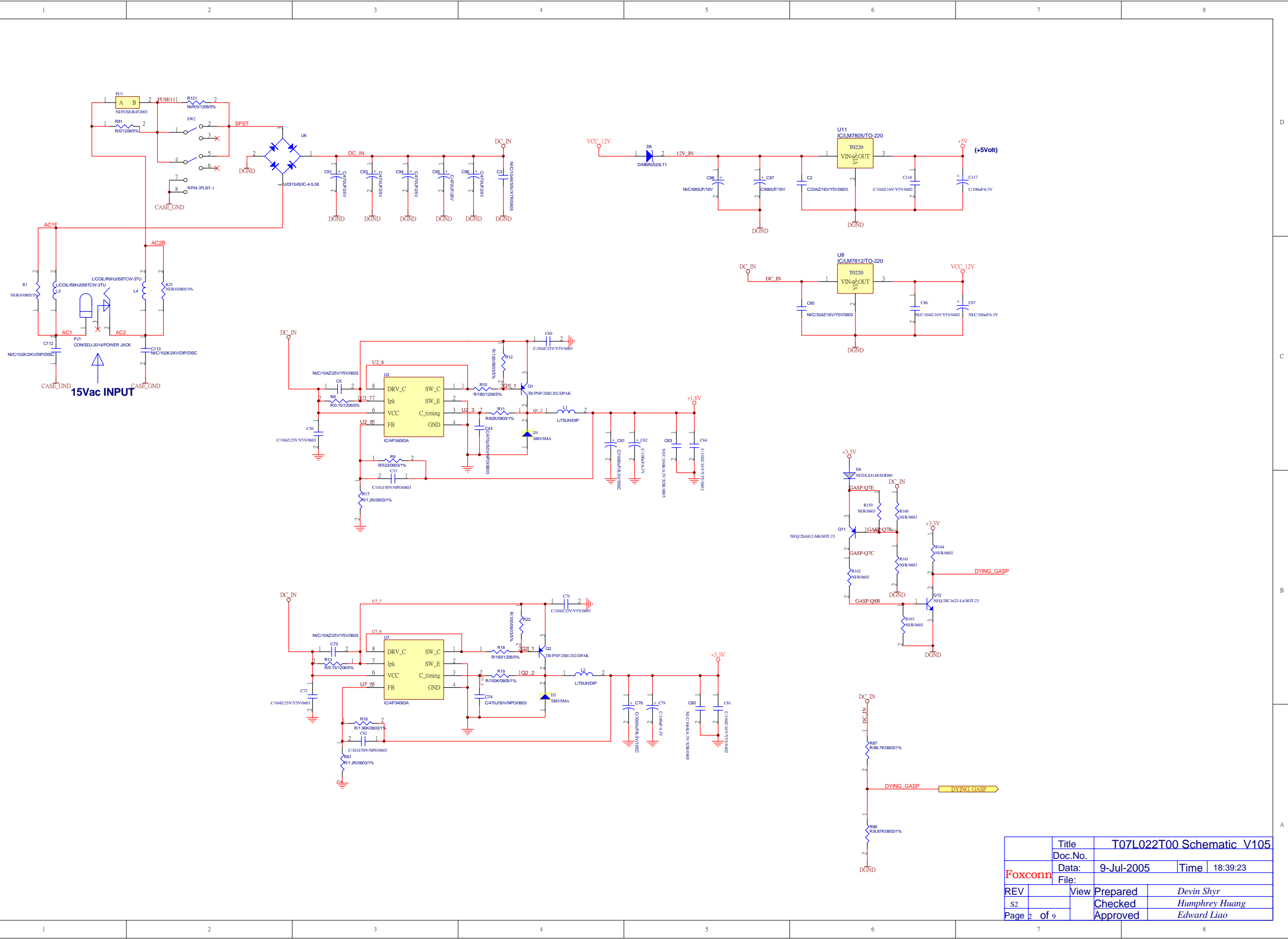
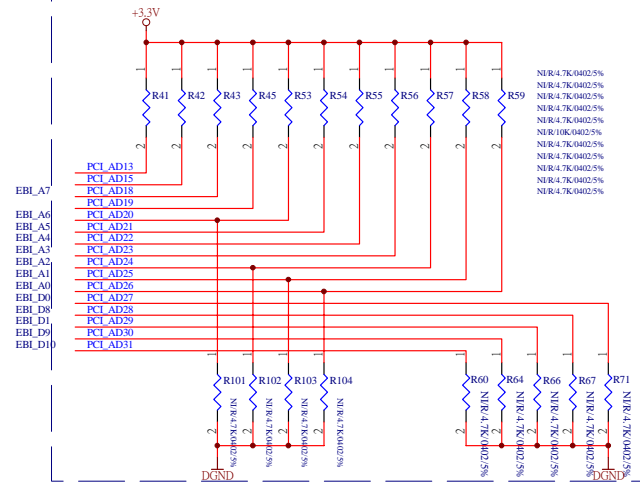


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	Doc.No.			
Foxconn	Date:	9-Jul-2005	Time	18:39:22
	File:			
REV	View	Prepared	Devin Shyr	
S2		Checked	Humphrey Huang	
Page	of 9	Approved	Edward Liao	

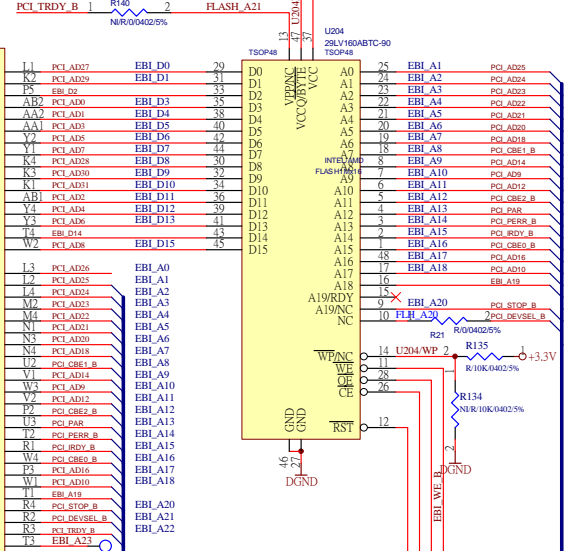
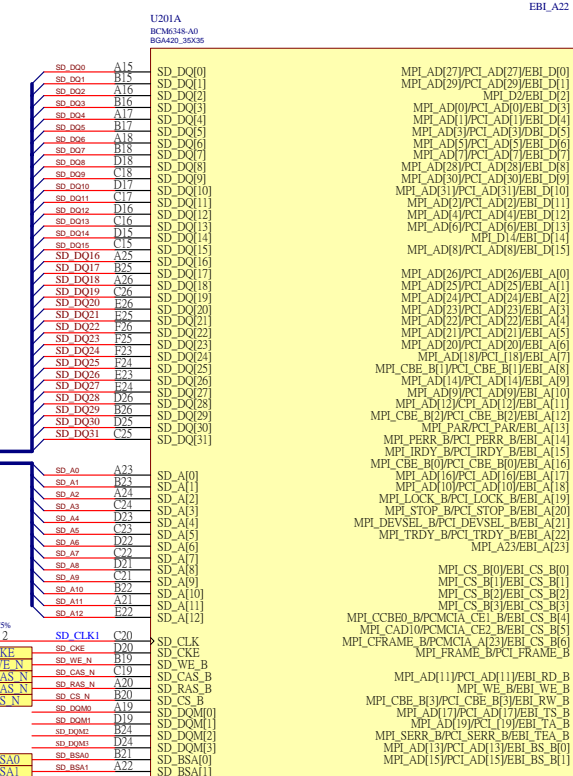
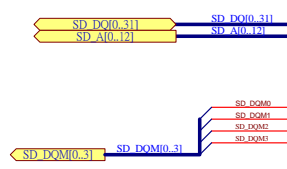


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Doc.No.			
Date:	9-Jul-2005	Time	18:39:23
REV	View	Prepared	Devin Shyr
S2		Checked	Humphrey Huang
Page 2	of 9	Approved	Edward Liao

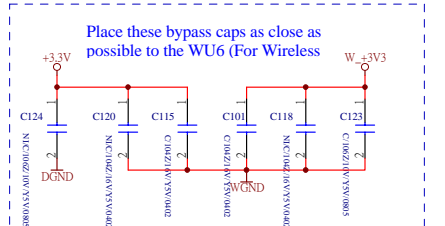
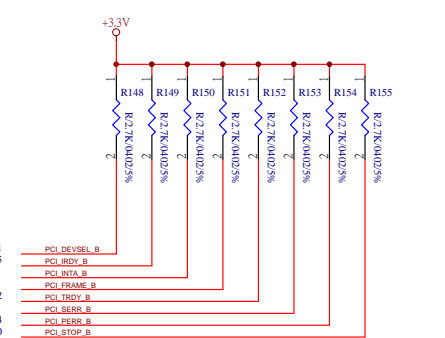
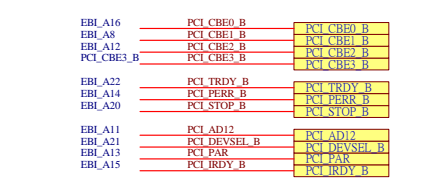
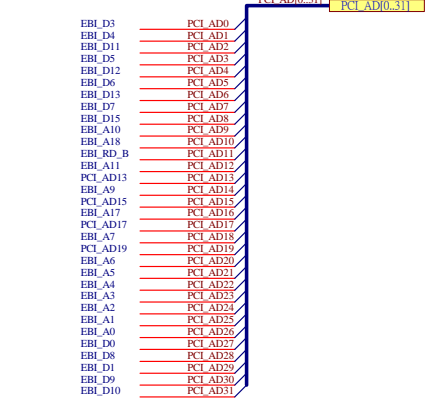
Power-On Strap Pins



- Flash Data Width 16-Bits
- MIPS Endian Mode Big Endian
- Utopia Clock Mode Internal Clock Mode
- PCI Arbiter Select Internal Arbiter
- SPI Fast Clock Mode Big Endian
- Internal MPI Mode Normal Mode
- SPI Flash Addressing Mode 24-Bits Serial Flash Address
- Boot Flash Mode Boot From Parallel Flash on the EBI Bus
- MIPS Reset Delay 16 Cycles
- MIPS Reset Delay 16 Cycles
- MIPS Asyn. Reset Mode MIPS Boots in Asyn. Mode
- PLL Clock Select Modes 240MHz MIPS, 133MHz SDRAM
- PLL Clock Select Modes 240MHz MIPS, 133MHz SDRAM
- PLL Clock Select Modes 240MHz MIPS, 133MHz SDRAM
- PLL Clock Select Modes 240MHz MIPS, 133MHz SDRAM

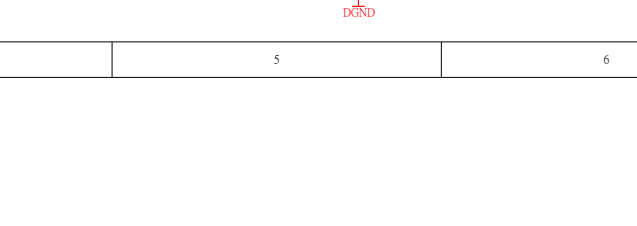
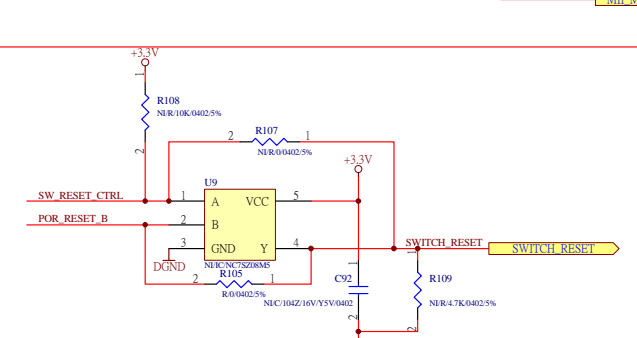
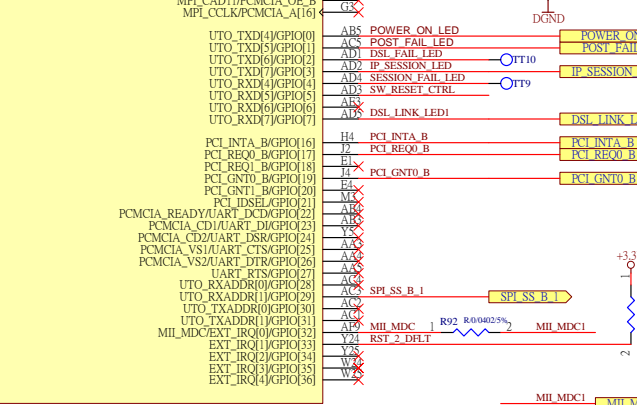
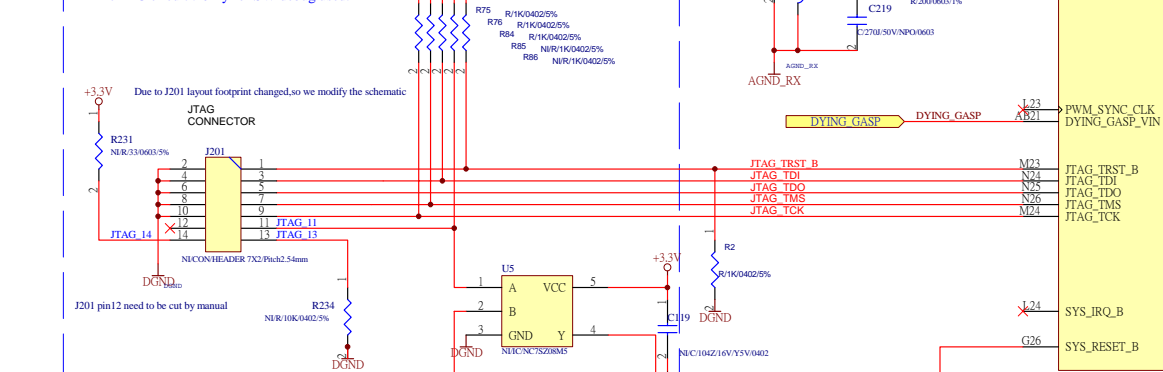


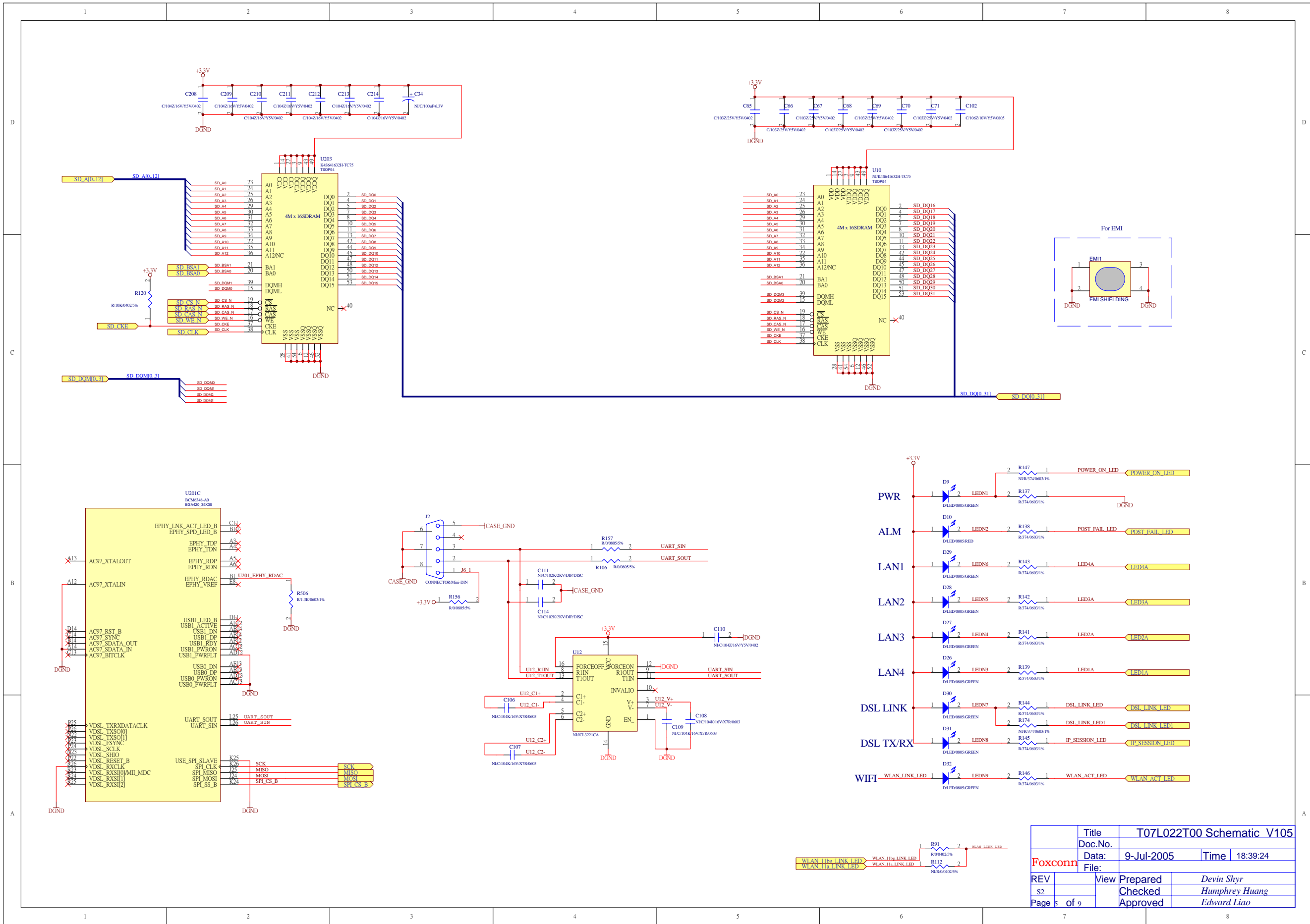
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R21	EQ	EQ	NE
R140	EQ	NE	NE
R134	NE	EQ	NE
R135	EQ	EQ	NE



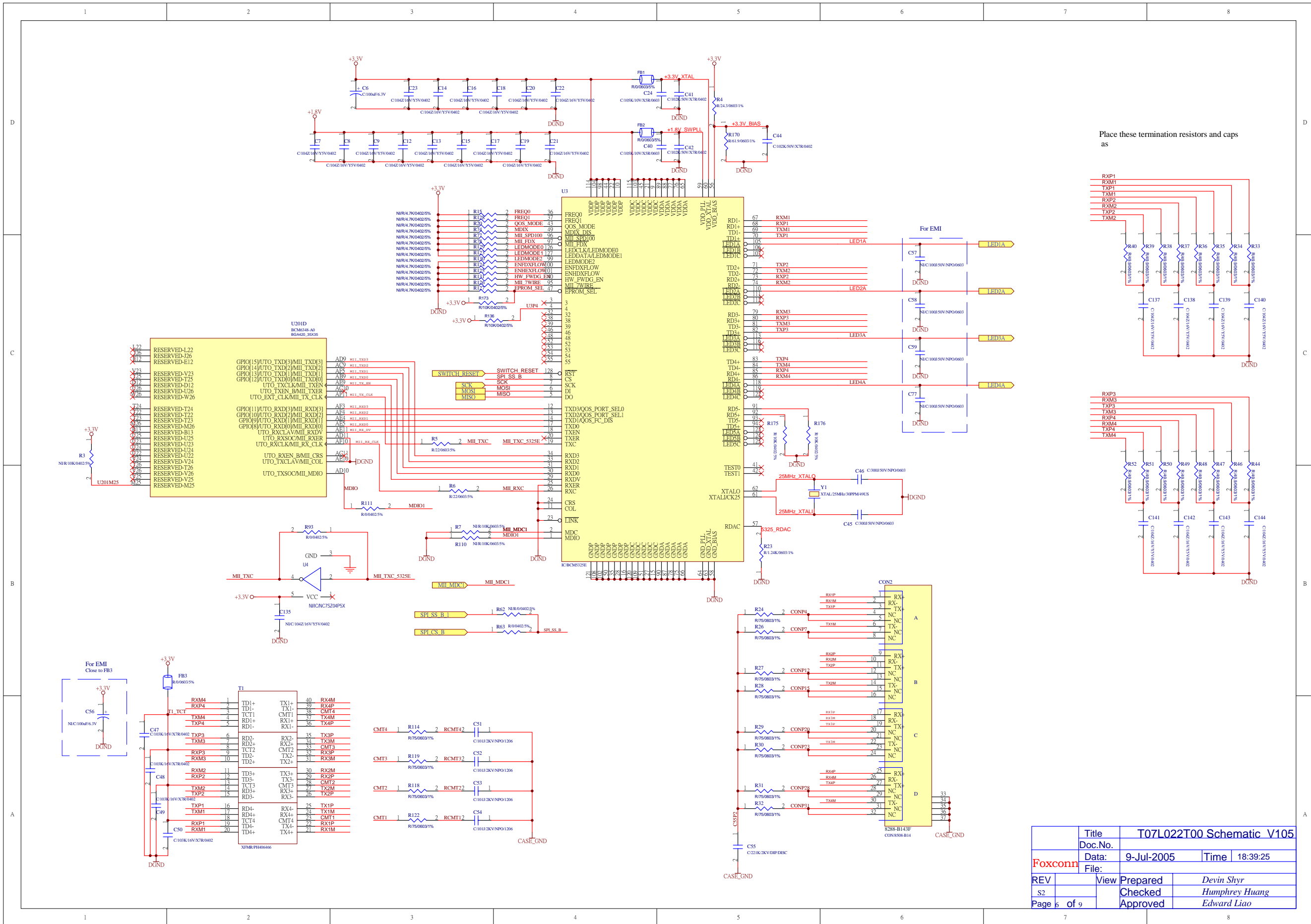
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Doc.No.			
Date:	9-Jul-2005	Time	18:39:24
File:			
REV	View	Prepared	Devin Shyr
S2	Checked	Humphrey Huang	
Page 4 of 9	Approved	Edward Liao	

JTAG circuit : Only for SW debug used.

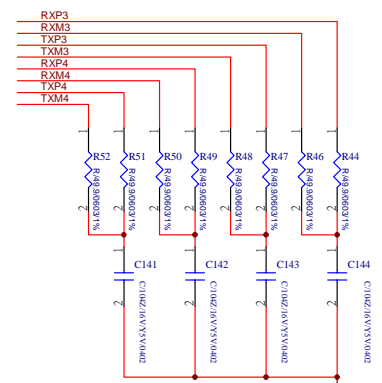
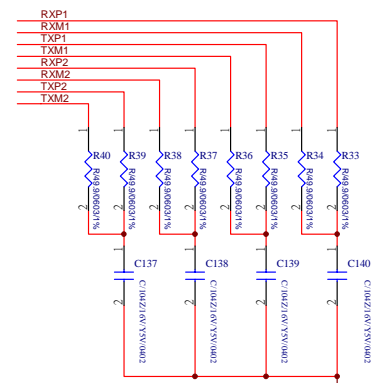




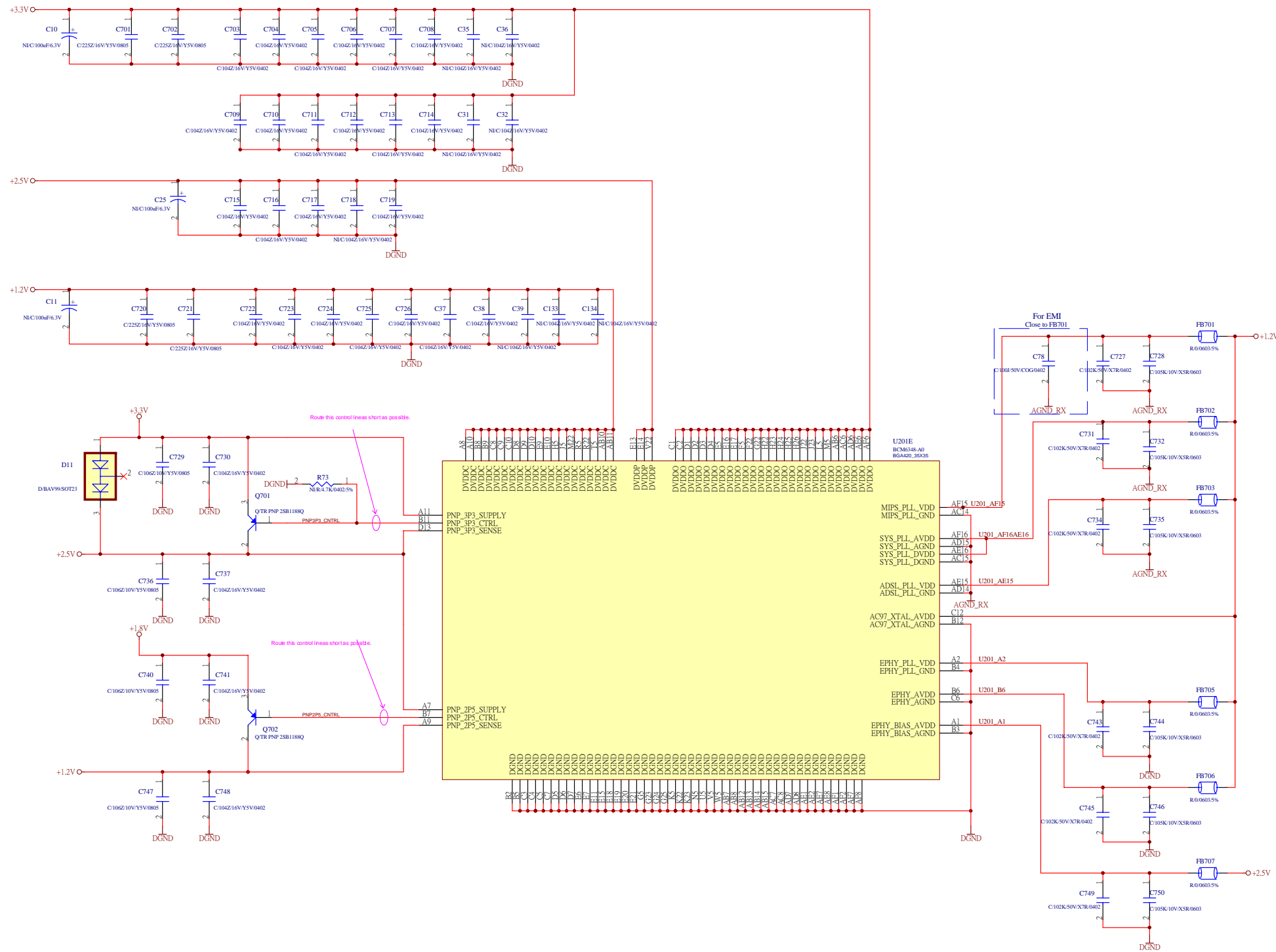
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Doc.No.			
Date:	9-Jul-2005	Time	18:39:24
File:			
REV	View	Prepared	Devin Shyr
S2	Checked	Humphrey Huang	
Page 5 of 9	Approved	Edward Liao	



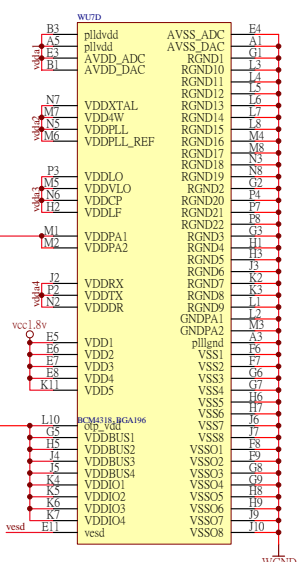
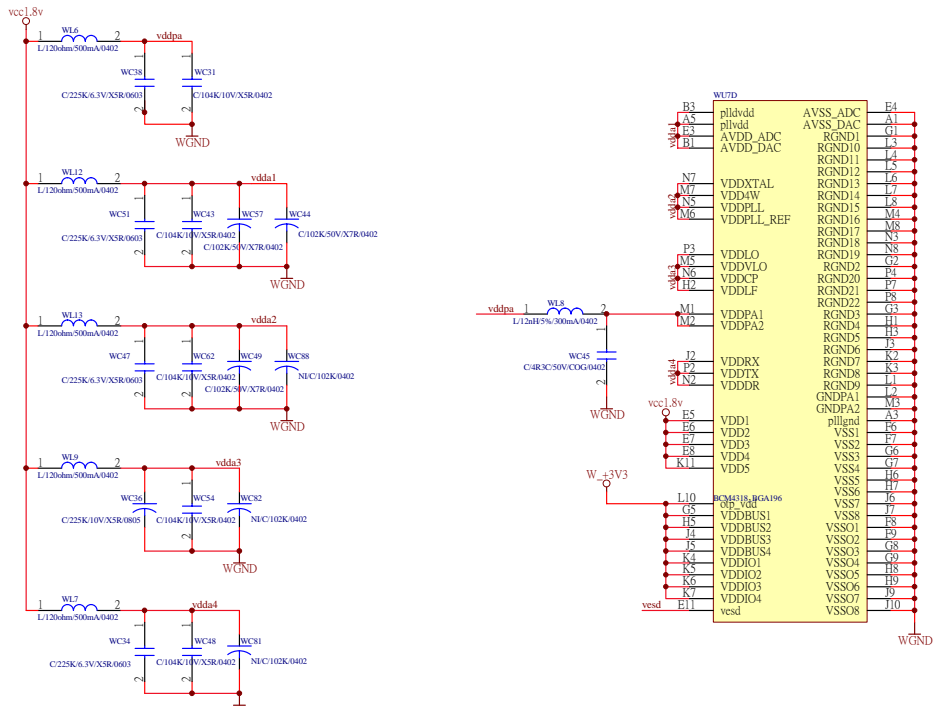
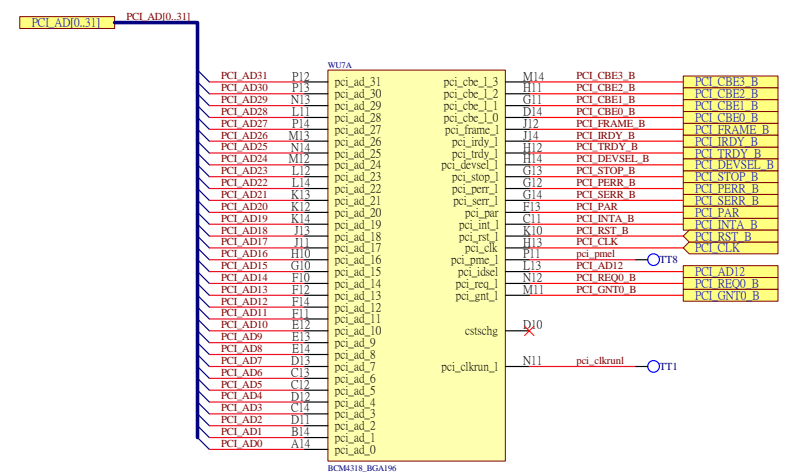
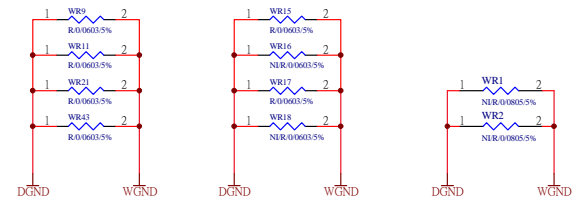
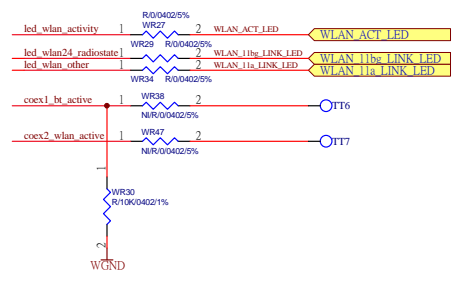
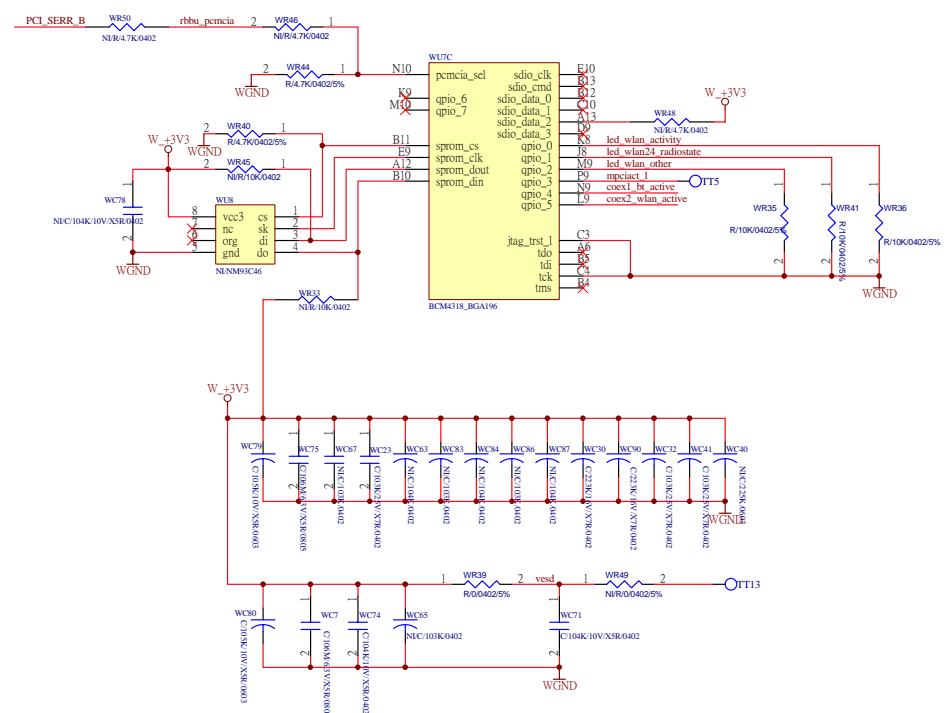
Place these termination resistors and caps as



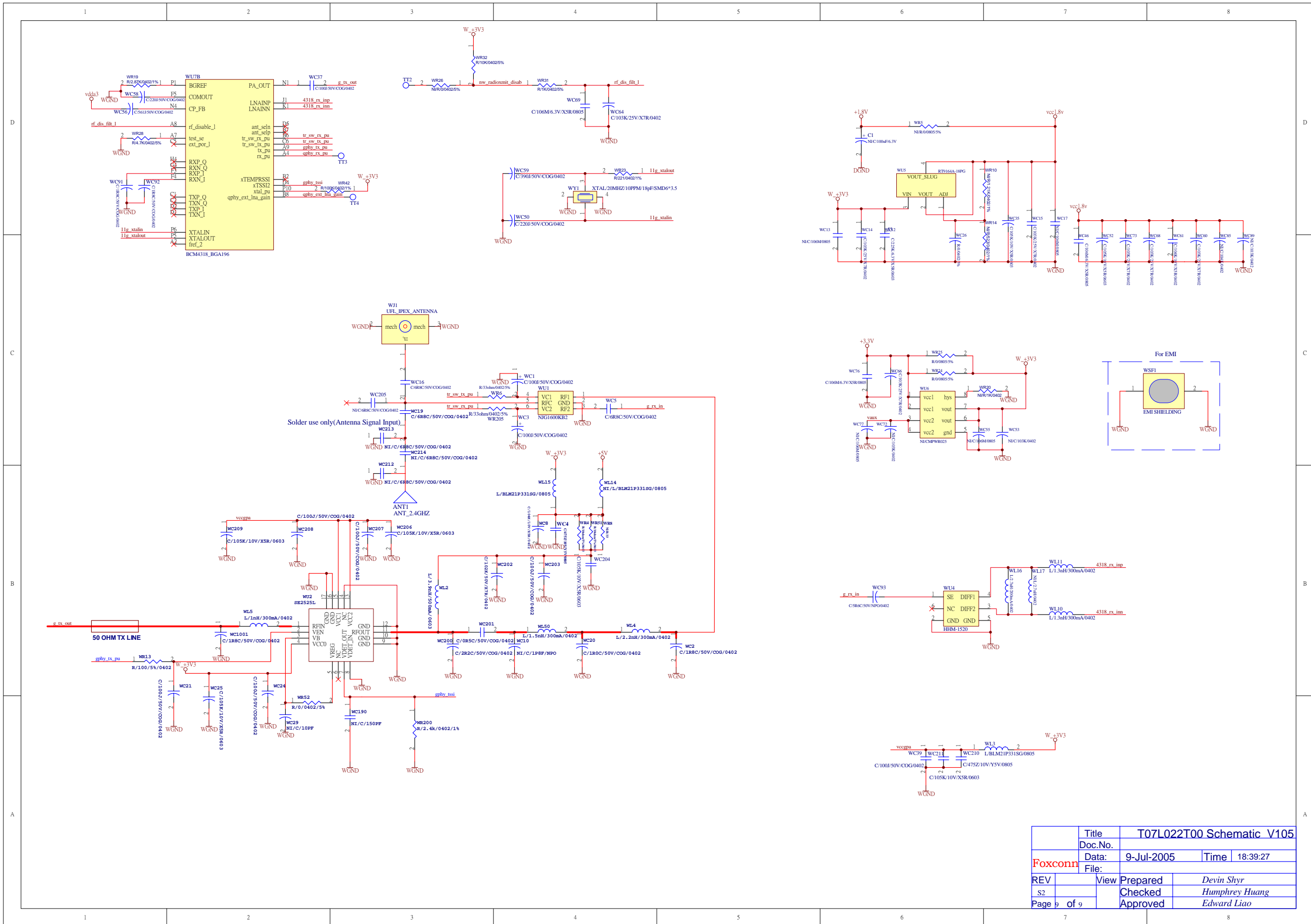
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Doc.No.			
Date:		9-Jul-2005	Time 18:39:25
File:			
REV	View	Prepared	Devin Shyr
S2		Checked	Humphrey Huang
Page 6 of 9		Approved	Edward Liao



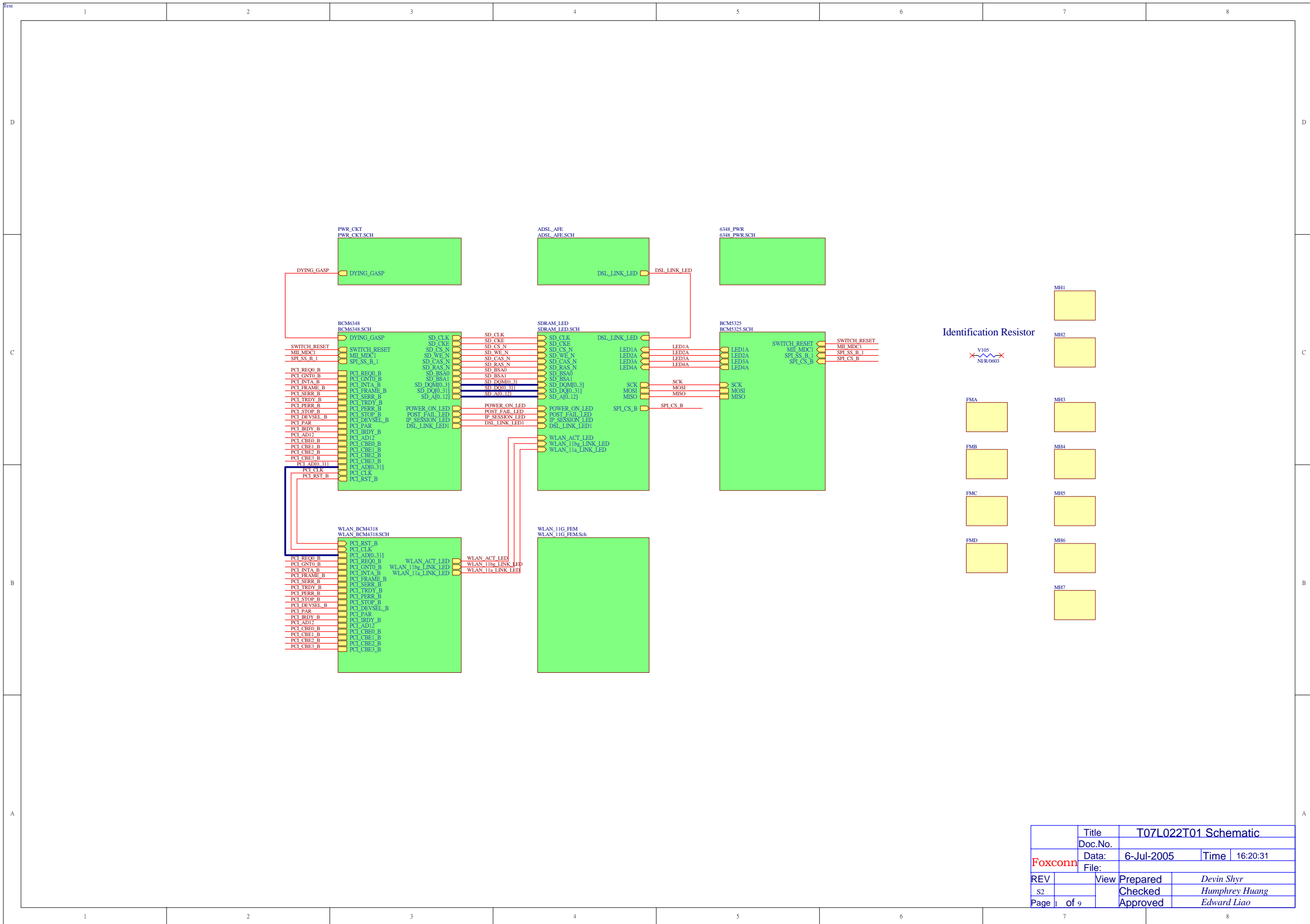
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Doc.No.			
Date:	9-Jul-2005	Time	18:39:25
File:			
REV	View	Prepared	Devin Shyr
S2		Checked	Humphrey Huang
Page 7	of 9	Approved	Edward Liao



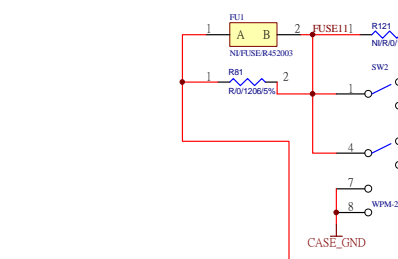
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Doc.No.			
Date:		9-Jul-2005	Time 18:39:26
File:			
REV	View	Prepared	Devin Shyr
S2		Checked	Humphrey Huang
Page 8 of 9		Approved	Edward Liao



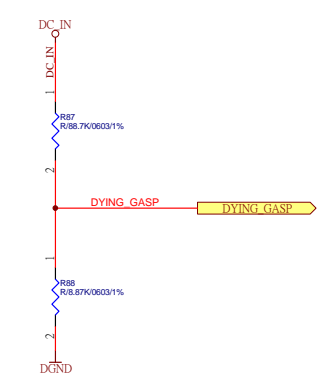
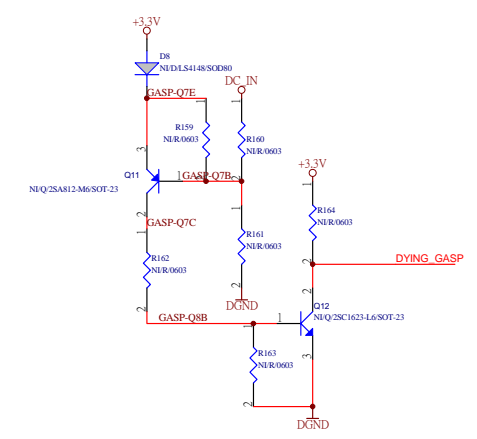
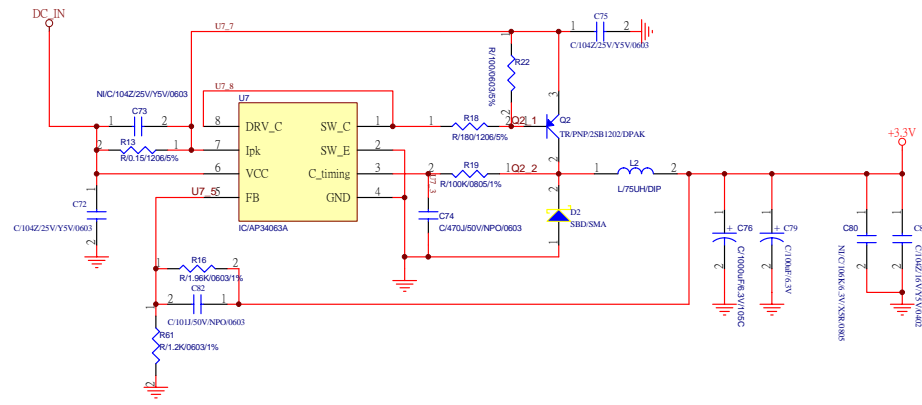
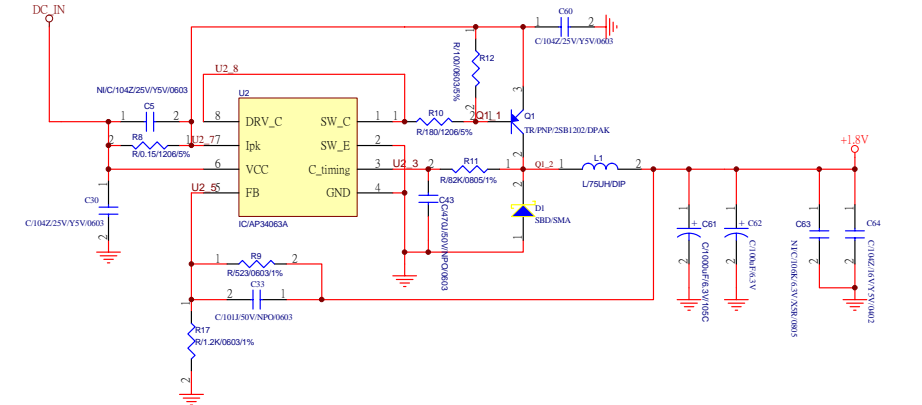
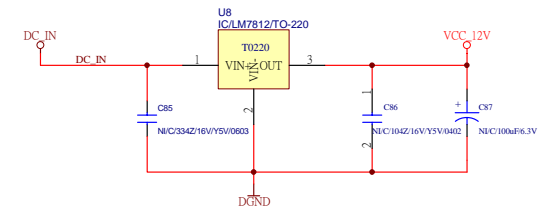
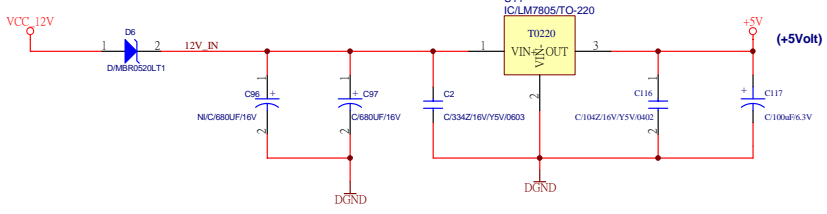
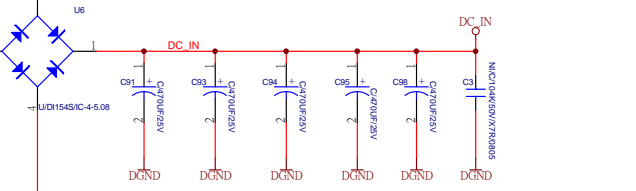
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Doc.No.			
Date:	9-Jul-2005	Time	18:39:27
File:			
REV	View	Prepared	Devin Shyr
S2	Checked	Humphrey Huang	
Page 9	of 9	Approved	Edward Liao



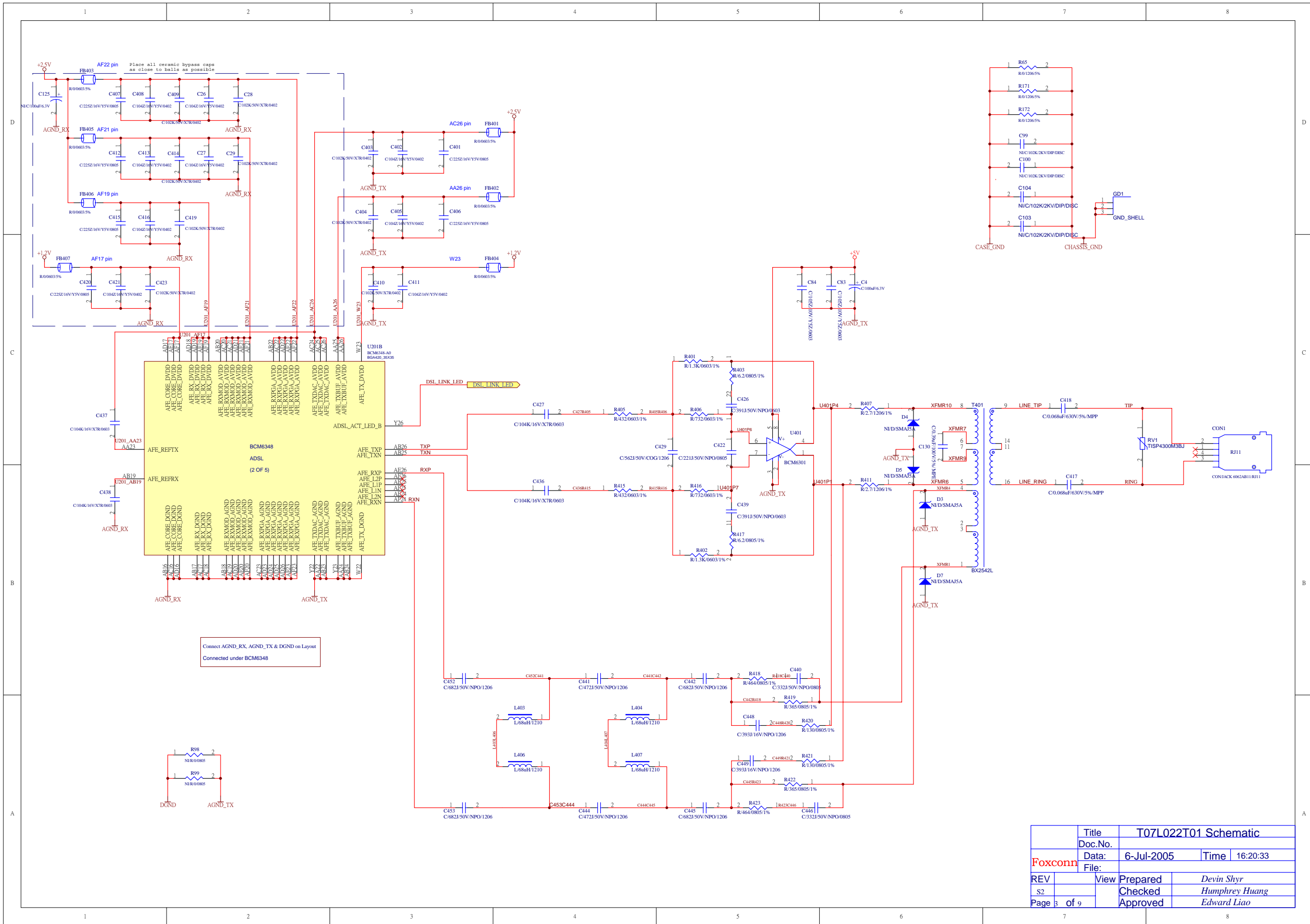
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	Doc.No.			
Foxconn	Date:	6-Jul-2005	Time	16:20:31
	File:			
REV	View	Prepared	Devin Shyr	
S2		Checked	Humphrey Huang	
Page	of 9	Approved	Edward Liao	



15vac INPUT

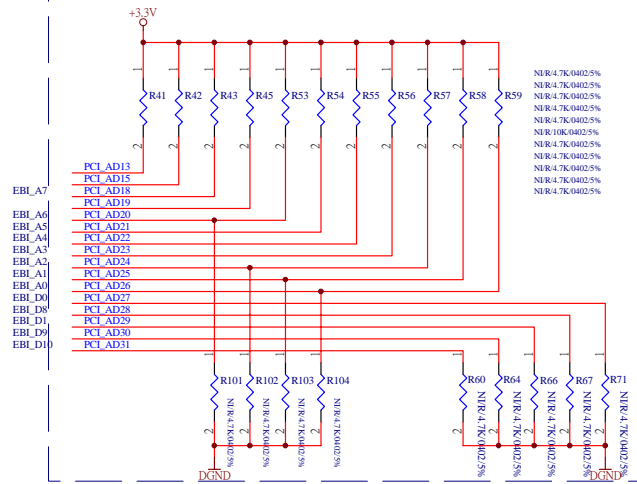


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Doc.No.			
Date:	6-Jul-2005	Time	16:20:32
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REV	View	Prepared	Devin Shyr
S2		Checked	Humphrey Huang
Page 2	of 9	Approved	Edward Liao

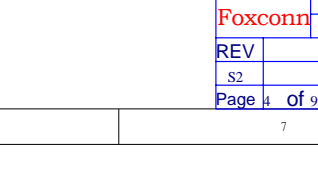
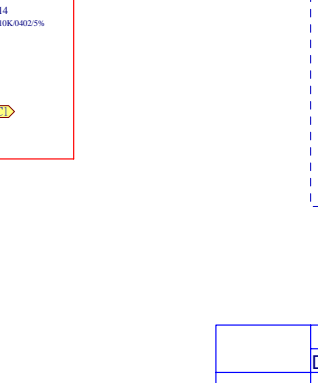
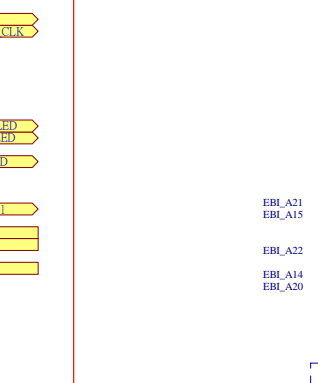
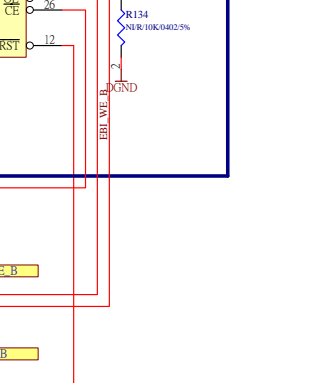
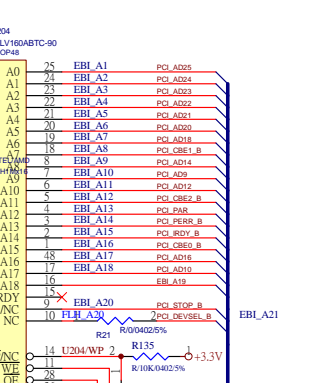
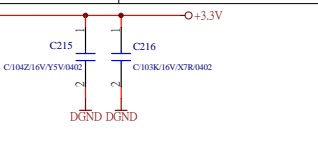
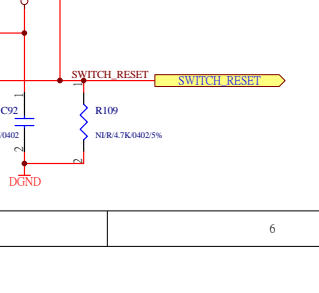
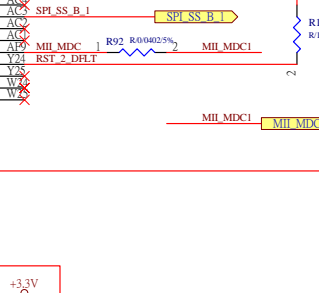
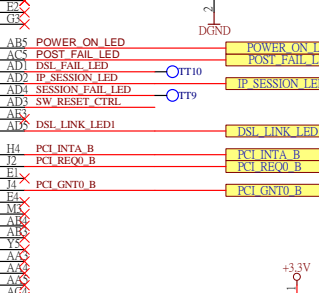
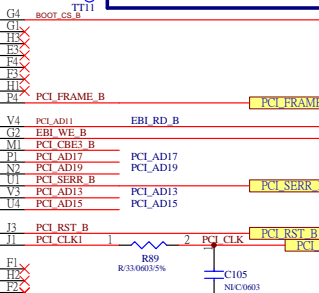
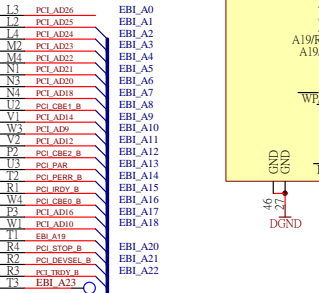
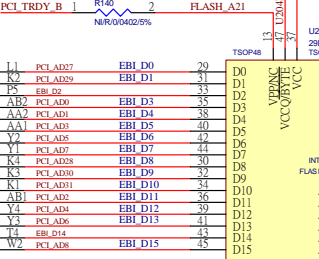
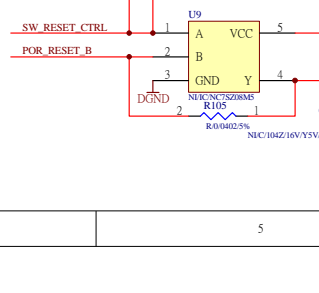
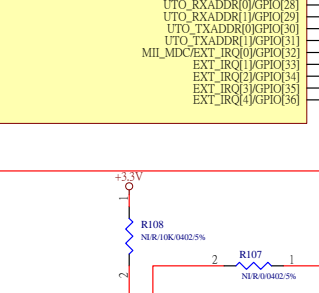
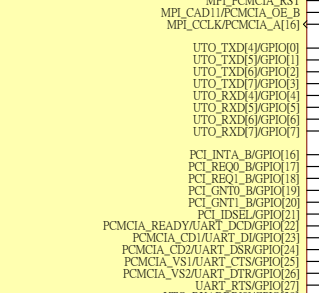
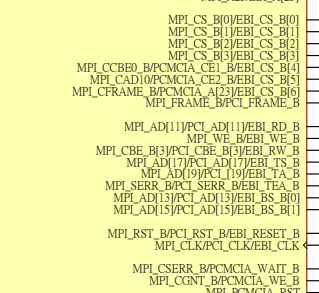
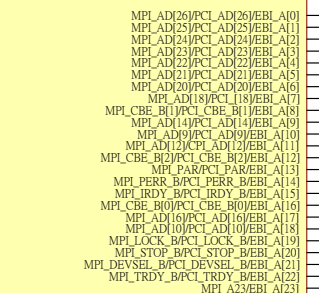
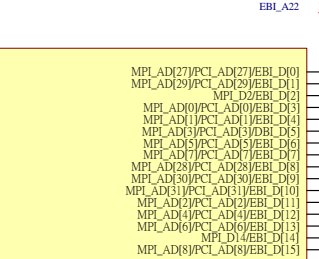
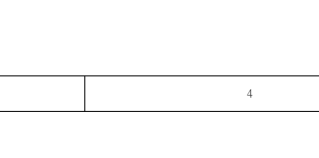
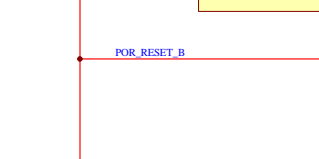
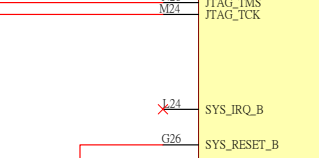
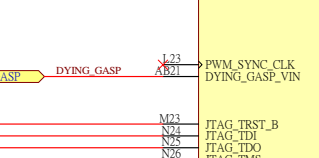
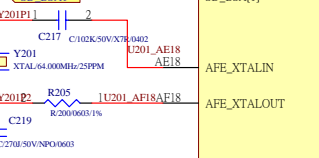
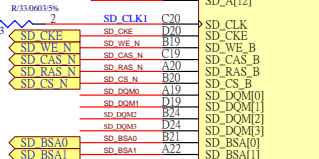
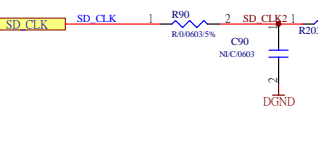
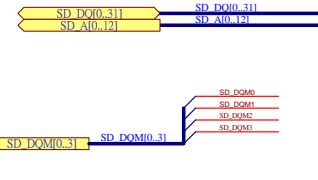


Title		T07L022T01 Schematic	
Doc.No.			
Date:		6-Jul-2005	Time 16:20:33
File:			
REV	View	Prepared	Devin Shyr
S2		Checked	Humphrey Huang
Page 3	of 9	Approved	Edward Liao

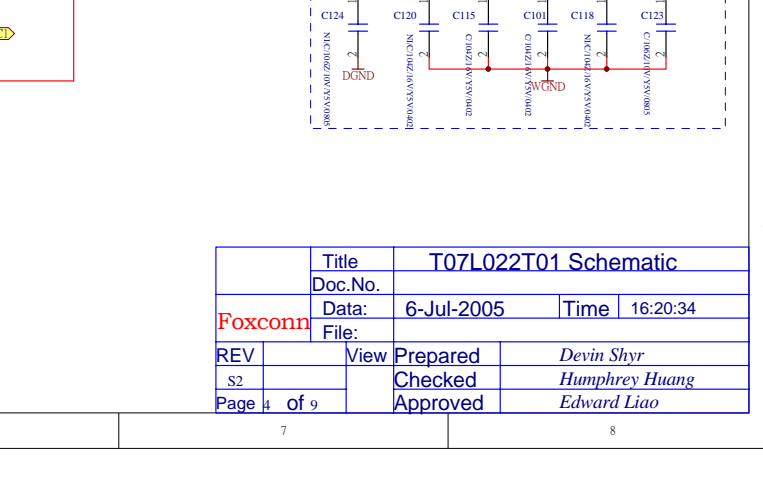
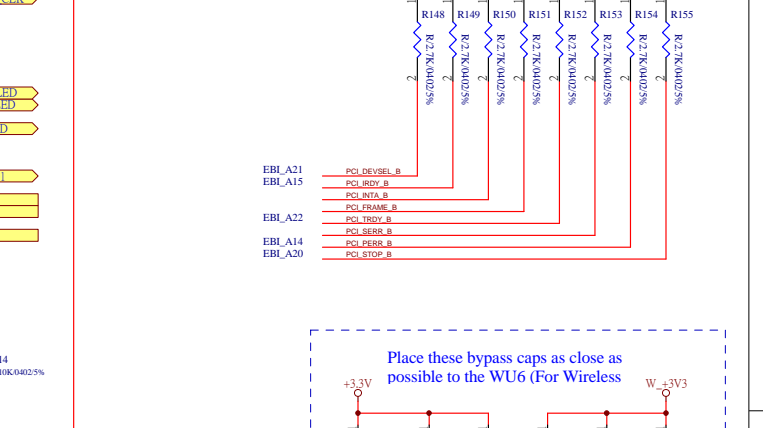
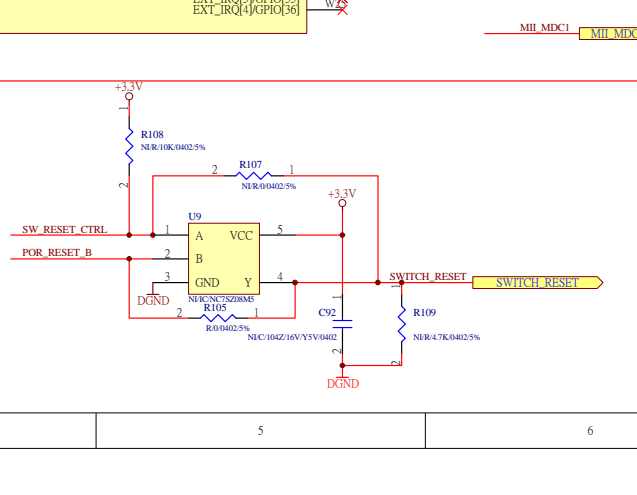
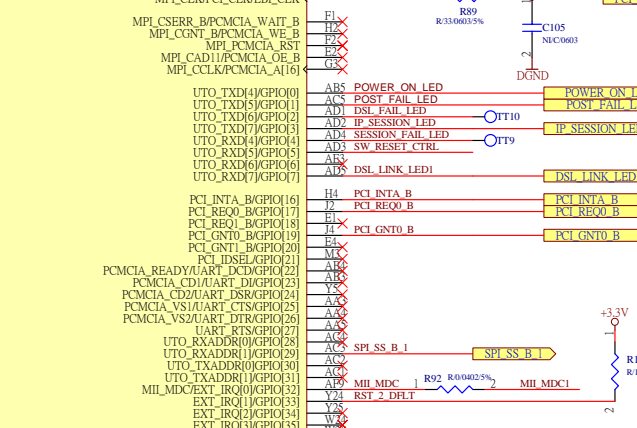
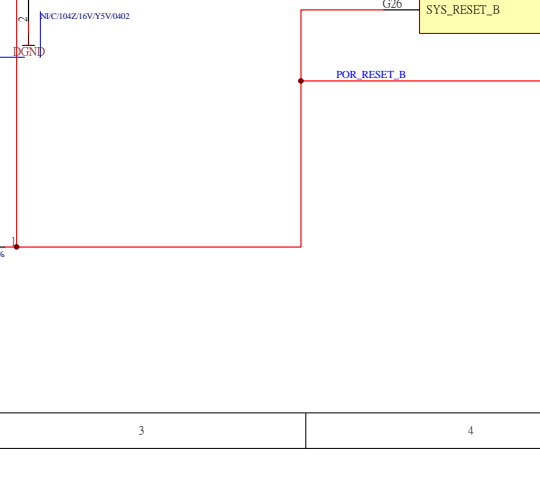
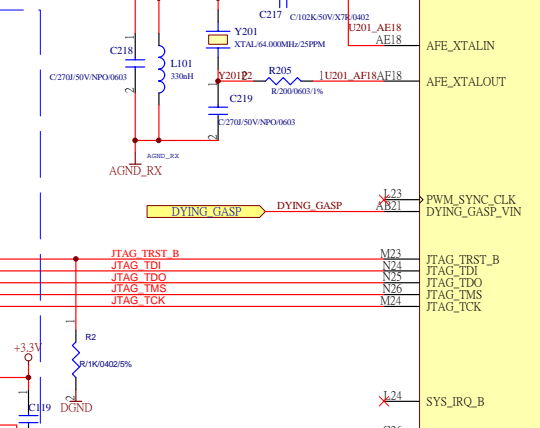
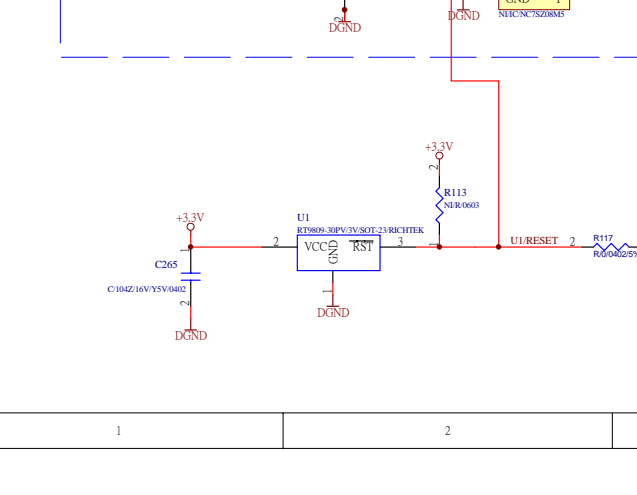
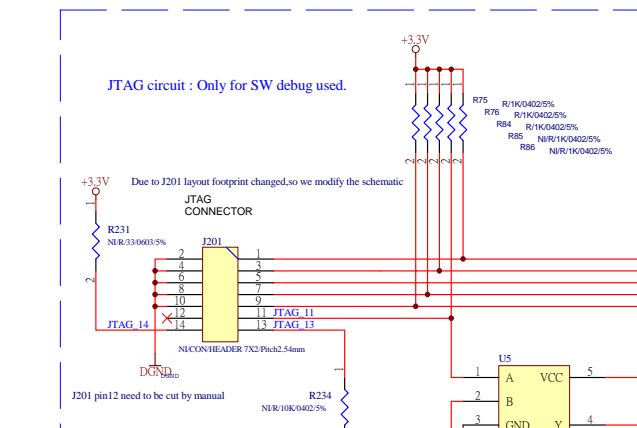
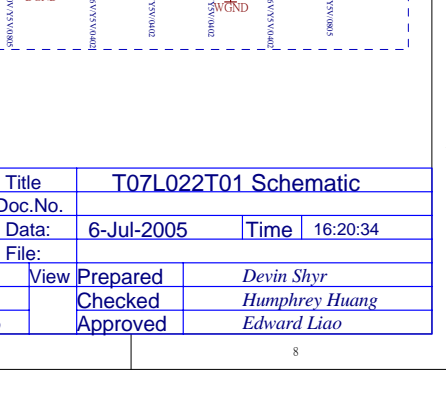
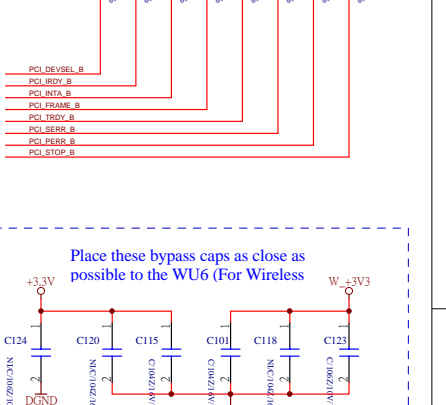
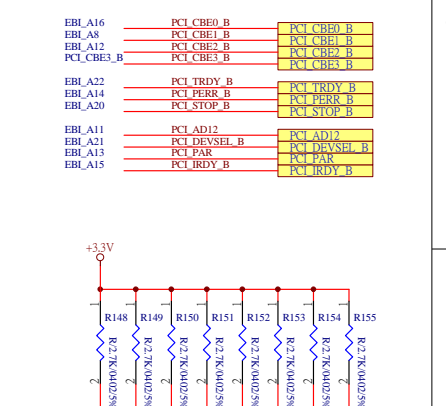
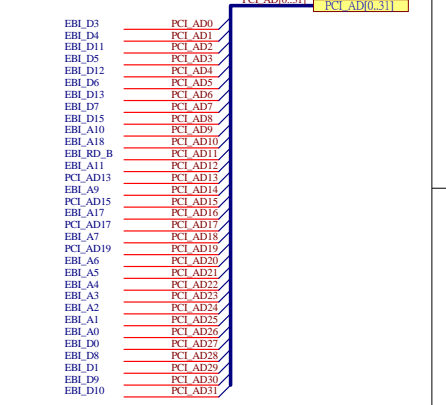
Power-On Strap Pins



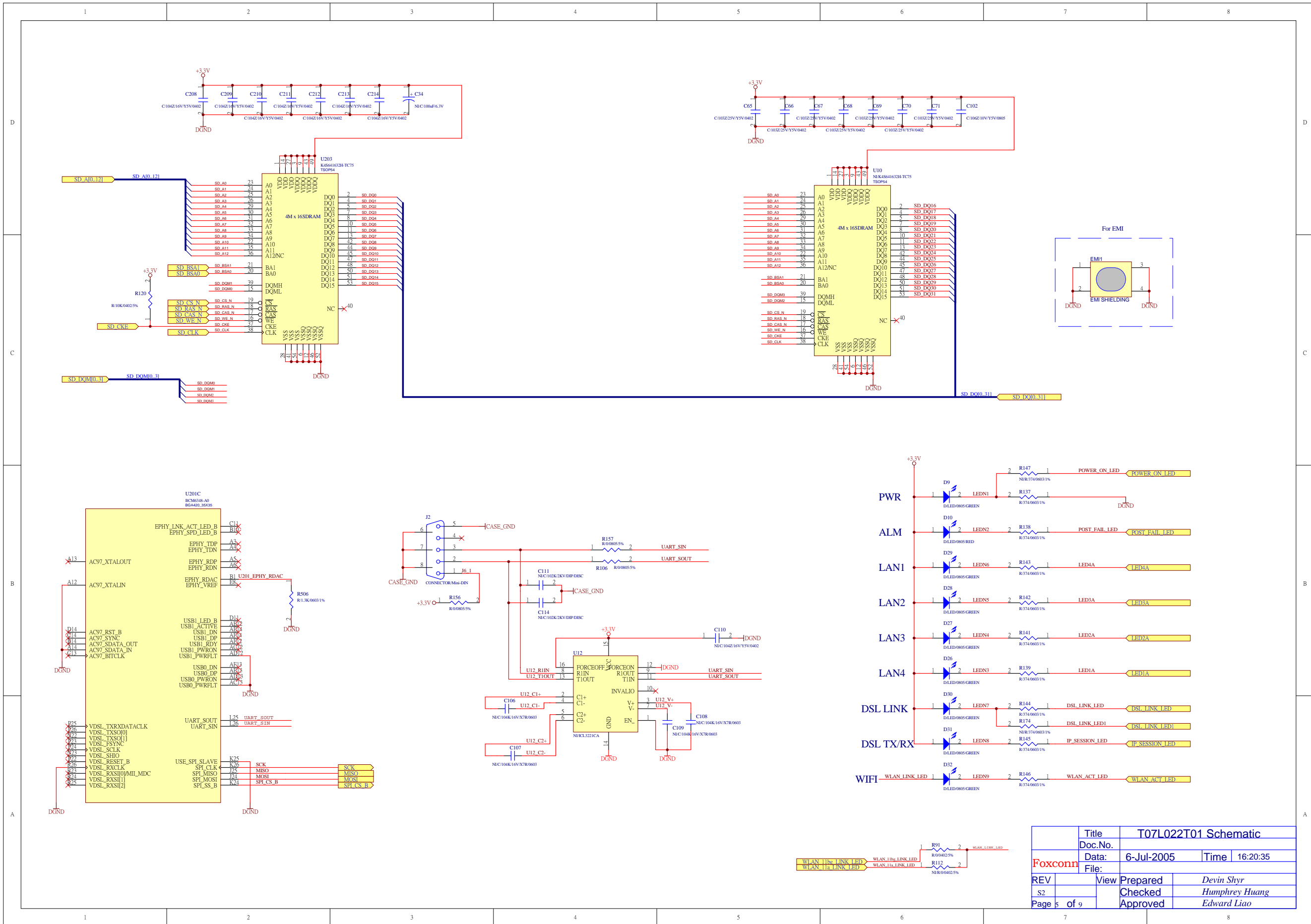
- Flash Data Width 16-Bits
- MIPS Endian Mode Big Endian
- Utopia Clock Mode Internal Clock Mode
- PCI Arbiter Select Internal Arbiter
- SPI Fast Clock Mode Big Endian
- Internal MPI Mode Normal Mode
- SPI Flash Addressing Mode 24-Bits Serial Flash Address
- Boot Flash Mode Boot From Parallel Flash on the EBI Bus
- MIPS Reset Delay 16 Cycles
- MIPS Reset Delay 16 Cycles
- MIPS Asyn. Reset Mode MIPS Boots in Asyn. Mode
- PLL Clock Select Modes 240MHz MIPS, 133MHz SDRAM
- PLL Clock Select Modes 240MHz MIPS, 133MHz SDRAM
- PLL Clock Select Modes 240MHz MIPS, 133MHz SDRAM
- PLL Clock Select Modes 240MHz MIPS, 133MHz SDRAM



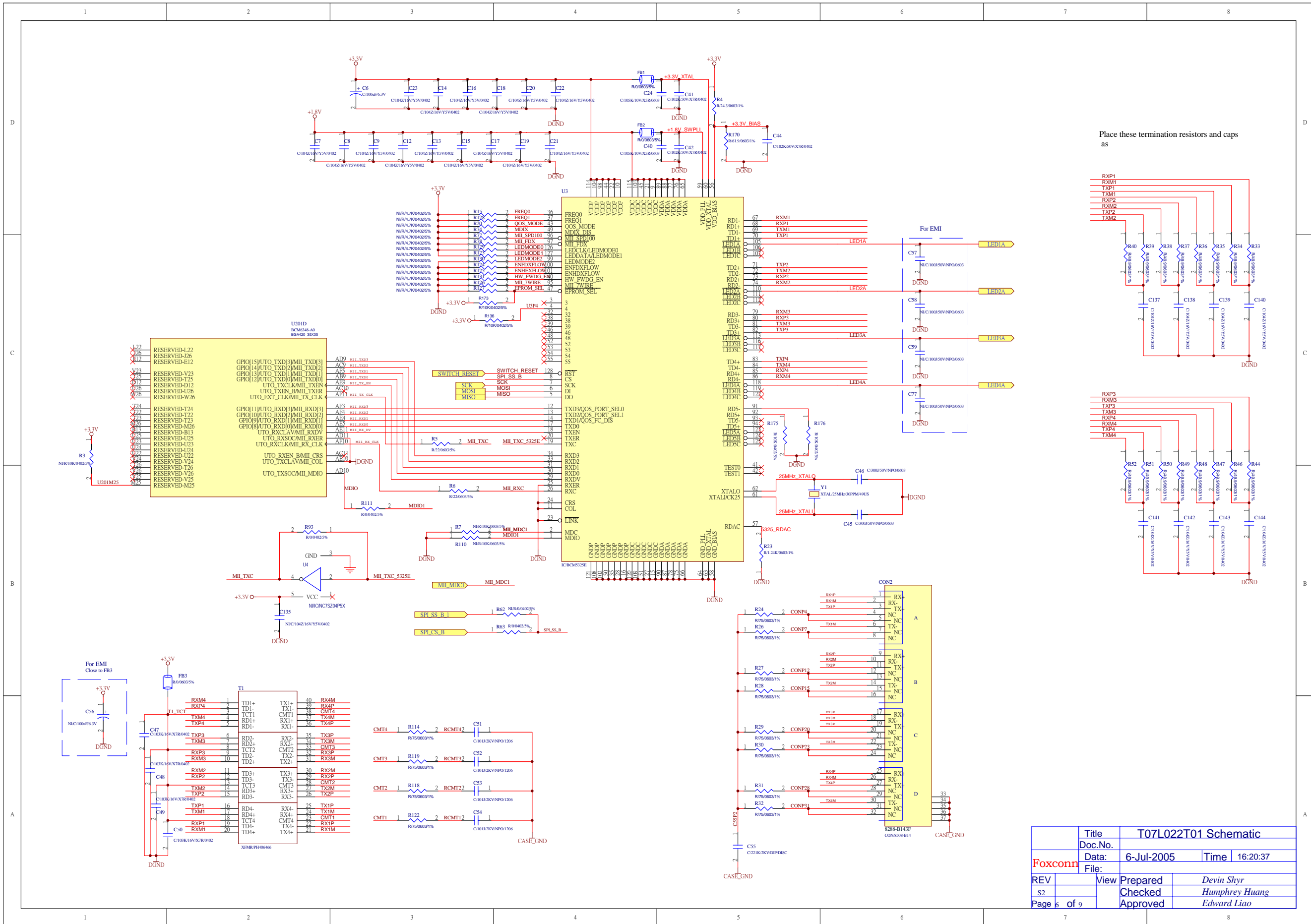
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R21	EQ	EQ	NE
R140	EQ	NE	NE
R134	NE	EQ	NE
R135	EQ	EQ	NE



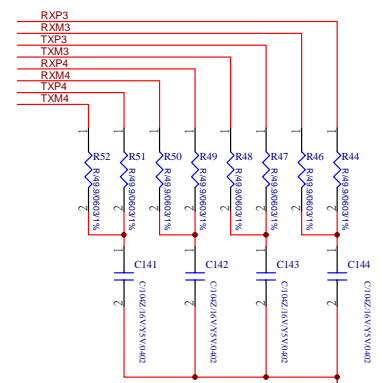
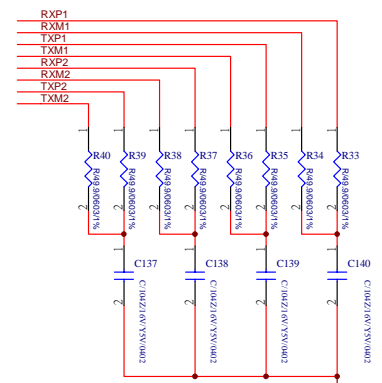
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Date:	6-Jul-2005	Time	16:20:34
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REV	View	Prepared	Devin Shyr
S2	Checked	Humphrey Huang	
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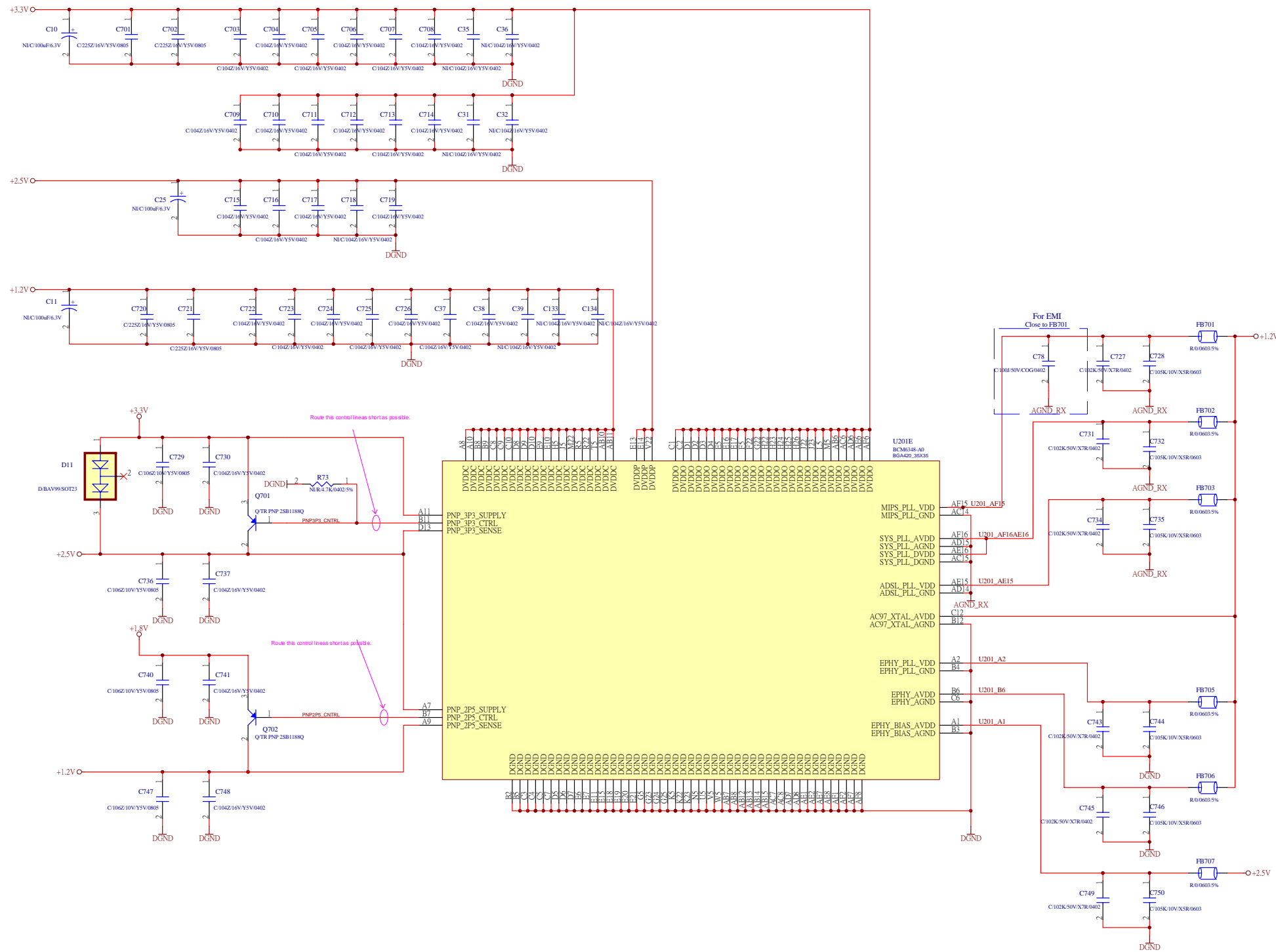
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Doc.No.			
Date:	6-Jul-2005	Time	16:20:35
File:			
REV	View	Prepared	Devin Shyr
S2	Checked	Humphrey Huang	
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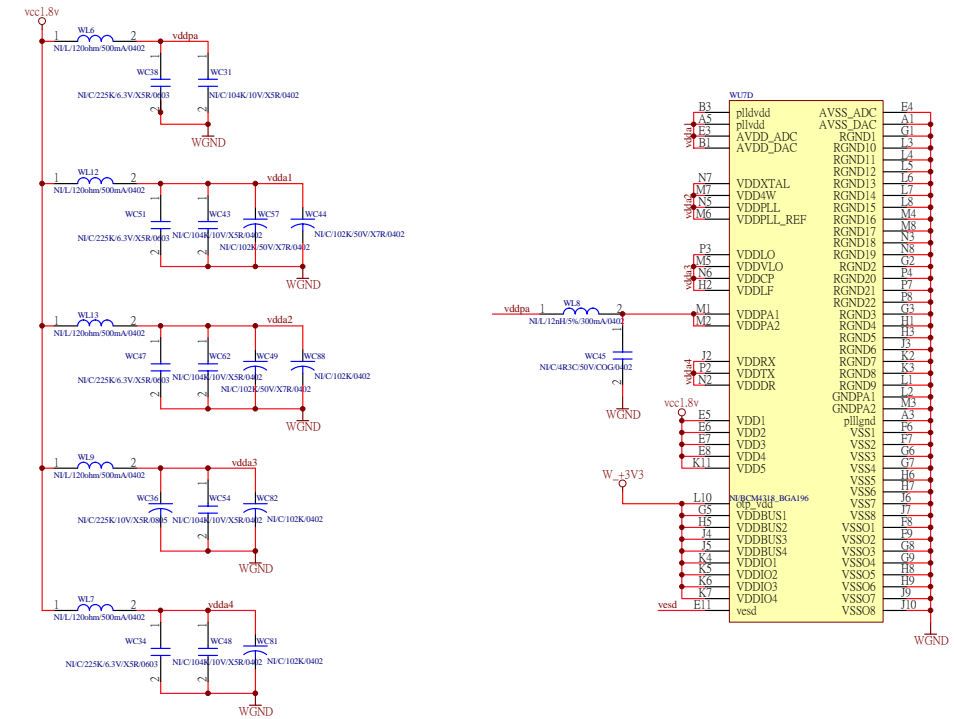
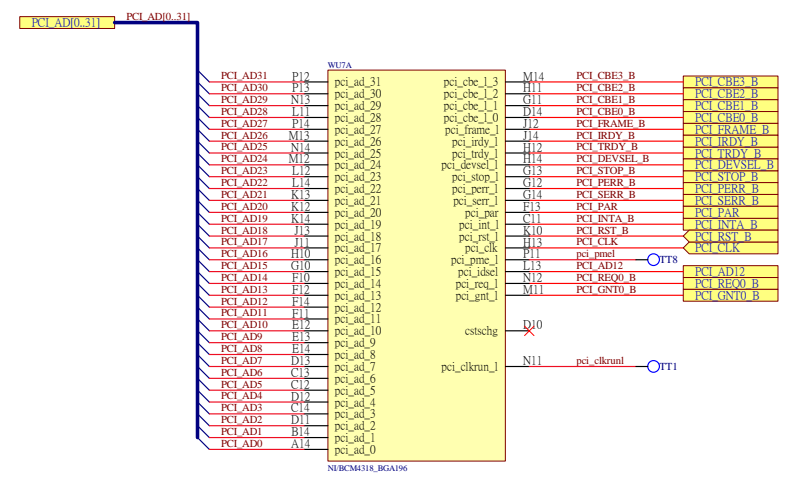
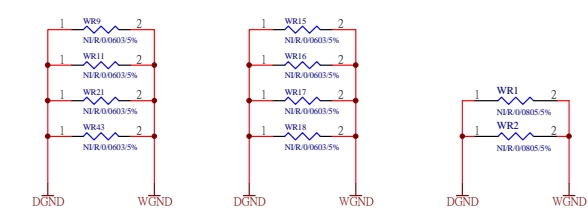
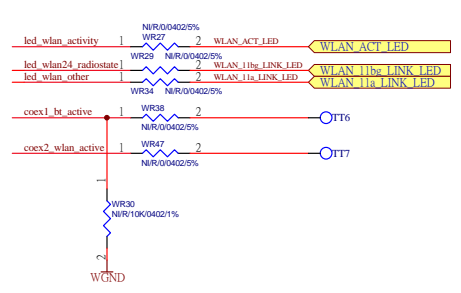
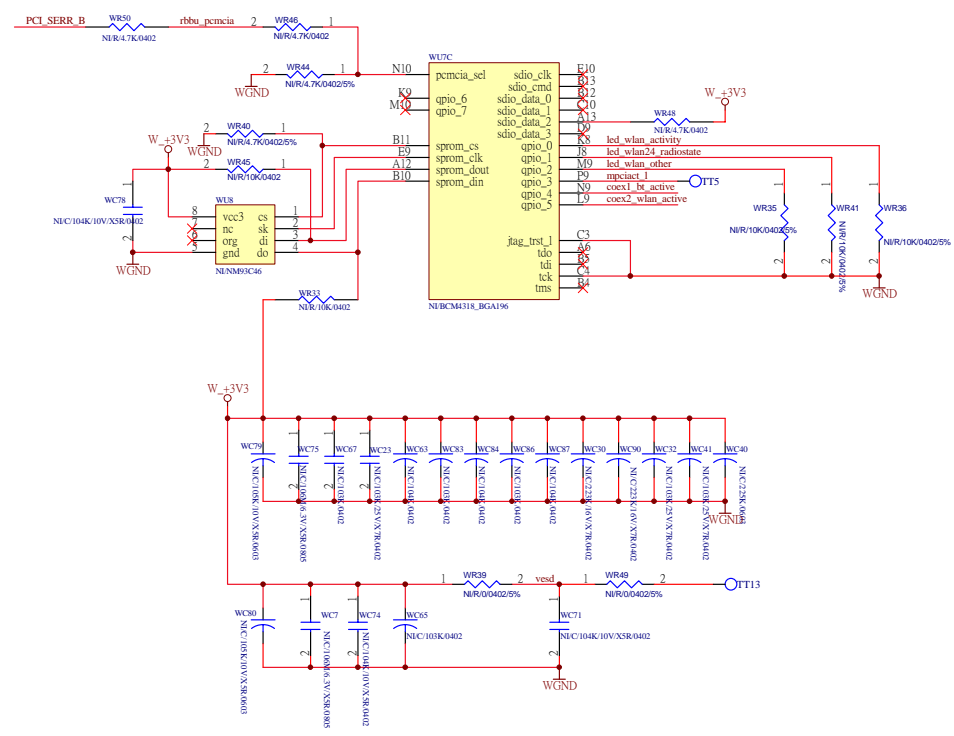
Place these termination resistors and caps as



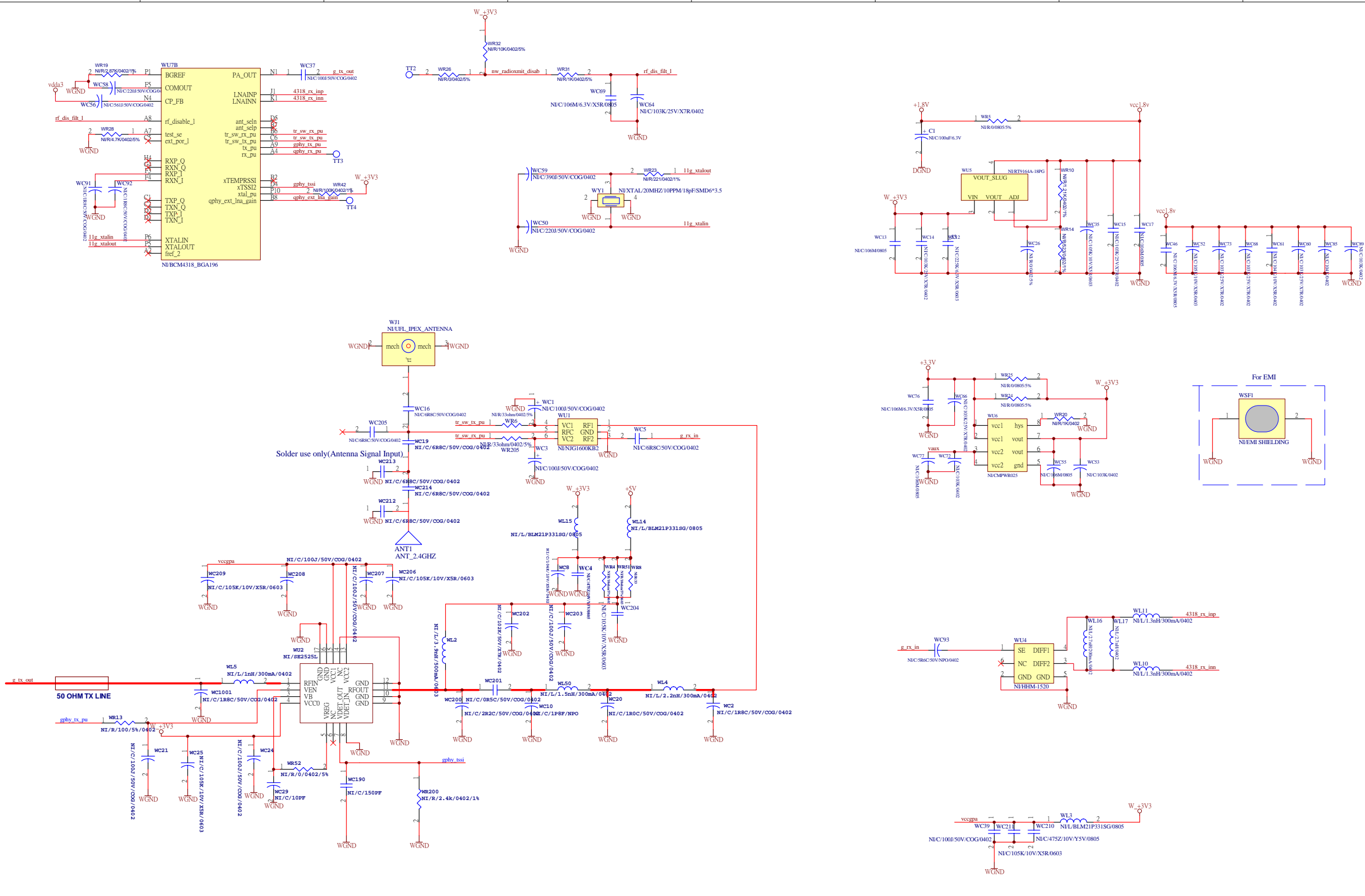
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Doc.No.			
Date:		6-Jul-2005	Time 16:20:37
File:			
REV	View	Prepared	Devin Shyr
S2		Checked	Humphrey Huang
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Doc.No.			
Date:		6-Jul-2005	Time 16:20:38
File:			
REV	View	Prepared	Devin Shyr
S2		Checked	Humphrey Huang
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Title		T07L022T01 Schematic	
Doc.No.			
Date:		6-Jul-2005	Time 16:20:38
File:			
REV	View	Prepared	Devin Shyr
S2		Checked	Humphrey Huang
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Title	T07L022T01 Schematic		
Doc.No.			
Date:	6-Jul-2005	Time	16:20:43
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REV	View	Prepared	Devin Shyr
S2		Checked	Humphrey Huang
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