F1DQ3021

Datasheet

Revision A5

List of Contents

1. General

1.1 Overview

This specification covers Bluetooth module (class-1) which complies with Bluetooth specification version 5.1 and integrates RF & Baseband controller in small package. This Module has deployed Qualcomm's QCC3021 QFN Chipset.

F1DQ3021_RevA1_Block Diagram

Chip Antenna	Bluetooth Radio	Apps Developer Processor	IO and USB		PIO
Apps Firmware Processor				USB/UART
				I2C/SPI
				LED
Kalimba DSP	Audio Inteface			I2S/PCM
				LINE IN
64Mbit Flash Memory	32MHz Crystal			Audio in/out
				SPDIF
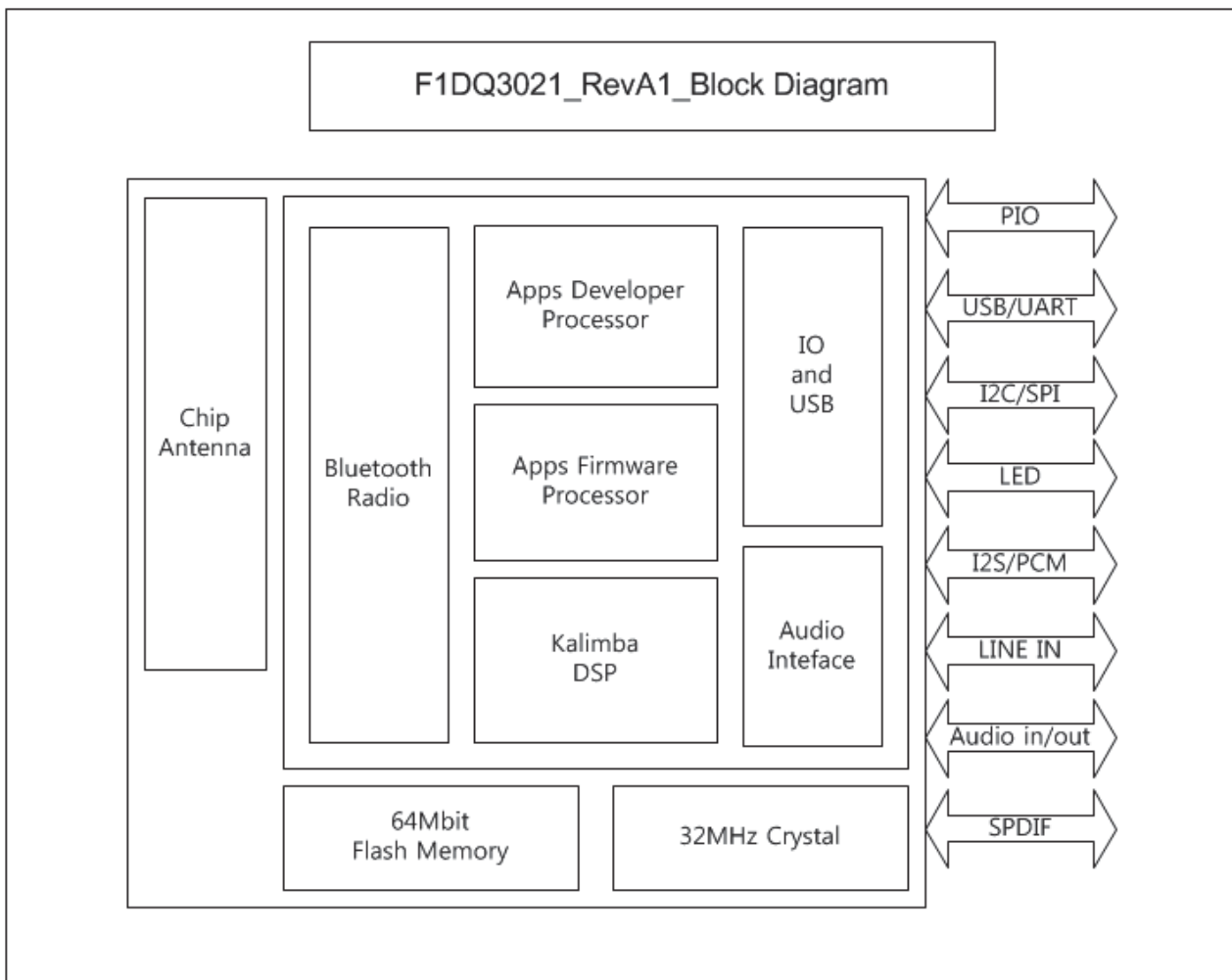
1.2 Features
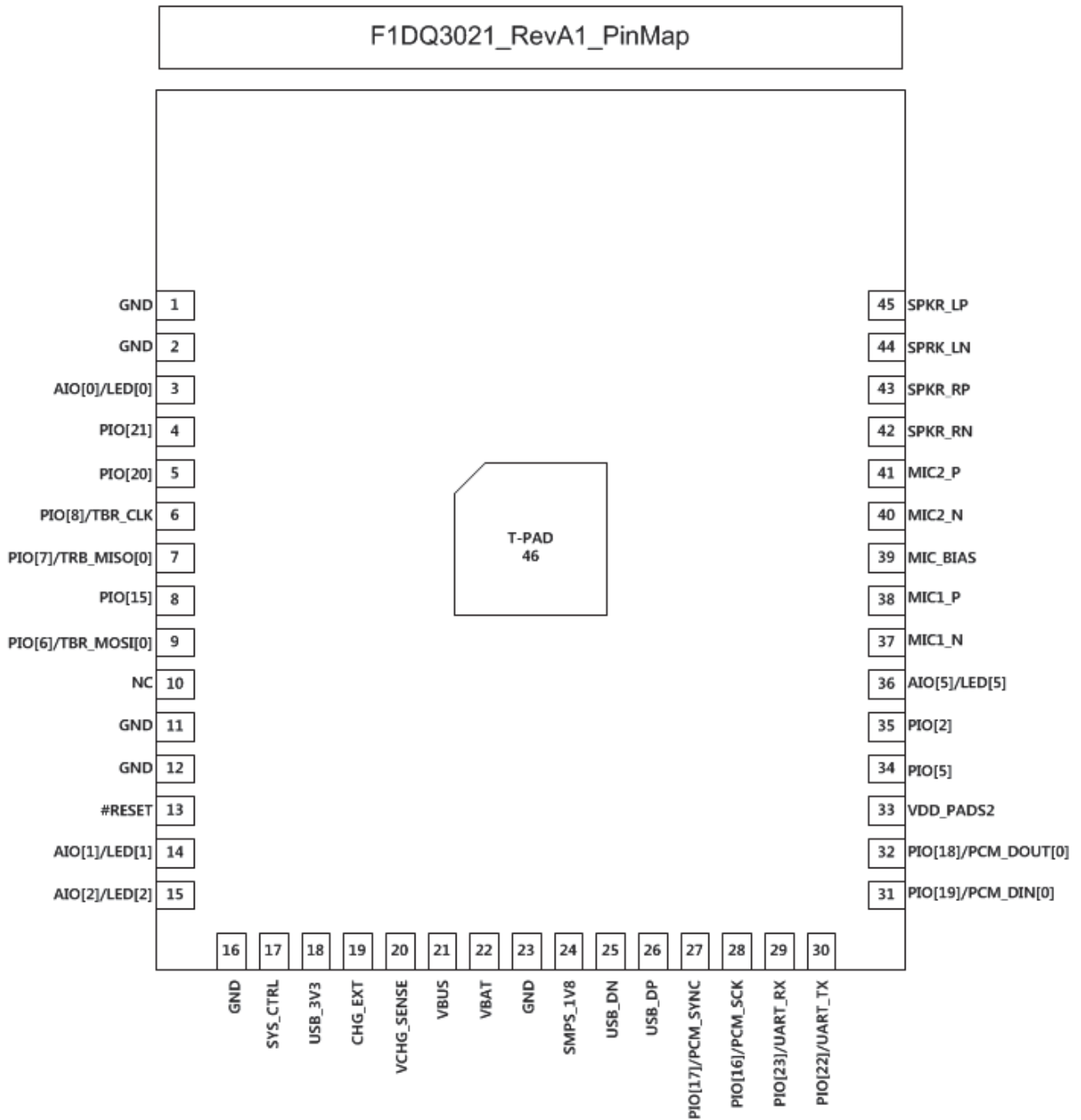
• Bluetooth supports

. Bluetooth 5.1 specification compliant

. RF performance of 8.5dbm Transmitter power(Conducted)

. -95dBm Basic rate Receiver sensitivity(Conducted)

. Internal Chip Antenna

• Kalimba DSP

. Qualcomm Kalimba DSP (120MIPS)

• Audio Interface

. I2S and PCM

. SPDIF

. Analog and Digital microphone

• Physical interfaces

. UART/USB(2.0)

. 15 general PIO

. 1 PCM/I2S

. 1 SPDIF interfaces

. 5 LED drivers

• Memory

. On-chip 5Mb Rom,

. 80KB Program Ram, 256KB Data Ram, External 64M bit Serial Quad I/O Flash

• Battery Charger

. Lithium ion/Lithium polymer battery charger

. Support USB charger detection

• Improved Audio Quality

. CVC noise cancel support

. SBC and ACC audio codec

. Stereo Codec

1.3 Application

• Wireless speakers

1.4 Pinout Diagram

Top view

F1DQ3021_RevA1_PinMap

Pin	Name
1	GND
2	GND
3	AIO[0]/LED[0]
4	PIO[21]
5	PIO[20]
6	PIO[8]/TBR_CLK
7	PIO[7]/TRB_MISO[0]
8	PIO[15]
9	PIO[6]/TBR_MOSI[0]
10	NC
11	GND
12	GND
13	#RESET
14	AIO[1]/LED[1]
15	AIO[2]/LED[2]

Pin	Name
45	SPKR_LP
44	SPRK_LN
43	SPKR_RP
42	SPKR_RN
41	MIC2_P
40	MIC2_N
39	MIC_BIAS
38	MIC1_P
37	MIC1_N
36	AIO[5]/LED[5]
35	PIO[2]
34	PIO[5]
33	VDD_PADS2
32	PIO[18]/PCM_DOUT[0]
31	PIO[19]/PCM_DIN[0]

T-PAD 46

Pin	Name
16	GND
17	SYS_CTRL
18	USB_3V3
19	CHG_EXT
20	VCHG_SENSE
21	VBUS
22	VBAT
23	GND
24	SMPS_1V8
25	USB_DN
26	USB_DP
27	PIO[17]/PCM_SYNC
28	PIO[16]/PCM_SCK
29	PIO[23]/UART_RX
30	PIO[22]/UART_TX

1.5 Device Terminal Functions

Pad	Pin Name	I/O	Pin Description
1	GND	-	GROUND
2	GND	-	GROUND
3	AIO[0]/LED[0]	I/O	Analog or digital input/open drain output or open drain LED output.
4	PIO[21]	I/O	Programmable input/output
5	PIO[20]	I/O	Programmable input/output
6	TRB_CLK	I/O	Alternative function: ■PIO[8]
7	TRB_MISO[0]	I/O	Alternative function: ■PIO[7]
8	PIO[15]	I/O	Programmable input/output
9	TRB_MOSI[0]	I/O	Alternative function: ■PIO[6]
10	NC	-	NC
11	GND	-	GROUND
12	GND	-	GROUND
13	RESET#	I/O	Reset if low. Pull low for minimum 5 ms to cause a reset.
14	AIO[1]/LED[1]	I/O	Analog or digital input/open drain output or open drain LED output.
15	AIO[2]/LED[2]	I/O	Analog or digital input/open drain output or open drain LED output.
16	GND	-	GROUND
17	SYS_CTRL	I	Regulator enable and multifunction button.
18	3V3_USB	O	3.3V bypass linear regulator output.
19	CHG_EXT	O	External battery charger transistor base control when using external charger boost.
20	VCHG_SENSE	I	Supply to SMPS power switch from charger input.
21	VBUS	I	Charger input.
22	VBAT	I	Battery positive terminal.
23	GND	-	GROUND
24	SMPS_1V8	O	SMPS 1V8 OUT
25	USB_DN	I/O	USB data minus
26	USB_DP	I/O	USB data plus
27	PIO[17]/PCM_SYNC	I	Alternative function:■I2S_WS
28	PIO[16]/PCM_CLK	I	Alternative function:■UART_CTS ■ I2S_SCK
29	UART_RX	I	Alternative function:■ PIO[23]
30	UART_TX	O	Alternative function:■ PIO[22]

31	PIO[19]/PCM_DIN[0]	I	Alternative function: ∎I2S_SD_IN
32	PIO[18]/PCM_DOUT[0]	O	Alternative function: ∎I2S_SD_OUT
33	VDD_PADS2	I	Positive supply input for input ports.
34	PIO[5]	I/O	Programmable input/output
35	PIO[2]	I/O	Programmable input/output
36	LED[5]	I/O	Analog or digital input/open drain output or open drain LED output.
37	MIC1_N	I	Line or microphone input negative, channel 1
38	MIC1_P	I	Line or microphone input positive, channel 1
39	MIC_BIAS	O	Microphone bias
40	MIC2_N	I	Line or microphone input negative, channel 2
41	MIC2_P	I	Line or microphone input positive, channel 2
42	SPKR_RN	O	Speaker output negative, right
43	SPKR_RP	O	Speaker output positive, right
44	SPKR_LN	O	Speaker output negative, left
45	SPKR_LP	O	Speaker output positive, left
46	T-PAD	-	GROUND

1.6 Module Dimension

F1DQ3021_RevA1_Dimension

1. Top View (Unit : mm)

20

6

14.4

1

45

2.5

24.5

1.2

3

10

0.7

15

31

1.7

16

30

1

1.2

1.6

2.0

Shield Can

3

1

PCB
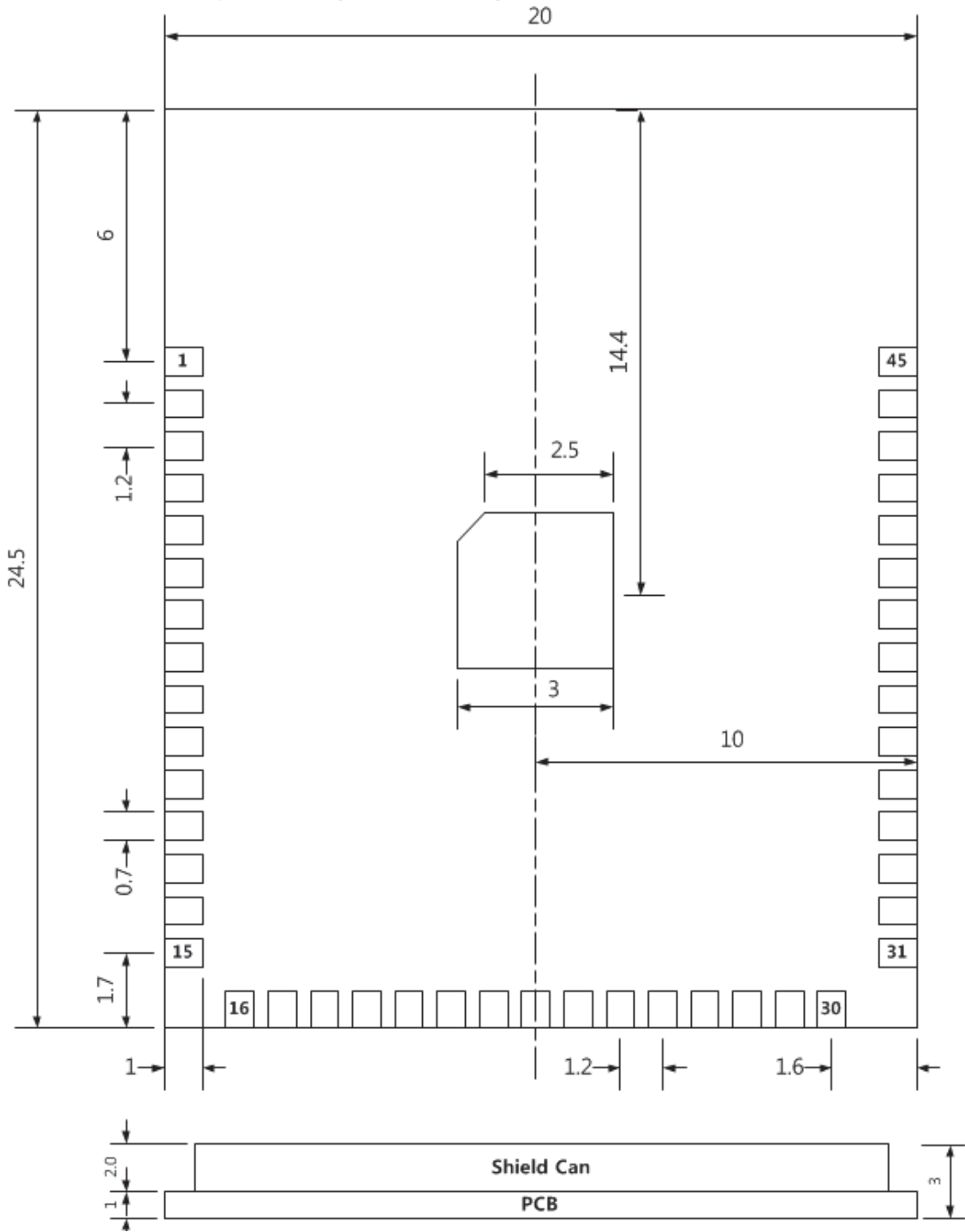
2. Characteristics

2.1.1 Electrical Characteristics

Absolute Maximum Rating					
Parameter			MIN	MAX	UNIT
Storage temperature			-40	85	℃
Supply voltage					
5 V (USB)	VBUS		-0.4	7	
	VCHG_EXT				
	VCHG_SENSE				
BATTERY	VBAT		-0.4	4.8	
3.3V	USB_3V3		-0.4	3.8	
	USB_DP				
	USB_DN				V
1.8V	SMPS_1V8		-0.4	2.1	
	AUDIO IN/OUT				
DIGITAL I/O	PIO[23:15, 8:2]		-0.4	3.8	
	VDD_PADS2				
	AIO/LED[5, 2:0]		-0.4	7	
	SYS_CTRL		-0.4	4.8	

Recommended operating conditions						
Parameter			MIN	TYP	MAX	UNIT
Operating Temp. Range			-40	20	85	℃
Supply voltage						
5 V (USB)	VBUS		4.75 / 4.0a	5	6.5	
	VCHG_EXT					
	VCHG_SENSE					
BATTERY	VBAT		3.0 / 2.8b	3.7	4.6	
3.3V	USB_3V3		2.8	2.9/3.3	3.5	
	USB_DP		0	-	3.6	V
	USB_DN					
1.8V	SMPS_1V8		1.7	1.8	1.95	
	AUDIO IN/OUT		0	-	1.95	
DIGITAL I/O	PIO[23:15, 8:2]		0		VDD_PADS	
	#RESET		0		USB_3V3	
	VDD_PADS2		1.7	1.8	3.6	
	AIO/LED[5, 2:0]		0		1.95	
	SYS_CTRL		0		4.6	

a Minimum input voltage of 4.75 V is required for full specification. Li-ion charger operates at reduced specification from 4.0 V.

b Recommended software power-off threshold at 3.0 V. Device operates down to 2.8 V.

2.1.2 Power Consumption

ID	Scenario	Consumption
DASH_LP_01	Power Off	2 uA
DASH_BT_01	500 ms Bluetooth Sniff, four slot no retries, AFH on, Sink App running, Audio off	840 uA
DASH_A2DP_05	A2DP SBC 350 kbit, Low Power Graph, Input 48 kHz, Output Stereo DAC 48 KHz	12.0 mA
DASH_A2DP_08	A2DP aptX Classic 384 kbit, Input 48 kHz, Output Stereo DAC 48 KHz	15.0 mA
DASH_A2DP_12	A2DP AAC-LC 256kbit, Low Power Graph, Input 48kHz, Output Stereo DAC 48KHz	11.7 mA
DASH_HFP_01	HFP Narrow Band (CVSD) 2EV3, 1 Analog MIC cVc Speaker, Analog DAC	14.9 mA
DASH_HFP_08	2 MIC Wide Band (SBC) Speaker LP DAC, LP ADC 2EV3	17.3 mA

2.2 RF Characteristics

2.2.1 BR(conducted)

Transmitter

RF Characteristics		Min	Typ	Max	Bluetooth Specification	Unit
Maximum RF transmit power		-	5	-	-6 to 20	dBm
RF power variation over temperature range		-	±1	-	-	dB
20 dB bandwidth for modulated carrier		-	937	1000	≤1000	kHz
ACP	F = F0 ± 2 MHz	-	-43	-20	≤-20	dBm
	F = F0 ± 3 MHz	-	-49	-40	≤-40	dBm
	F = F0 ± > 3 MHz	-	-58	-40	≤-40	dBm
Δf1avg maximum modulation		140	165	175	140 < f1avg < 175	kHz
Δf2max minimum modulation		115	143	-	≥115	kHz
Δf2avg/Δf1avg		0.8	0.93	-	≥0.80	-
ICFT		-75	3	75	±75	kHz
Drift rate		-	4	20	≤20	kHz/50 µs
Drift (single slot packet)		-	7	25	≤25	kHz
Drift (five slot packet)		-	9	40	≤40	kHz
2nd harmonic content		-	-27	-	-	dBm
3rd harmonic content		-	-21	-	-	dBm

Receiver

RF Characteristics	Frequency (GHz)	Min	Typ	Max	Bluetooth Specification	Unit
Sensitivity at 0.1% BER for all basic rate packet types	2.402	-	-90	-	≤-70	dBm
	2.441	-	-90	-		
	2.480	-	-90	-		
Maximum received signal at 0.1% BER		-20	>-9	-	≥-20	
Continuous power required to block Bluetooth reception (for input power of -67 dBm with 0.1% BER)	0.030 - 2.000	-10	>4	-	-10	
	2.000 - 2.400	-27	-4	-	-27	
	2.500 - 3.000	-27	-2	-	-27	
	3.000 - 12.75	-10	>5	-	-10	
C/I co-channel		-	10	11	≤11	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	-	-12	0	≤0	dB
	F = F0 - 1 MHz	-	-9	0	≤0	dB
	F = FImage(F0 + 2 MHz)	-	-33	-9	≤-9	dB
	F = F0 - 2 MHz	-	-39	-30	≤-20	dB
	F = FImage + 1 MHz	-	-43	-20	≤-40	dB
	F = F0 - 3 MHz	-	-48	-40	≤-40	dB
Maximum level of intermodulation interferers		-39	-24	-	≥-39	dBm
Spurious output level		-	-155	-	-	dBm/Hz

2.2.2 EDR(Conducted)

Transmitter

RF Characteristics, VDD = 3.3 V		Min	Typ	Max	Bluetooth Specification	Unit
Maximum RF transmit power	π/4 DQPSK	-	5	-	≤20	dBm
	8DPSK	-	5	-	≤20	dBm
Relative transmit power		-	0	-	-4 to 1	dB
π/4 DQPSK max carrier frequency stability	|ωo|	-	1	10	≤10 for all blocks	kHz
	|ωi|	-	1	75	≤75 for all packets	kHz
	|ωo + ωi|	-	1	75	≤75 for all blocks	kHz
8DPSK max carrier frequency stability	|ωo|	-	1	10	≤10 for all blocks	kHz
	|ωi|	-	1	75	≤75 for all packets	kHz
	|ωo + ωi|	-	1	75	≤75 for all blocks	kHz
π/4 DQPSK	RMS DEVM	-	4	20	≤20	%
	99% DEVM	-	9	30	≤30	%
	Peak DEVM	-	10	35	≤35	%
8DPSK modulation accuracy	RMS DEVM	-	4	13	≤13	%
	99% DEVM	-	10	20	≤20	%
	Peak DEVM	-	11	25	≤25	%
In-band spurious emissions	F > F0 + 3 MHz	-	-52	-39	≤-40	dBm
	F < F0 - 3 MHz	-	-52	-40	≤-40	dBm
	F = F0 - 3 MHz	-	-38	-37	≤-40	dBm
	F = F0 - 2 MHz	-	-27	-20	≤-20	dBm
	F = F0 - 1 MHz	-	-34	-26	≤-26	dB
	F = F0 + 1 MHz	-	-34	-26	≤-26	dB
	F = F0 + 2 MHz	-	-28	-20	≤-20	dBm
	F = F0 + 3 MHz	-	-42	-40	≤-40	dBm
EDR differential phase encoding		99	No Errors	-	≥99	%

Receiver

RF Characteristics, VBAT = 3.3 V		Modulation	Min	Typ	Max	Bluetooth Specification	Unit
Sensitivity at 0.01% BER	Ch 0	π/4 DQPSK	-	-90	-	≤-70	dBm
	Ch 39	π/4 DQPSK	-	-90	-		
	Ch 78	π/4 DQPSK	-	-90	-		
	Ch 0	8DPSK	-	-84	-		
	Ch 39	8DPSK	-	-84	-		
	Ch 78	8DPSK	-	-84	-		
Maximum received signal at 0.1% BER		π/4 DQPSK	-20	>-9	-	≥-20	dBm
		8DPSK	-20	>-9	-	≥-20	
C/I co-channel at 0.1% BER		π/4 DQPSK	-	9	13	≤13	dB
		8DPSK	-	16	21	≤21	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	π/4 DQPSK	-	-13	0	≤0	dB
		8DPSK	-	-8	5	≤5	dB
	F = F0 - 1 MHz	π/4 DQPSK	-	-10	0	≤0	dB
		8DPSK	-	-5	5	≤5	dB
	F = Fimage (F0 + 2 MHz)	π/4 DQPSK	-	-34	-7	≤-7	dB
		8DPSK	-	-24	0	≤0	dB
	F = F0 - 2 MHz	π/4 DQPSK	-	-41	-30	≤-30	dB
		8DPSK	-	-38	-25	≤-25	dB
	F = FImage + 1 MHz	π/4 DQPSK	-	-43	-20	≤-20	dB
		8DPSK	-	-37	-13	≤-13	dB
	F = F0 - 3 MHz	π/4 DQPSK	-	-48	-40	≤-40	dB
		8DPSK	-	-42	-33	≤-33	dB

2.2.3 LE 1Mb/s(Conducted)

Transmitter

RF Characteristics, VBAT = 3.3 V		Min	Typ	Max	Bluetooth Specification	Unit
Maximum RF transmit power		-	5	-	-20 to10	dBm
In-band spurious emissions	F = F0 ± 2 MHz	-	-28	-20	≤-20	dBm
	F = F0 ± 3 MHz	-	-47	-30	≤-30	dBm
	F = F0 ± > 3 MHz	-	<-61	-30	≤-30	dBm
Δf1avg maximum modulation		225	264	275	225 < f1avg < 275	kHz
Δf2max minimum modulation		185	235	-	≥185	kHz
Δf2avg/Δf1avg		0.8	0.92	-	≥0.80	-
Maximum carrier frequency offset		-20	3	150	<150	kHz
Maximum drift rate		-	4	20	≤20	kHz/50 μs
Carrier drift		-	6	50	≤50	kHz
2nd harmonic content		-	-29	-	-	dBm
3rd harmonic content		-	-22	-	-	dBm

Receiver

RF Characteristics, VBAT = 3.3 V	Frequency (GHz)	Min	Typ	Max	Bluetooth Specification	Unit
Sensitivity at 0.1% BER for all basic rate packet types	2.402	-	-92	-	≤-70	dBm
	2.44	-	-92	-		
	2.48	-	-92	-		
Reported PER during PER report integrity test	2.426	50	50	65.4	50 < PER < 65.4	%
Maximum received signal at 30.8% PER		-10	>-9	-	≥-10	dBm
Continuous power required to block Bluetooth reception (for input power of -67 dBm with 30.8% PER)	0.030 - 2.000	-30	>3	-	-30	dBm
	2.000 - 2.400	-35	-2	-	-35	
	2.500 - 3.000	-35	2	-	-35	
	3.000 - 12.75	-30	>5	-	-30	
C/I co-channel		-	6	21	≤21	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	-	-11	15	≤15	dB
	F = F0 - 1 MHz	-	-8	15	≤15	dB
	F = Fimage (F0 + 2 MHz)	-	-34	-9	≤-9	dB
	F = F0 - 2 MHz	-	-39	-17	≤-17	dB
	F = Fimage + 1 MHz	-	-45	-15	≤-15	dB
	F = F0 - 3 MHz	-	-51	-27	≤-27	dB
Maximum level of intermodulation interferers		-50	-40	-	≥-50	dBm
Spurious output level		-	-155	-	-	dBm/Hz

2.3 Audio Characteristics

2.3.1 High-quality (HQADC) single-ended audio input

Parameter	Conditions	Min	Typ	Max	Unit
Output Sample Width	-	-	-	24	Bits
Output Sample Rate, F_{sample}	-	8	-	96	kHz
Input level	-	-	-	2.4	V pk-pk
Input impedance	0 dB to 24 dB analog gain	-	20	-	kΩ
	27 dB to 39 dB analog gain	-	10	-	kΩ
SNR	f_{in} = 1 kHz 48 kHz A-Weighted THD+N < 0.1% 2.4 V pk-pk input (0 dB gain)	-	101	-	dBA
THD+N	f_{in} = 1 kHz 48 kHz 2.4 V pk-pk input (0 dB gain)	-	-85	-	dB
Digital gain	Digital gain resolution = 1/32	-24	-	21.5	dB
Analog gain	3 dB steps	0	-	39	dB
Stereo separation (crosstalk)	-	80	-	-	dB

2.3.1 High-quality (HQADC) differential audio input

Parameter	Conditions	Min	Typ	Max	Unit
Output Sample Width	-	-	-	24	Bits
Output Sample Rate, Fsample	-	8	-	96	kHz
Input level	-	-	-	2.4	V pk-pk
Input impedance	0 dB to 24 dB analog gain	-	20	-	kΩ
	27 dB to 39 dB analog gain	-	10	-	kΩ
SNR	fin = 1 kHz 48 kHz A-Weighted THD+N < 0.1% 2.4 V pk-pk input (0 dB gain)	-	100	-	dBA
THD+N	fin = 1 kHz 48 kHz 2.4 V pk-pk input (0 dB gain)	-	-91	-	dB
Digital gain	Digital gain resolution = 1/32	-24	-	21.5	dB
Analog gain	3 dB steps	0	-	39	dB
Stereo separation (crosstalk)	-	80	-	-	dB

2.3.3.Class-AB DAC: digital-to-analog converter

Parameter	Conditions	Min	Typ	Max	Unit
Input Sample Width	-	-	-	24	Bits
Input Sample Rate, Fsample	-	8	-	192	kHz
Output Power	0 dBFS, 32 Ω load	-	-	30	mW
	-3 dBFS, 16 Ω load				
Load	-	16	32	30k	Ω
SNR	f_{in} = 1 kHz 48 kHz Fsample B/W = 20 Hz → 20 kHz A-Weighted 0 dBFS 32 Ω load	-	101	-	dBA
THD+N	fin = 1 kHz 48 kHz B/W = 20 Hz → 20 kHz -1 dBFS 32 Ω load	-	-90.5	-	dB
Digital gain	Digital gain resolution = 1/32	-24	-	21.5	dB
Stereo separation (crosstalk)	-	80	-	-	dB

2.4 ESD Protection

Test	Pins	Specification	Class
Human Body Model	AIO/LED[5, 2:0]	JS-001-2017	1C (1000 V)
	All other pins	JS-001-2017	2 (2000 V)
Charge Device model	All pins	JS-002-2014	C2a (500 V)
System Level ESD	▪ USB_DN ▪ USB_DP ▪ AUDIO_MIC1_N/ LINEIN_L_N ▪ AUDIO_MIC1_P/ LINEIN_L_P ▪ AUDIO_MIC2_N/ LINEIN_R_N ▪ AUDIO_MIC2_P/ LINEIN_R_P	IEC 61000-4-2 (device level)	Level 4 (8 kV contact / 15 kV air)

3. Interface

3.1 UART interface

F1DQ3021 has a standard UART serial interface that provides a simple mechanism to communicate with other serial devices using the RS232 protocol. The UART interface multiplexes with PIOs and other functions. Hardware flow control is optional. Table 5-1 lists possible UART settings.

3.1.1 Table 5-1 UART configuration options

Parameter		Possible value
Baud rate	Minimum	2400 Bd (≤2%Error)
		19,200 Bd (≤1%Error)
	Maximum	4 MBd (≤1%Error)
Flow control		RTS/CTS or None
Parity		None, Odd, or Even
Number of stop bits		1 or 2
Bits per byte		8

3.2 USB interface

F1DQ2031 has a USB device interface: An upstream port, for connection to a host Phone/PC

or battery charging adaptor.

For details software support for USB features, refer to ADK documentation.

3.2.1 USB Device port

The device port is a USB2.0 Full Speed (12 Mb/s) port. TypicallyF1DQ3021 enumerates as a compound device with a hub with the enabled audio source / sink / HID / mass storage device appearing behind this hub.

The DP 1.5 k pull-up is integrated inF1DQ3021. No series resistors are required on the USB data lines.
F1DQ3021 contains integrated ESD protection on the data lines to IEC 61000-4-2 (device level). In normal applications, no external ESD protection is required.

Extra ESD protection is not required on VCHG (VBUS) becauseF1DQ3021 meets the USB certification requirements of a minimum of 1uF, and a maximum of 10 µF being present on VCHG (VBUS).

The VCHG input of F1DQ3021 is tolerant of a constant 6.5 V and transients up to 7.0 V. If extra overvoltage protection is required, external clamping protection devices can be used.

3.3 Transaction bridge

The transaction bridge is an external bridge into the internal transaction bus between F1DQ3021 subsystems. It is the primary debug interface and can also be used for production programming. A USB to transaction bridge interface (TRBI200) is available.

> NOTE   A direct USB2.0 connection from a host computer to theF1DQ3021 can be used for most debugging and programming activities. For more details, see ADK documentation.

TRBI200 can use USB3.0 for maximum data rate.

> NOTE   USB3.0 signals can generate noise in the Bluetooth ISM band. For applications where sensitive RF measurements take place, QTIL recommends connecting TRBI200 using USB2.0.

The transaction bridge is a multilane interface, and only requires three wires for its minimum configuration (suitable for production programming).

> NOTE   The TRBI200 USB transaction bridge interface requires power for input/output buffers to be supplied externally. This voltage must match the power supply domain used for the TRB pads (VDD_PADS2).

> NOTE not for   Minimum configuration is sufficient for production programming and code download, but extensive debug and code tracing. The configuration in use is automatically detected.

TRB	PIO	Required for minimum configuration	Intermediate configuration	Full bus width
TBR_CLK	PIO[8]	Yes	Yes	Yes
TBR_MISO[0]	PIO[7]	Yes	Yes	Yes
TBR_MOSI[0]	PIO[6]	Yes	Yes	Yes

> NOTE   PIO[7] should not be held low during boot.

3.4 LED drivers

F1DQ3021 includes a 4-pad synchronized PWM LED driver for driving RGB LEDs for producing a wide range of colors. All LEDs are controlled by firmware. The terminals are open-drain outputs, so the LED must be connected from a positive supply rail to the pad in series with a current-limiting resistor.

3.5 Audio Interfaces

F1DQ3021's audio interface consists below.

■ Dual analog audio in/outputs

■ 2 digital microphone input

■ 1 configurable I²S interfaces

■ Configurable SPDIF input interface
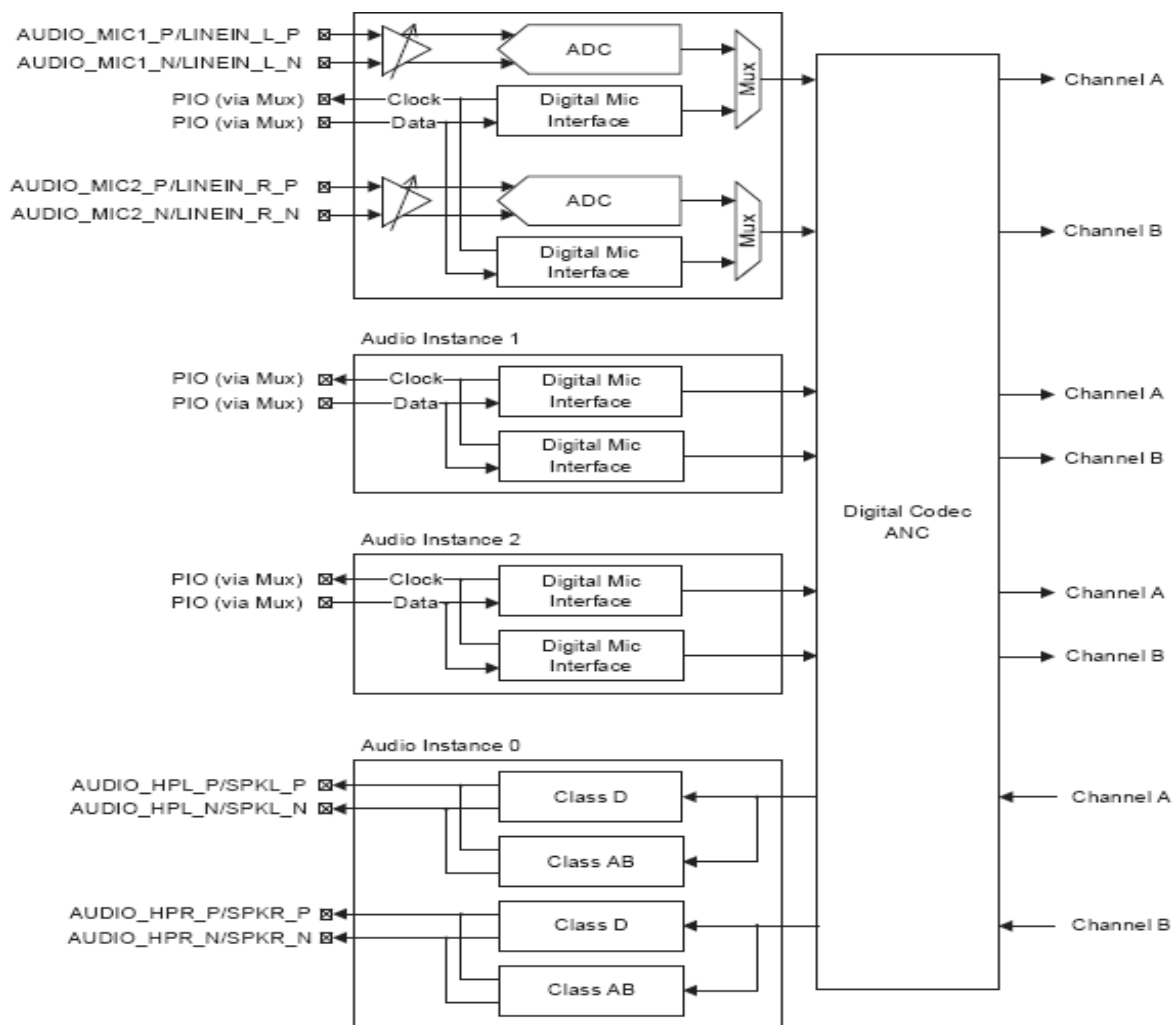
3.5.1 Analog Input

F1DQ3021 analog interfaces include:

- Line/Mic inputs
- Line/Headphone outputs

F1DQ3021 contains an independent low-noise microphone bias generator. In using Line input, F1DQ3021 supports a differential input and a single-ended input.
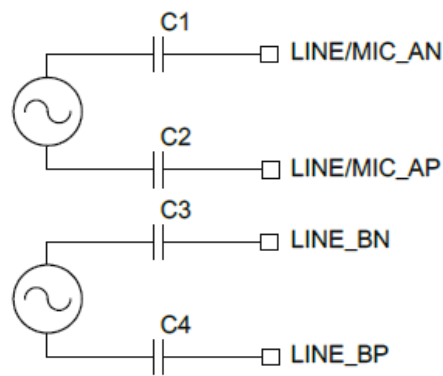
■ Differential input
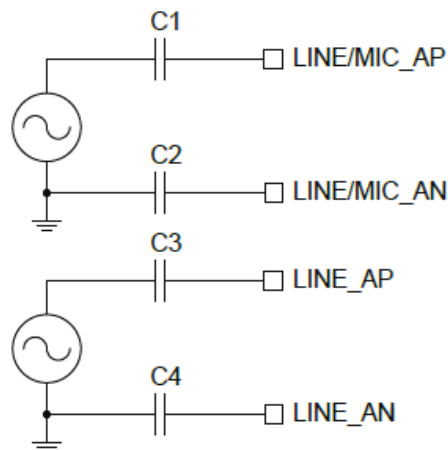
■ Single-ended input

3.5.2 Audio Output

The output stage digital circuitry converts the signal from 16 bit per sample, linear PCM of variable sampling frequency to bit stream, which is fed into the analog output circuitry.

The analog output circuit comprises a DAC, a buffer with gain-setting, a low pass filter, and a class AB output stage amplifier.
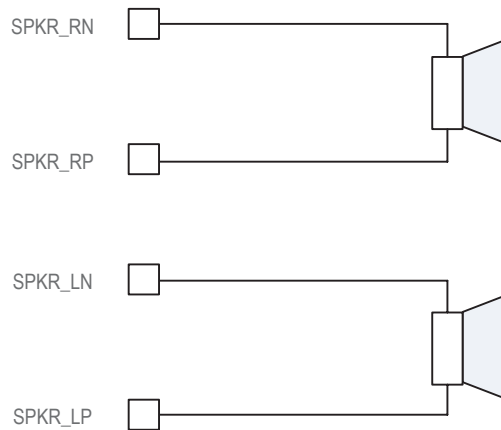
Mono operation is a single-channel operation of the stereo codec. The left channel represents the single mono channel for audio in and audio out. In mono operation, the right channel is the auxiliary mono channel for dual-mono channel operation

3.5.3 Standard I²S/PCM interface

F1DQ3021 provides a standard I²S/PCM interface capable of operating at up to a 192 kHz sample rate. The I²S/PCM port is highly configurable with alternate PCM modes, and has the following options:

- SYNC edge position selectable to align with start of channel data (PCM mode), or 1 clock before start of channel data (I²S mode)
- Master (generate CLK and SYNC) or Slave (receive CLK and SYNC) (PCM/I²S)
- SYNC polarity (PCM)
- Long or short SYNC (PCM)
- Left or right justification (PCM/I²S)
- Sign extension / zero pad (PCM)
- Optional tri-state at end of word (PCM)
- Optional invert of clock (PCM/ I²S)
- 13/16/24-bit per sample (PCM/ I²S)
- Up to four slots per frame (PCM)

F1DQ3021 pin name	PCM signal	I²S signal	Description
PCM_DIN	PCM_DIN	I2S_DIN / SDIN / ADCDAT	Data input
PCM_DOUT	PCM_DOUT	I2S_DOUT / SDOUT / DACDAT	Data output
PCM_SYNC	PCM_SYNC	I2S_FS / WS / LRCLK	Word sync
PCM_CLK	PCM_CLK	I2S_CLK / SCK / BCLK	Bit clock

3.5.4 SPDIF interface

SPDIF (IEC 60958) is a digital audio interface. It uses biphase coding to minimize the DC content of the transmitted signal, and enables the receiver to decode clock information from the transmitted signal.F1DQ3021 has up to two SPDIF interfaces configurable as input or output. These interfaces are compatible with IEC 60958-1, IEC 60958-3, IEC 60958-4, and AES/EBU standards.

Signals are input/output via PIO and typically require external line drivers (for 75 Ω cabling) or optical transceivers ('Toslink'). Any PIO is assignable for SPDIF use.

3.6 Reset, RST#

The F1DQ3021 digital reset pin (RESET#) is an active low reset signal. PIO[1] defaults to RESET# upon boot.
The pin is active low and on-chip glitch filtering avoids the need to filter out any spurious noise that may cause unintended resets. The RESET# pin has a fixed strong pull-up to VDD_PADS_1, and therefore can be left unconnected. The input is asynchronous, and is pulse extended within F1DQ3021 to ensure a full reset.

F1DQ3021 contains internal Reset Protection functionality to automatically keep the power rails enabled and enable the system to restart after unintended reset (such as a severe ESD event). Assertion of RESET# beyond the Reset Protection timeout (typically greater than ~1.8 s) causes the device to power down if VCHG is not present and SYS_CTRL is low.F1DQ3021 then requires a SYS_CTRL assertion or VCHG attach to restart.

> **NOTE** F1DQ3021 is always powered if VCHG is present. It does not power down if RESET# is asserted while VCHG remains present.
> QTIL recommends thatF1DQ3021 is powered down via software-controlled methods rather than external assertion of RESET#.

Holding RESET# low continuously is not the lowest F1DQ3021 power state, because pull downs are enabled on VCHG and VDD_BYP in this state.

RESET# is guaranteed to work if held low for 120 µs.

After boot, PIO[1] is configurable as a digital PIO.

3.7 SYS_CTRL pin

SYS_CTRL is an input pin that acts as a power on signal for the internal regulators. It can also be used as an input (appears to software as virtual PIO[0]) or as a multifunction button.

From the OFF state, SYS_CTRL must be asserted for >20 ms to start power up.

SYS_CTRL is VBAT tolerant (4.8 V max), and typically connected via a button to VBAT. SYS_CTRL has no internal pull resistor, and requires an external pull-down if left undriven.

SYS_CTRL can be logically disconnected from the power on signal for internal regulators by software. Therefore, for example, once booted, software takes control of the internal regulators and the state of SYS_CTRL is ignored by the regulators.

3.8   LED pads

F1DQ3021 contains LED pads that are configurable in four different operating modes:

1. LED Driver: This mode is designed for driving LEDs. The pad operates as an open-drain pad, tolerable of voltages up to 7.0 V. Therefore the cathode of the LED should be connected to theF1DQ3021 LED pad. Each pad is rated to sink up to 50 mA of current.

2. Digital / Button input: This mode is designed for slow input signals, typically buttons. It is not designed for fast switching digital inputs like SPI. For these types of inputs, use the standard PIOs.

   In this mode, an internal weak pull-down can be enabled. Typically this is used for active high button signals to ensure that the input returns to 0 when the button is released. The pads are 7.0 V tolerant and the logic 1 threshold is typically 1 V.

   In digital input mode, the logic inputs can be read by the software as virtual PIO[71, 68:66].

3. Analog input: In this mode, the LED pad is used as an analog input port. The pad voltage is routable to a 10‑bit auxiliary ADC.

4. Disabled: This is the default state for LED pads, where the pad is 7.0 V tolerant and a high impedance with no pull-down.

   NOTE   LED[1] pin will be driven to ground level for up to 6 ms within 50 ms of the chip powering up from off state or after chip reset being released.

   Other LED pins might be driven to ground level for up to 300 µs within 50 ms of the chip powering up from off state.

4. Li-ion charger

The F1DQ3021 Li-ion charger is designed to support small to large batteries (several Amp hours). It is connectable in one of two modes:

- Internal configuration: Supporting charge rates of 2 mA to 200 mA with no external components required.

- External configuration: Supporting charge rates of 200 mA to 1800 mA with the addition of one PNP pass device and external resistor.

4.1 General charger operation

Trickle charge

This mode is entered when VBAT is sensed in the range 0 to Vpre. This is encountered only with a deeply discharged battery (below Vpre threshold, point (A)), or when the cell's battery protection circuit has opened, temporarily disconnecting the cell. It is used to pass a small charging current to safely charge a cell, and also cause a cell battery protection circuit to reset.
The hysteresis on Trickle charge into Pre-Charge is typically 100 mV.
During Trickle charge,F1DQ3021 controls charge current internally. The external pass transistor is not used.

Parameters in Trickle charge

Parameter	Description	Min	Typ	Max
Vpre threshold (A)	Voltage at which the charger transitions out of Trickle charge into Pre-charge.	2.0 V	2.1 V	2.2 V
Itrick	Trickle charge current.	1 mA	-	50 mA

4.2 Pre-charge

This mode is entered when VBAT is sensed in the range Vpre to Vfast. In this range, it is not recommended to charge the cell at maximum rate, but a faster charge rate than that of Trickle charge is allowable. Typically this is ~10 % to 20 % of the Fast charge rate. The Vfast threshold, point (B) is programmable.

The hysteresis on the Vfast transition from Pre-Charge to Fast charge is typically 200 mV.
During Pre-Charge,F1DQ3021 controls the charge current internally and the external pass transistor is not used.

Parameters in Pre-charge

`	Description	Min	Typ	Max
Vfast threshold (B)	Voltage at which the charger transitions out of Pre-charge into Fast charge.	0=2.8V 1=2.9V 2=3.0V 3=2.4V	0=2.9V 1=3.0V 2=3.1V 3=2.5V	0=3.0V 1=3.1V 2=3.2V 3=2.6V
Ipre	Pre-charge current.	2 mA	-	200 mA

4.3 Fast charge

Fast charge has two parts:

- **Constant current**: Entered when VBAT is sensed in the range Vfast to Vfloat point (C). This is the maximum charge rate, and should be set according to the battery manufacturers Data Sheet.

- **Constant voltage**: When Vfloat is reached the cell voltage is maintained at Vfloat, and the current slowly reduces until the termination point (E) is reached where charging ceases, and the charger transitions to Standby mode.

Vfloat can be configured from 3.65 V to 4.40 V in 50 mV increments. This allows use of cells with different Vfloat values, or cell life extension by reducing Vfloat. Vfloat can also be altered depending on temperature change, for cell life protection.

The current termination point (E) can be adversely influenced by dynamic changes in VBAT load current, or to a lesser extent changes in VCHG voltage.

Parameters in Fast charge

Parameter	Description	Min	Typ	Max
Ifast	Ifast Fast charge current (Internal mode).	2 mA	-	200 mA
Ifast	Ifast Fast charge current (External mode).	-	-	1.8 A
Termination point (E)	Transition from fast charge (constant voltage) to Standby. Expressed as % of Ifast.	-	0=10 1=20 2=30 3=40	-

4.4 Standby mode

Once the charge current has fallen and the charger is terminated, the system enters Standby mode. In Standby mode, the charger does not charge. It continues to monitor the battery voltage. If the voltage falls back below Vfloat by more than a configurable threshold Vhyst, point (D), then the charger re-enters Fast charge mode. Vhyst is expressed as a percentage of Vfloat.

Parameter	Description	Min	Typ	Max
Vhyst threshold (D)	Percentage of Vfloat at which the charger moves from Standby back to Fast charge.	0=1.8	0=2.4	0=3.0
		1=3.0	1=3.6	1=4.2
		2=4.2	2=4.8	2=5.4
		3=5.4	3=6.0	3=6.5

5. Application Schematic
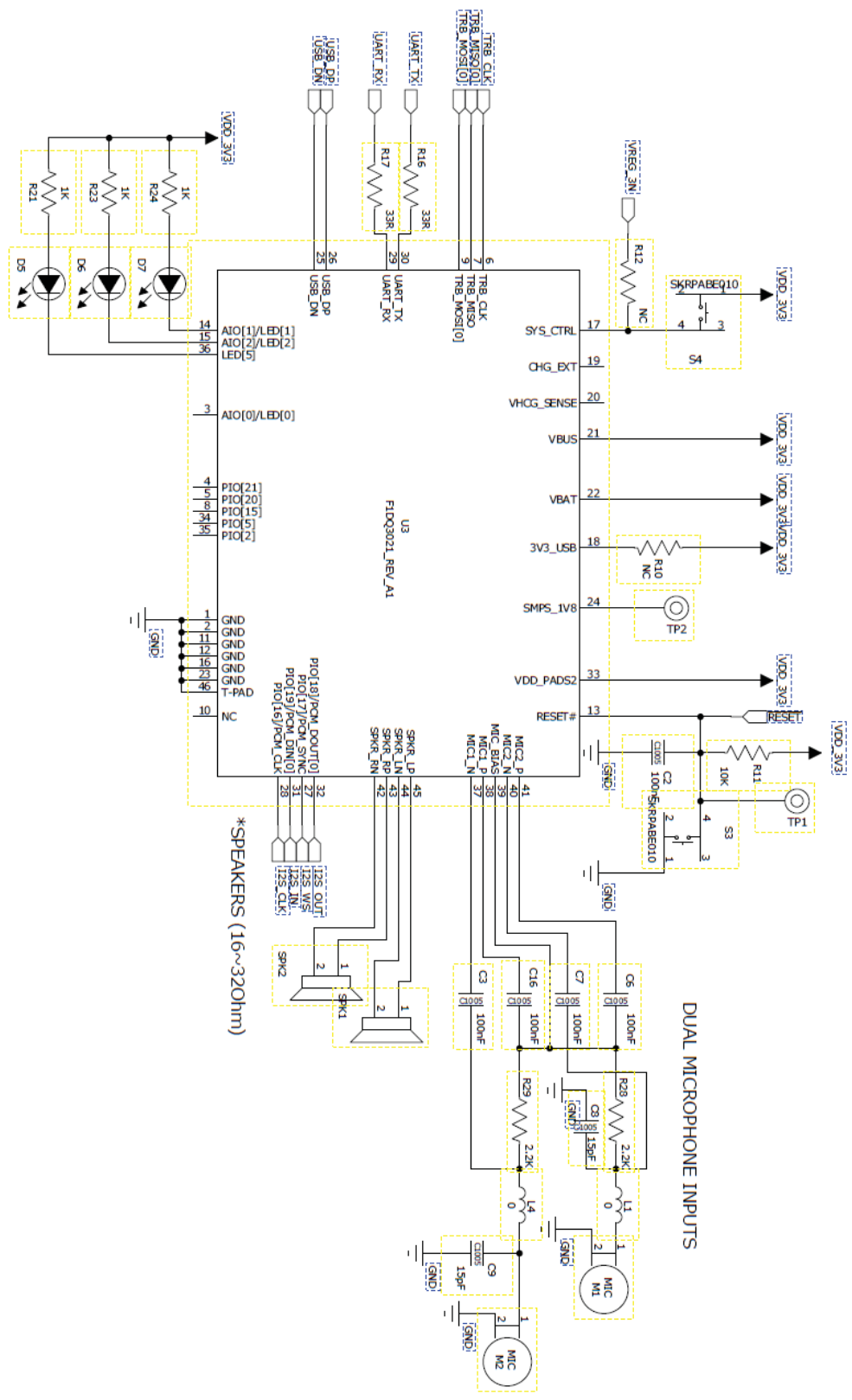
6. Antenna spec
Active measurement data(Anam ES B'D)

VSWR   S11

TIS

Ch1. TIS 3D Graph.

Ch2. TIS 3D Graph.

Ch3. TIS 3D Graph.

TRP

Ch1. TRP 3D Graph.

Ch2. TRP 3D Graph.

Ch3. TRP 3D Graph.
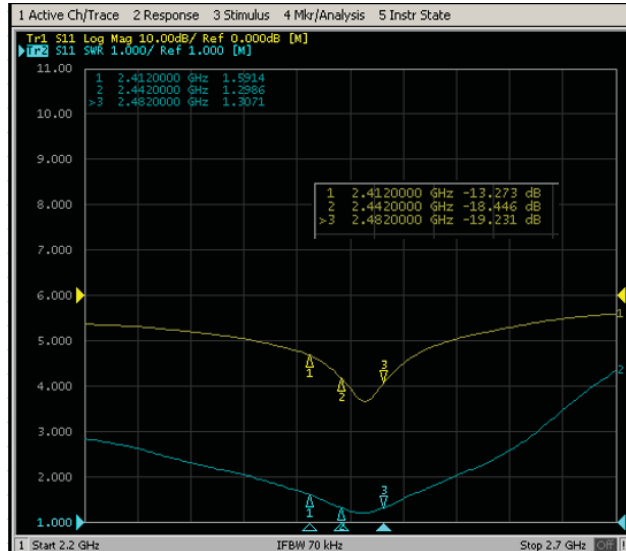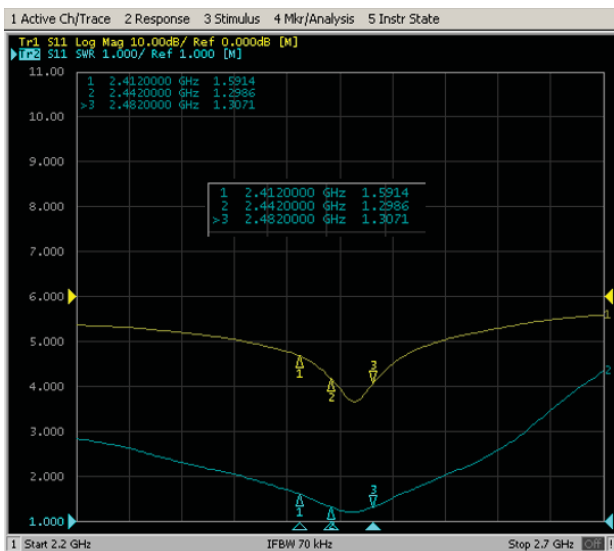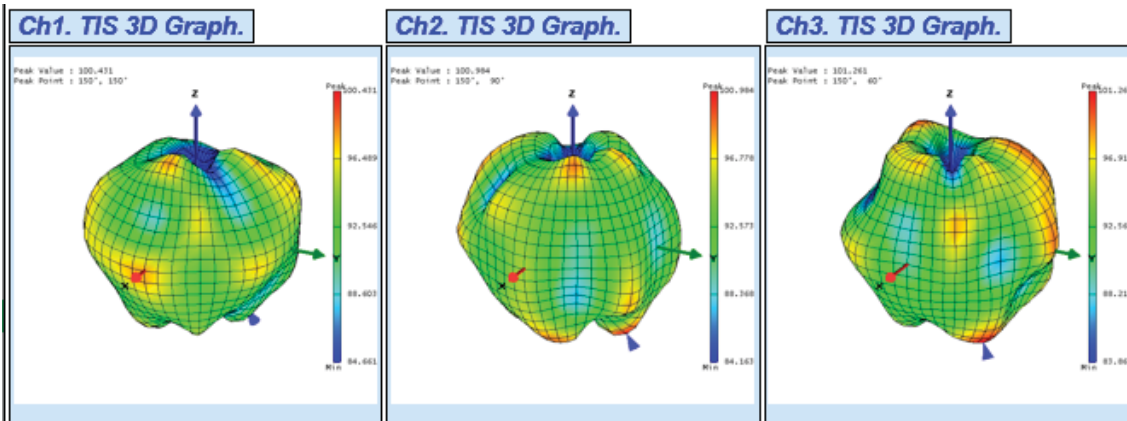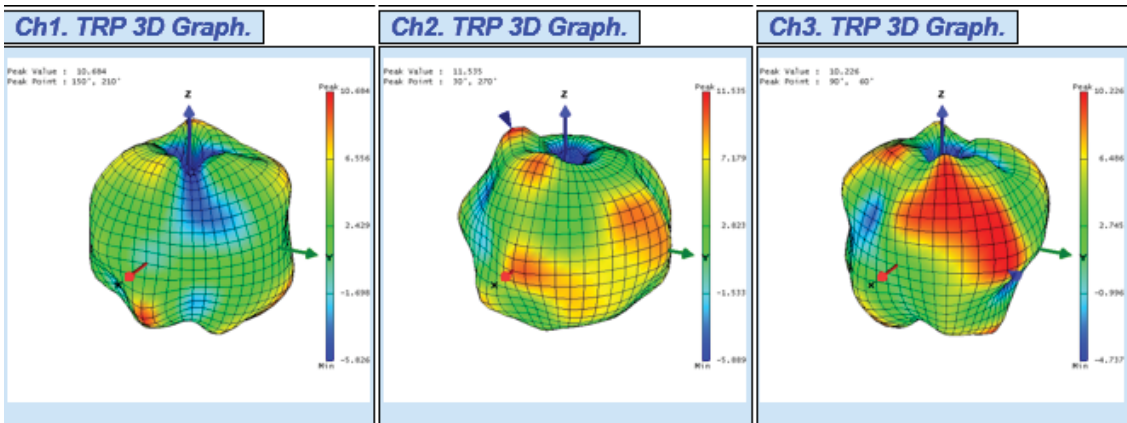
7. Module Placement Rule

On the main PCB, the areas under the antenna should not contain any top, inner layer, or bottom copper as shown in Figure. For the best range performance, keep all external metal away from the chip antenna at least 45 mm. In all cases, the performance of the antenna can vary depending on GND.
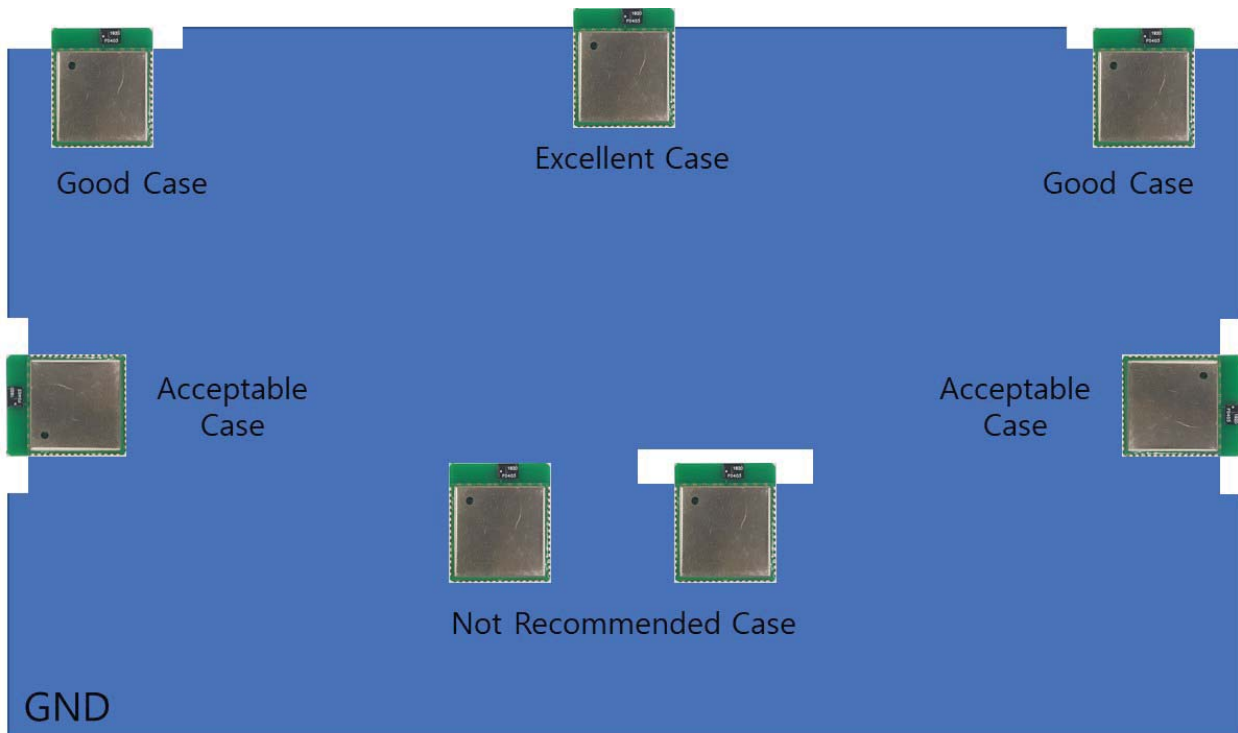
8. PCB Layout

F1DQ3021_Rev0.1_Layout

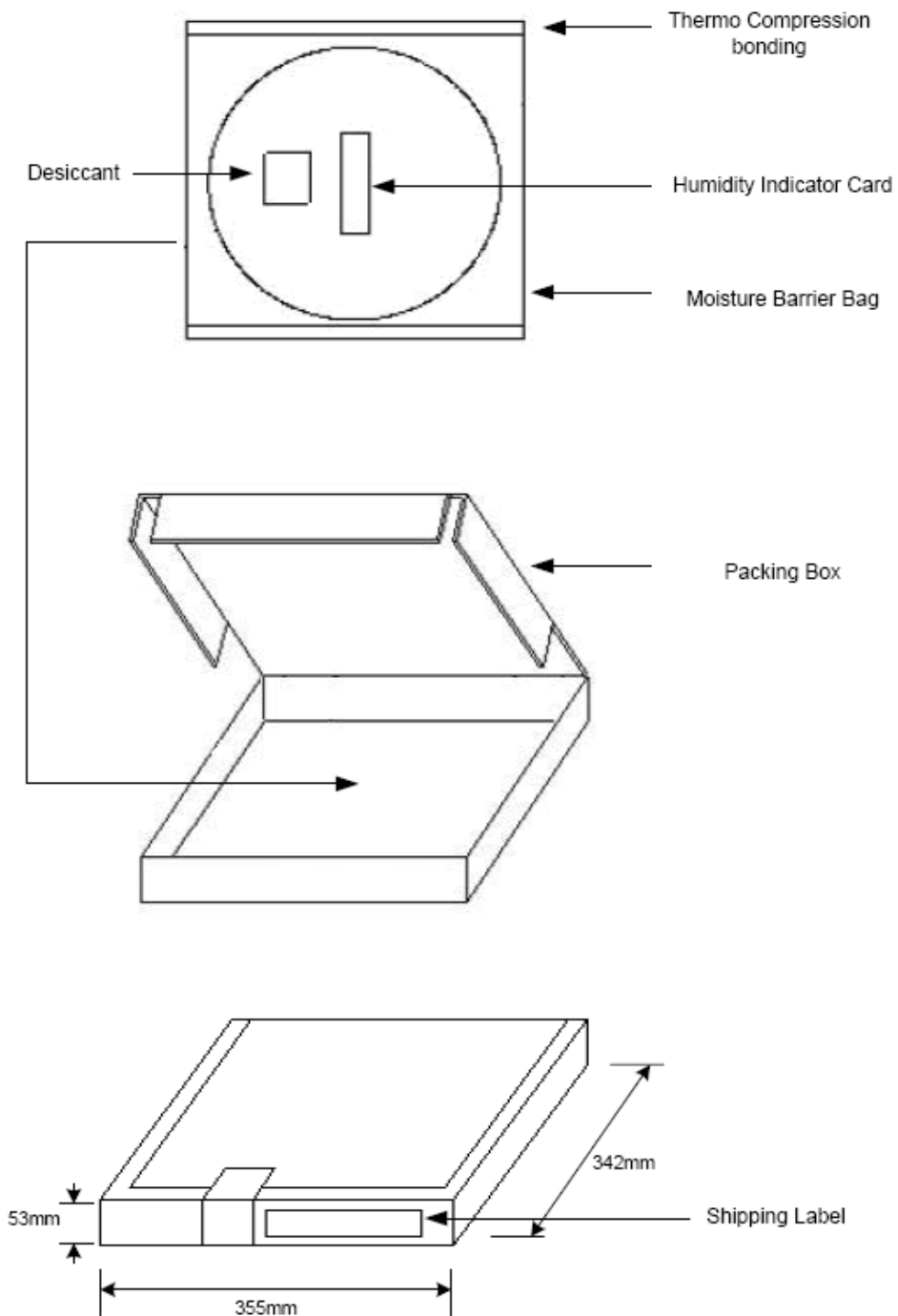### 1. Top View (Unit : mm)
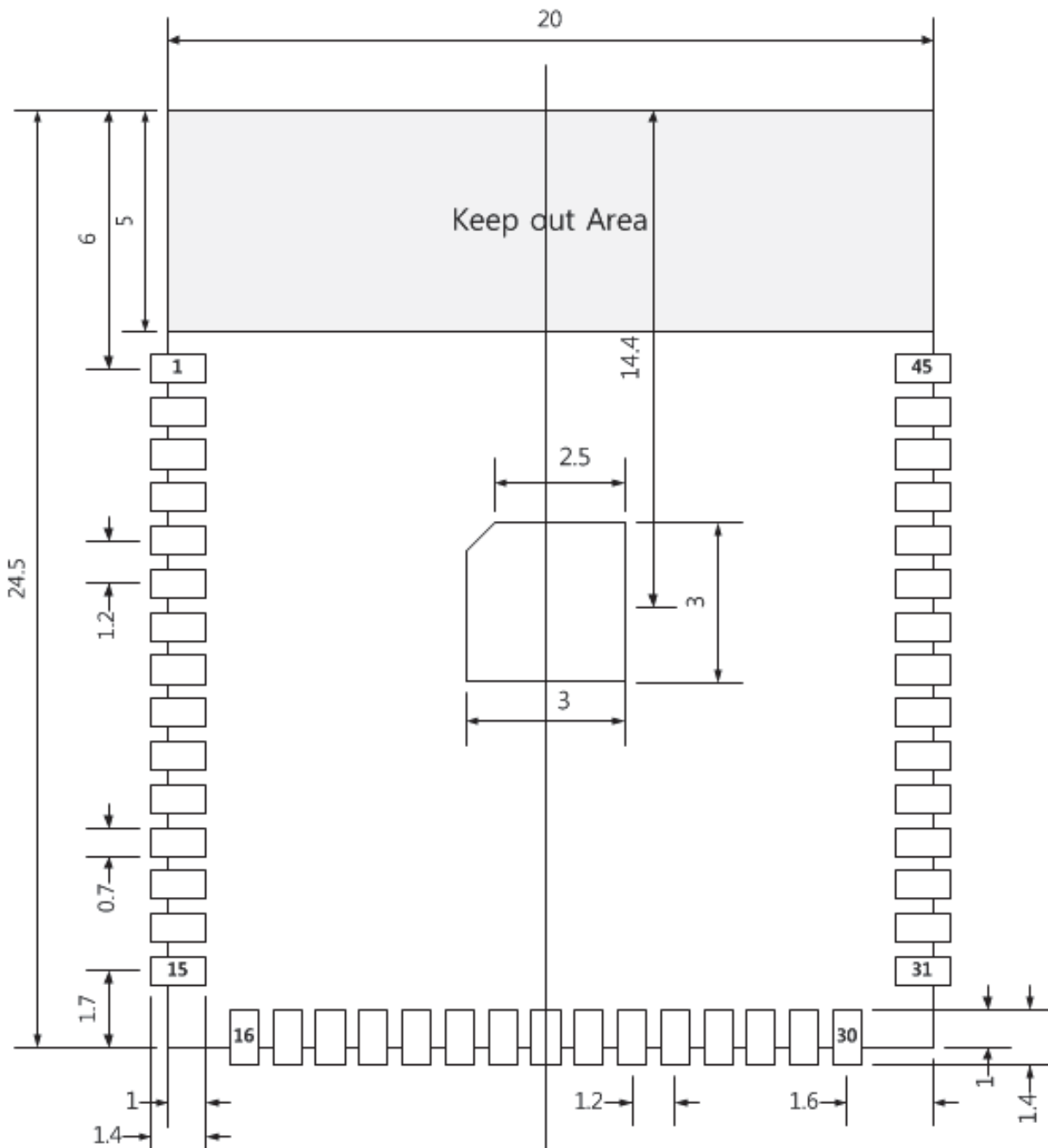
9 Reflow Temperature Profile

Temperature

Peak: 245±5℃, 10sec max.

245℃

3℃/sec ↓

220℃

3℃/sec ↓
Peak ℃ ~ 120 ℃

200℃

130℃

30~60 sec

60~120 sec

3℃/sec ↓   Pre-heating   Reflow   Cool down   t [sec]
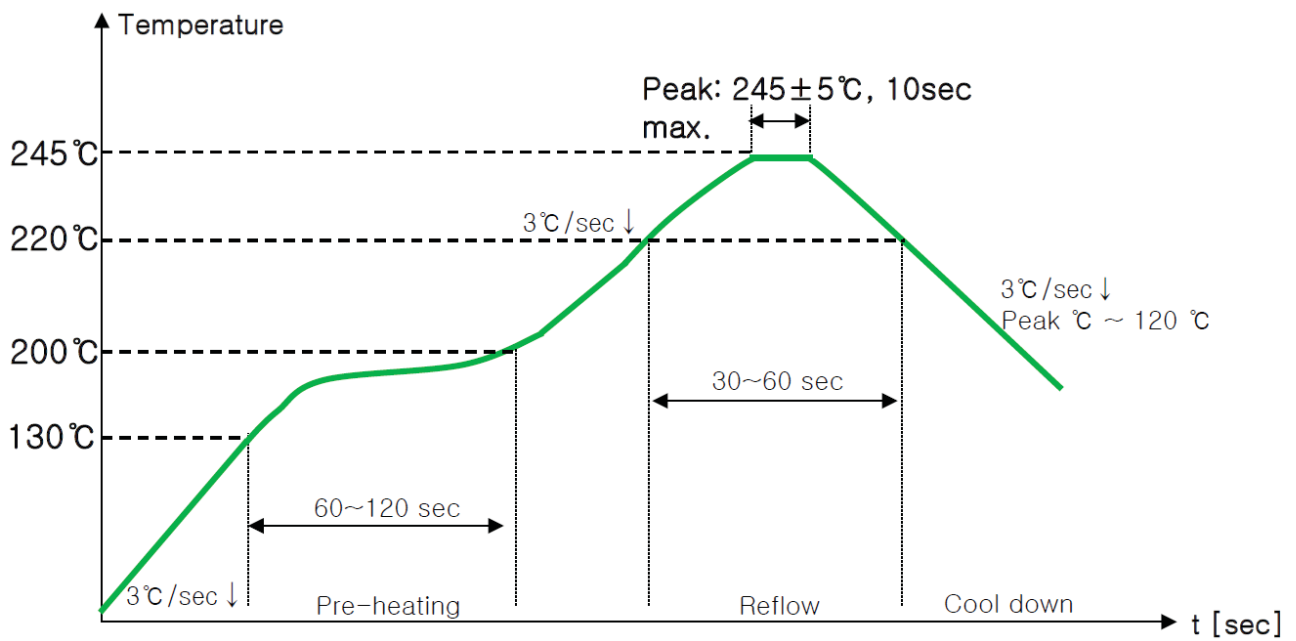
- Please use the reflow within 2 times.

10.Packing information
10-1. Reel Specification

10-2. Box Specification

Thermo Compression bonding

Desiccant

Humidity Indicator Card

Moisture Barrier Bag

Packing Box

342mm

53mm

Shipping Label

355mm
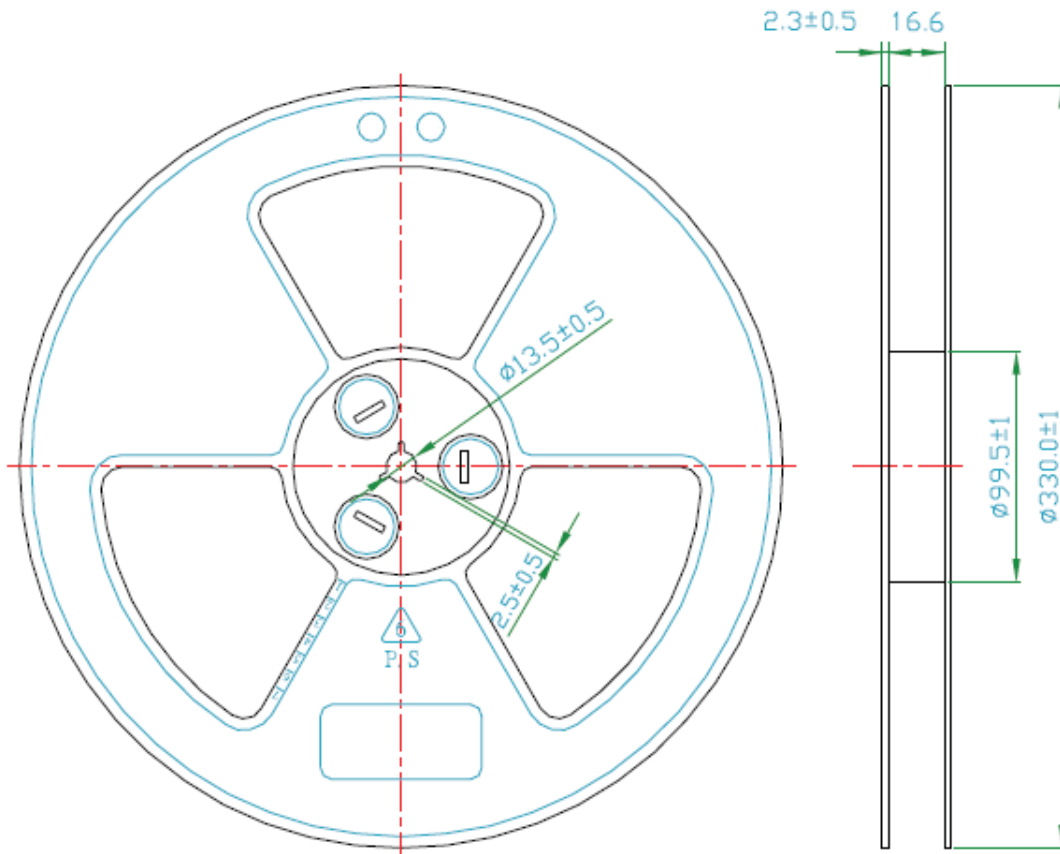
Qty of goods : 700 pcs / Reel

10-3. Barcode
- Product Label

MODEL : F1DQ3021
FCC ID : XXXXXXXXXX
IC : XXXXXX-XXXXXXXX
CMIIT ID: XXXXXXXXXX
INPUT : 3.3V⎓, 15mA

CE

X-X-XXX-XXXXXXXX ANATEL
XXXXX-XX-XXXXX
XXXXXXXXXXXXXX

KC

XXX-XXXXX

Made in Korea
Anam Electronics Co, Ltd.

- Gift box Label

MPN : F1DQ3021

Customer No : 091(아남)

Firmware Version : v1.xx

Lot No : F1A000

F1media
F1 of mobile multimedia

DTE : C1XXXX

QTY:700

V RoHS

- Carton box Label

MPN : F1DQ3021

Customer No : 091(아남)

Firmware Version : v1.xx

Lot No : F1A000

F1media
F1 of mobile multimedia

DTE : C1XXXX

QTY:7000

V RoHS

10- 4. Box Packing
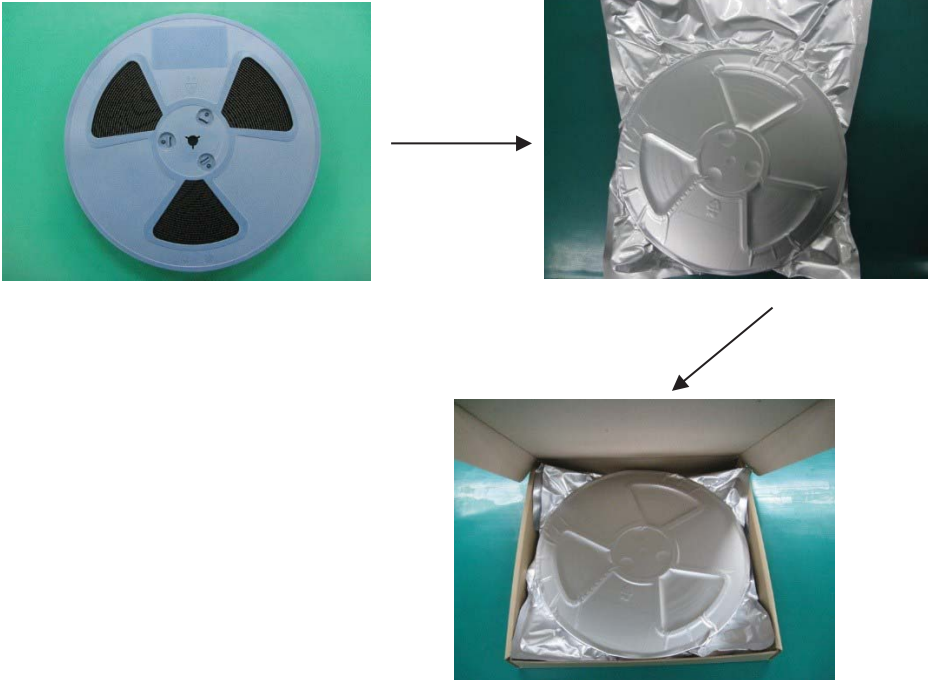
10-5. Carton Box

– **Carton Box Size**

	Carton Box			
	W(mm)	D(mm)	H(mm)	Q'ty
#1	630	360	370	7,000
#2	375	320	360	3,500

11.Revision History

Revision	Date	Change Descriptions	Issued by
Rev A1	2021-07-26	Initial release	T.G.KIM
Rev A2	2021-07-28	Modify PCB Layout	T.G.KIM
Rev A3	2021-11-09	Add Power Consumption, RF Characteristics, Antenna spec and packing information Modify Device Terminal Functions.	T.G.KIM
Rev A4	2021-11-11	Modify Pinout diagram	T.G.KIM
Rev A5	2021-11-11	Remove LE 2M SEPC	T.G.KIM

Installation Procedure
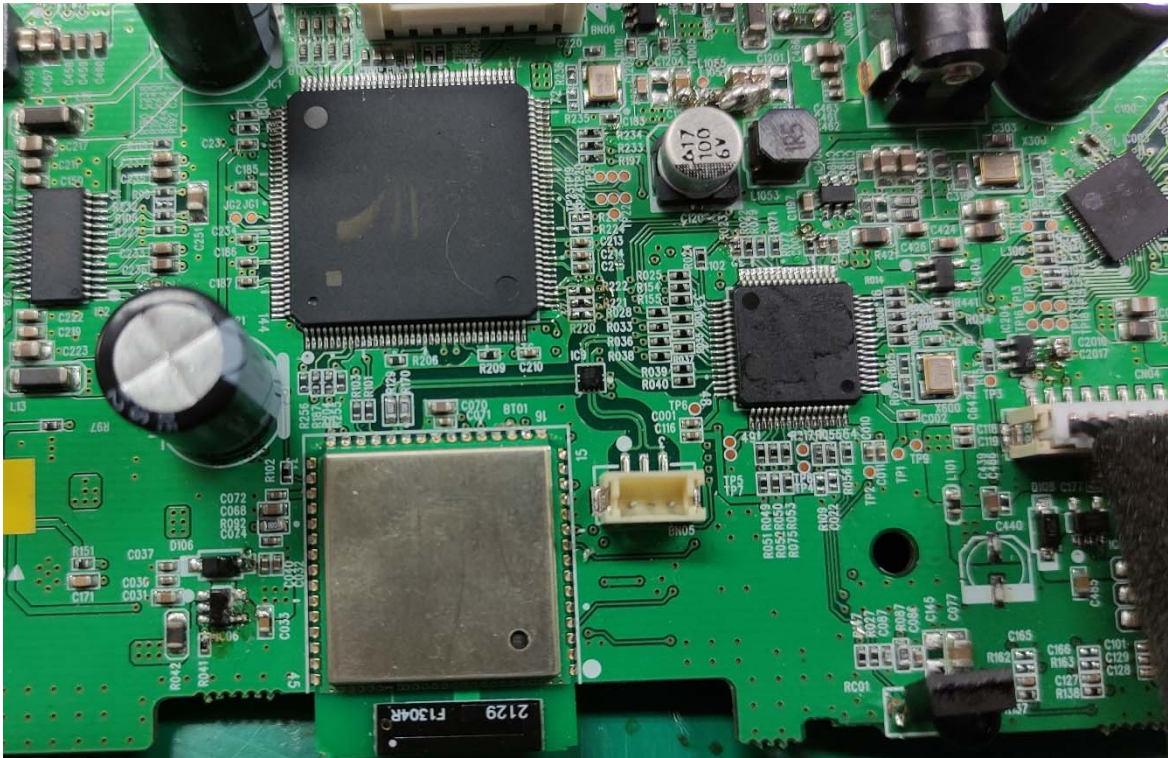
FCC Statement

FCC Part 15C 15.247, 15E 15.407 is applied to the modular transmitter.

Federal Communication Commission Interference Statement
This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

● Reorient or relocate the receiving antenna.

● Increase the separation between the equipment and receiver.

● Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

● Consult the dealer or an experienced radio/TV technician for help.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following

two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

FCC Caution: Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

This device and its antenna(s) must not be co-located or operation in conjunction with any other antenna or transmitter.

IMPORTANT NOTE:

FCC Radiation Exposure Statement:
This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment.

This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

This module is intended for OEM integrator. The OEM integrator is still responsible for the FCC compliance requirement of the end product, which integrates this module.

USERS MANUAL OF THE END PRODUCT:

In the users manual of the end product, the end user has to be informed to keep at least 20cm separation with the antenna while this end product is installed and operated. The end user has to be informed that the FCC radio-frequency exposure guidelines for an uncontrolled environment can be satisfied. The devices must be installed and used in strict accordance with the manufacturer's instructions as described in the user documentation that comes with the product.The end user has to also be informed that any changes or modifications not expressly approved by the manufacturer could void the user's authority to operate this equipment. If the device is small or for such use that it is not practicable to place the statement on the product, then additional FCC part 15.19 statement is required to be available in the users manual: This device complies with Part 15 of FCC rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference and (2) this device must accept any interference received, including interference that may cause undesired operation.

LABEL OF THE END PRODUCT:

The final end product must be labeled in a visible area with the following " Contains FCC ID: MBBF1DQ3021 ". If the device is small or for such use that it is not practicable to place the statement on the product, then the following FCC part 15.19 statement has to also be available on the label: This device complies with Part 15 of FCC rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference and (2) this device must accept any interference received, including interference that may cause undesired operation.

IC Statement

This Class B digital apparatus complies with Canadian ICES-003.

This device complies with Industry Canada license-exempt RSS standard(s).

Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Cet appareil numérique de la classe B est conforme á la norme NMB-003 du Canada.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Any changes or modifications not expressly approved by the manufacturer could void the user's authority to operate this equipment.

This device and its antenna(s) must not be co-located or operation in conjunction with any other antenna or transmitter.

The device could automatically discontinue transmission in case of absence of information to transmit, or operational failure. Note that this is not intended to prohibit transmission of control or signaling information or the use of repetitive codes where required by the technology.

IMPORTANT NOTE:

IC Radiation Exposure Statement

This equipment complies with IC RSS-102 radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

Cet équipement est conforme aux limites d'exposition aux rayonnements IC établies pour unenvironnement non contrôlé. Cet équipement doit être installé et utilisé avec un minimum de 20cm de distance entre la source de rayonnement et votre corps.

This module is intended for OEM integrator. The OEM integrator is still responsible for the IC compliance requirement of the end product, which integrates this module.

USERS MANUAL OF THE END PRODUCT:

In the users manual of the end product, the end user has to be informed to keep at least 20cm separation with the antenna while this end product is installed and operated. The end user has to be informed that the IC radio-frequency exposure guidelines for an uncontrolled environment can be satisfied. The end user has to also be informed that any changes or modifications not expressly approved by the manufacturer could void the user's authority to operate this equipment. If the device is small or for such use that it is not practicable to place the statement on the product, then following IC statement is required to be available in the users manual: IC statement is required to be available in the users manual: This device complies with Industry Canada license-exempt RSS standard(s). This Class B digital apparatus complies with Canadian ICES-003. Operation is subject to the following two conditions: (1) this device may not cause harmful interference and (2) this device must accept any interference received, including interference that may cause undesired operation.

LABEL OF THE END PRODUCT:

The final end product must be labeled in a visible area with the following
" Contains IC :   11657A-F1DQ3021   "

Transmit Antenna Notice

This radio transmitter [IC: 11657A-F1DQ3021] has been approved by Innovation, Science and Economic Development Canada to operate with the antenna types listed below, with the maximum permissible gain indicated. Antenna types not included in this list that have a gain greater than the maximum gain indicated for any type listed are strictly prohibited for use with this device.

Antenna list (type, maximum gain(dBi))

Model	Type	Maximum gain (dBi)
F1-FR4-ANT : F1304R	SMD	2.1