Wireless LAN Access Point(RFMD)

Operational Description

Version 1.0
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1. Introduction:

Basically speaking, the schematics could be separate in two parts:
Analog Part: Including RF3000, RF2494, RF2948B, Si4126,AR0213B
Digital Part: Including RF3000, AT76C510 ,IDT71V424, AT29LV040, MX824R, ATF1504ASV

This document contains circuit operation theory for Wirless LAN Access Point.
The Procomp Wireless LAN Access Point is a flexible data communications facility implemented as an extension to, or as an altemative for, a wired LAN. Using radio frequency(RF) connections. Thus, wireless LANs combine data commectivity with user mobility. Figure 1. shows a simplified block diagram of the Wireless LAN Access Point.

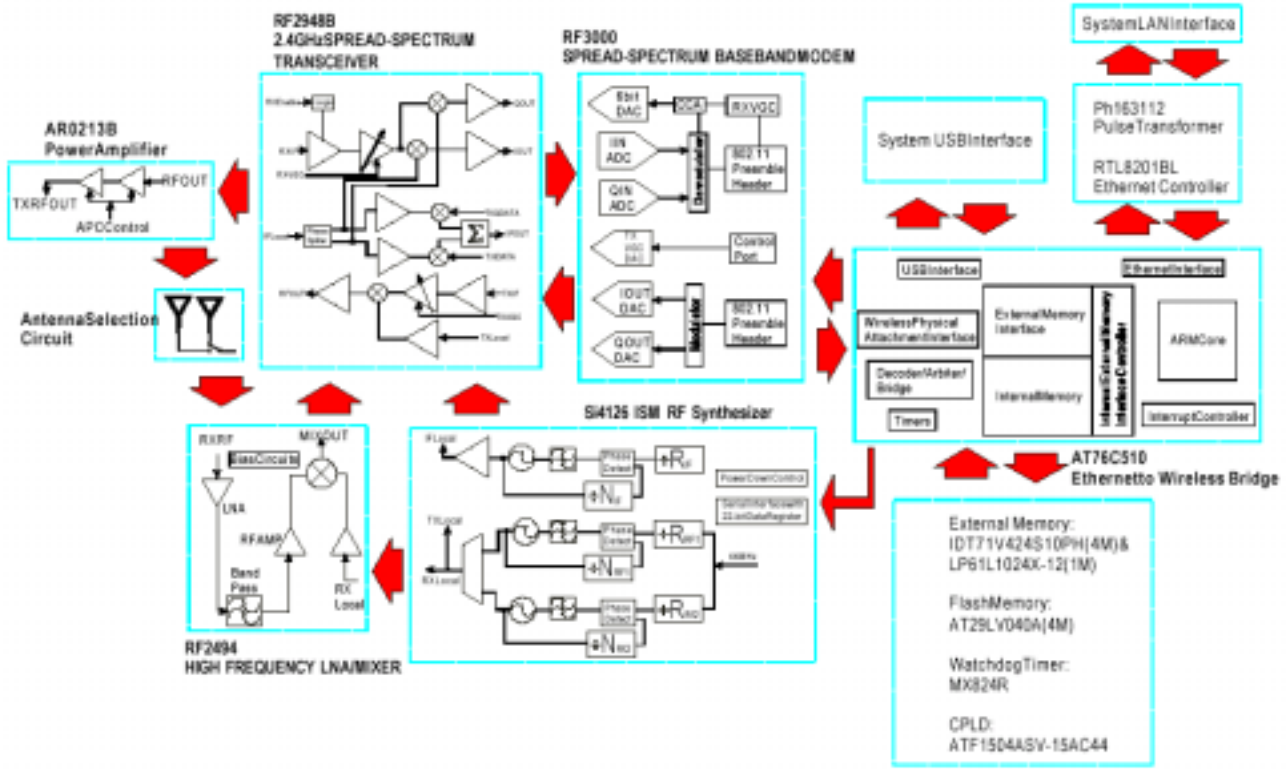

Figure 1. Wireless LAN Access Point Block Diagram

2. About AT76C510

2.1 General Description

A block diagram that is based on the AT76C510 (Bridge-on-a-Chip) performs the inter-networking between Ethernet and IEEE802.11b Wireless LAN is shown in Figure 2. The three more modules for allowing compact system implementation, flexibility for supporting almost all possible physical interfaces and thus reducing the system cost are the Ethernet PHY, the Wireless PHY and the RAM modules.

AT76C510 receives data from both networks, stores them locally for further processing, installs and maintains connections and transmits the packets to the proper destination. In order to implement such a device, a high processing power CPU is required along with the two network interfaces. At the WLAN side, AT76C510 the two different physical layers (PHYs) described at the IEEE802.11b standard, namely the Direct Sequence (DS) and Frequency Hopping (FH, at 2 Mbps) PHYs.

At the Ethernet side, a standard MII interface port is integrated into the chip along with the main bridge functions. This port is independent from the actual physical layer and allows the use of ready-made, well proven design modules for various 802.3 physical interfaces. Expansion of the wireless network area coverage is possible by means of the so called (according to the 802.11b standard) Access Points (AP). Multiple APs link the WLAN to the Ethernet and allow users to efficiently share network resources. The APs not only provide communication with the Ethernet network but also mediate wireless network traffic in their immediate neighborhood.

Multiple access points/bridges can provide wireless coverage for an entire building or campus. Bridge functions and management is a challenging task due to the non-deterministic behavior of the traffic generally used in Multimedia data communications with the mix of isochronous services.

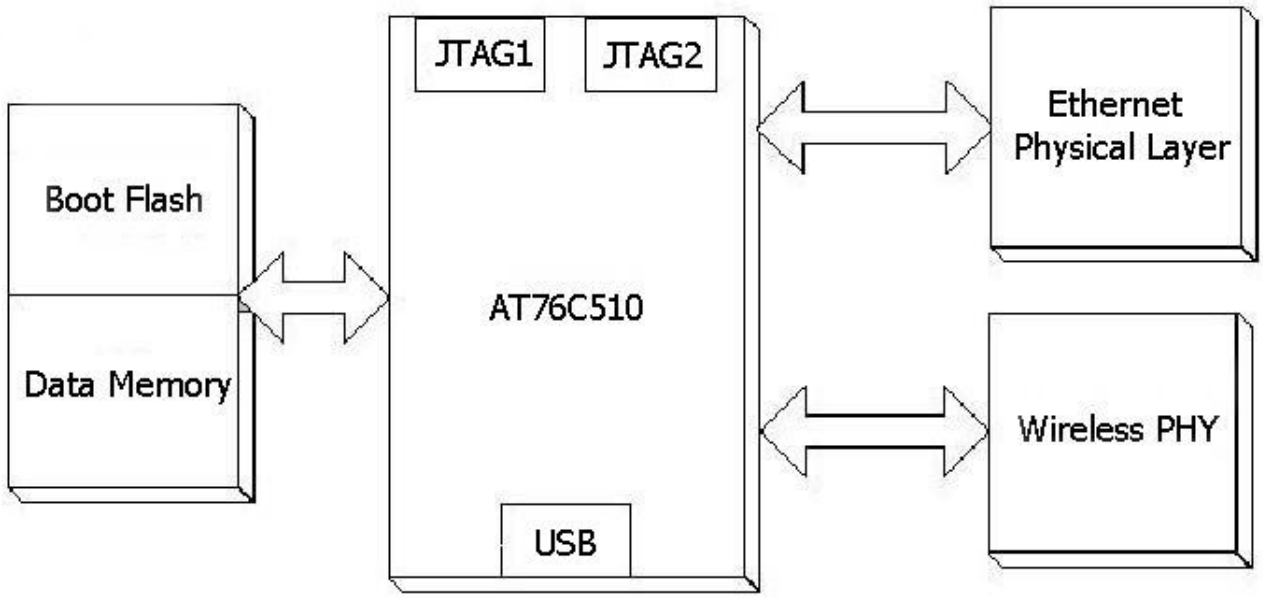

Figure 2. Typical Bridge-on-a-Chip System

2.2 Bridge Internal Data Flow

This section presents the data flow inside the chip and describes how the various modules are used for supporting it. Figure 3 shows a detailed description of the data flow at the Ethernet to WLAN direction, while Figure 4 shows the data flow at the WLAN to Ethernet direction.

When a packet is received at the Ethernet side, the following steps are executed:

1. The EMU processes the network data.
2. The EMU stores the network data in the local Rx FIFO.
3. The IWARM processor reads MAC information stored in EMU.
4. The IWARM processor programs the EMU DMA machine in order to transfer the packet in the appropriate Rx data buffer.
5. The IWARM constructs the buffer descriptors in memory and reads status information from Rx status FIFO.
6. The IWARM performs the appropriate bridging functions.
7. The IWARM informs the WLAN MAC unit for packet transmission and passes a pointer to the Tx buffer descriptors.

8. The WLAN MAC unit reads the Tx buffer descriptors.
9. The WLAN MAC unit constructs the MAC headers and performs all the necessary IEEE 802.11b functions.
10. The WLAN MAC programs the DMA machine of the 802.11b MAC Support Unit (MSU).
11. The MSU reads the data and temporarily stores it in internal FIFO for transmission.

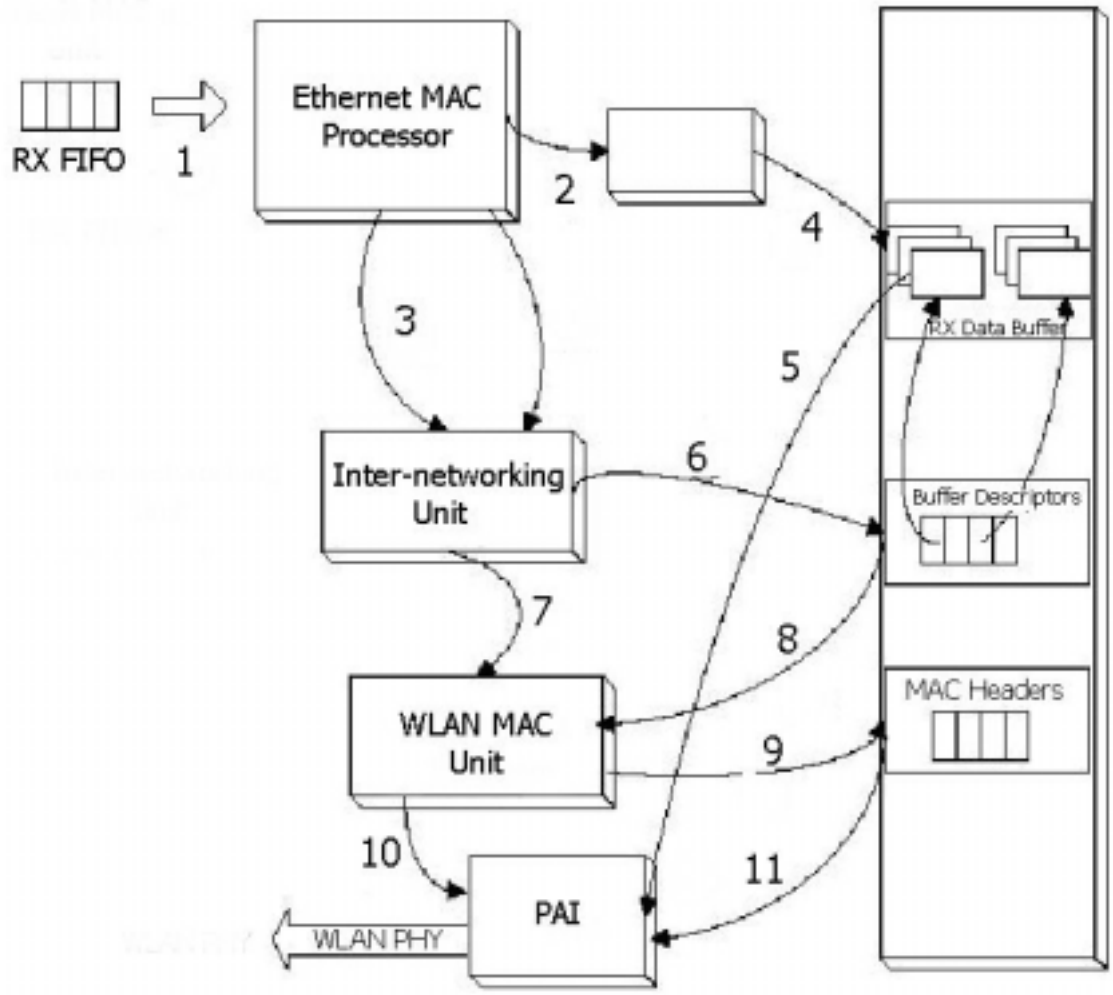

Figure 3. Ethernet Receive – WLAN Transmit Data Flow

When a packet is received at the WLAN side, the following steps are executed:The packet is stored in the internal FIFO of MSU.

1. The packet is stored in the internalFIFO or MSU.
2. The MSU informs the WLAN MAC unit for packet reception and for any other packet information (header type, CRC correct,..).
3. The WLAN MAC unit programs the MSU to perform DMA transfers to appropriate buffers in common memory and constructs buffer descriptors, which also reside in the common

memory.

4. The WLAN MAC performs the appropriate MAC functions such as error correction, reassembly, packet filtering, etc.
5. The WLAN MAC informs the inter-networking unit for the completion of the reception of the packet.
6. The inter-networking unit reads the Rx buffer descriptors and performs the appropriate bridging functions.
7. The inter-networking unit programs the EMU DMA machine to transfer the data in the Tx FIFO for Ethernet transmission.
8. The inter-networking unit informs the Ethernet MAC Unit that the transmission can start.
9. The EMU reads the data from Tx FIFO.
10. The EMU passes the data to the Ethernet Physical Device.

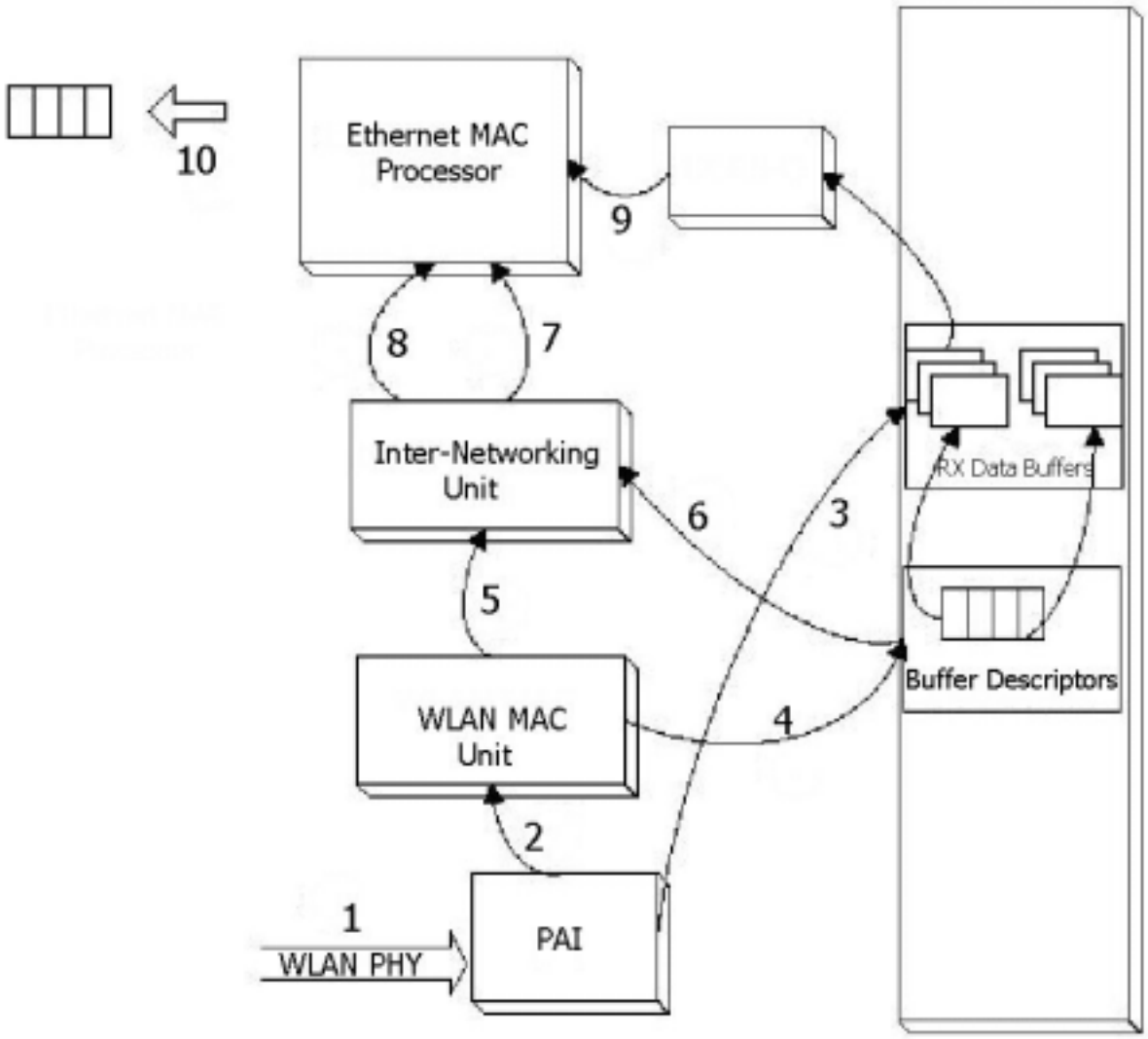

Figure 4. WLAN Receive – Ethernet Transmit Data Flow

3. About RF3000

3.1 General Description

The RF3000 is a complete spread-spectrum transceiver, allowing PSK system operation, and performs all of the functions necessary to modulate a digital data source for transmission in a wireless environment.

The architecture of the RF3000 allows the user to easily reconfigure parameters such as modulation type, and processing gain with PN codes up to 64 bits in length. When operating in IEEE802.11 modes, the RF3000: handles preamble and header generation and extraction; automatic gain control; clear channel assessment; antenna diversity; and, implements an equalizer to handle multi-path events at high data rates.Figure 5 shows a simplified block diagram of the RF3000.

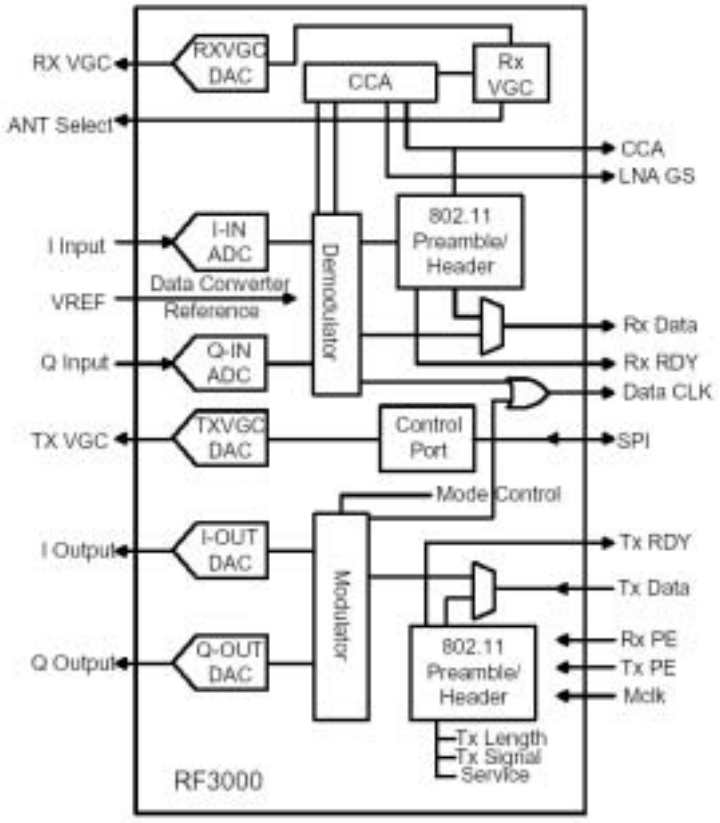

Figure 5. RF3000 Block Diagram

3.2 SPI Control Port

The control port is used by the Media Access Controller (MAC) to set up and modify the multiple operation modes of the RF3000. The port is set to SPI mode, with the RF3000 acting as Slave. Note that if no setup information is programmed into the RF3000's registers, it will default to a BPSK 1Mbps IEEE802.11 DSSS mode. If an IEEE802.11 mode is selected in Register 1, other waveform registers are ignored and the appropriate, standards compliant features are enabled (e.g., PN code, preamble/header, etc.). TX length is required for all IEEE802.11 modes.

All Registers, as defined in the Register Definition section of this datasheet, can be read in real time through this control port. Selected registers, as indicated in the Register section are read-only.

The control port of the RF3000 contains a mode to automatically increment the register pointer, allowing reading or writing of adjacent bytes without the need to stop and restart control port access.

3.3 RF3000 Method of Operation

The transmitter power enable (TX PE) input enables the transmitter process. (Note: Transmit has priority over receive.) When TX PE is high, the LNA GS signal will be driven low. The TX RDY output indicates the readiness of the RF3000 to receive data for transmit. Transmitted data is passed into the RF3000 through the TXDATA input and clocked by the DATA CLK output. The receiver power enable (RX PE) input enables the receiver, and the receive data ready (RX RDY) signal indicates that received data is upcoming. The RF3000 generates the received data clocks, and outputs the received data, through the RX DATA output. The receiver port also provides a clear channel assessment (CCA) to the MAC.

3.4 IEEE802.11 Transmit Modes

(IEEE802.11 DSSS Transmit Modes)
The RF3000 supports PSK and CCK DSSS modes defined in IEEE802.11b specification. The RF3000 also supports the optional short preamble and header format as defined in

IEEE802.11b.

The user must first prepare the applicable control port registers to determine the mode of operation and the transmission length. The mode of operation must be written into Register 1, followed by setting the transmission length (in microseconds). The length is to be written into Registers 17 (bit 0 only), 18 and 19. Mode byte values for IEEE802.11 modes are summarized below.

IEEE802.11 DSSS Mode	Mode Byte Value
1Mbps DBPSK	0x0016
1Mbps DBPSK	0x0216
2Mbps DQPSK Short preamble	0x0316
5.5Mbps CCK Long preamble	0x0416
5.5Mbps CCK Short preamble	0x0516
11Mbps CCK Long preamble	0x0616
11Mbps CCK Short preamble	0x0716

3.5 Diversity

The RF3000 makes diversity decisions every 1mS while looking for A/D saturation according to the state machine in Figure 6.

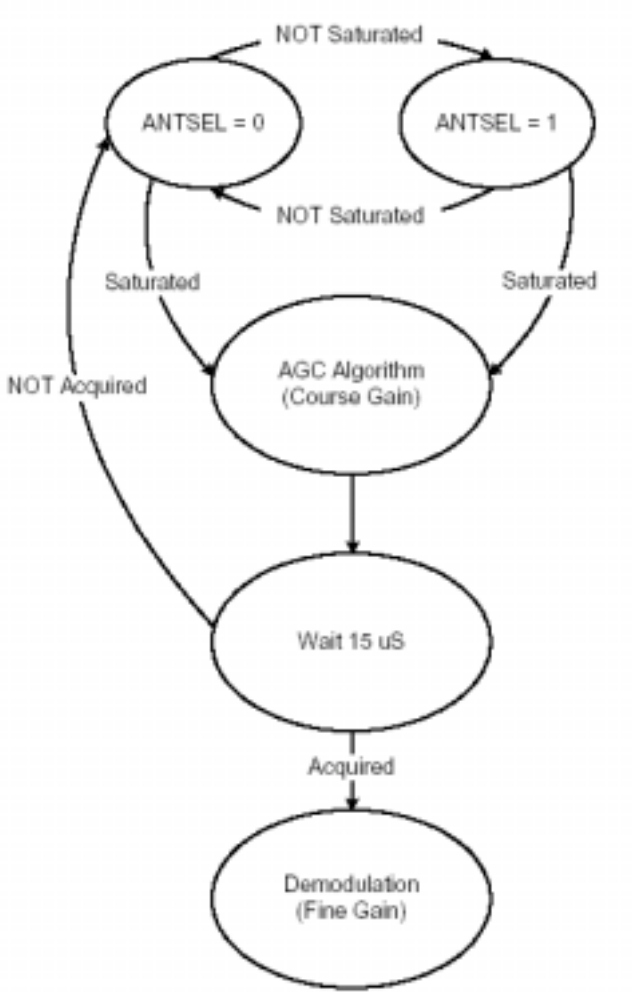

Figure 6. Diversity and AGC Algorithm

3.6 AGC Algorithm

The RF3000 AGC algorithm is implemented to automatically control both the RXVGC of the RF2948 and the LNAGS pin of the RF2494. The RF3000 is programmed to search the possible gain settings of LNAGS and RXVGC in a binary fashion to quickly determine the final gain setting needed to optimize the inputs to the A/D converters for demodulation. The AGC algorithm is completely controlled by detection of saturation of the A/D converters.

4. About RF2494

4.1 General Description

The RF2494 contains the LNA/Mixer for this chipset. The LNA is made from two stages including a common emitter amplifier stage with a power gain of 13dB and an attenuator which has an insertion loss of 3dB in high gain mode, and 17dB in low gain mode. The attenuator was put after the LNA so that system noise figure degradation would be minimized. A single gain stage was used prior to the image filter to maximize IP3 which minimizes the risk of large out-of-bad signals jamming the desired signal. Figure 7. shows a simplified block diagram of the RF2494.

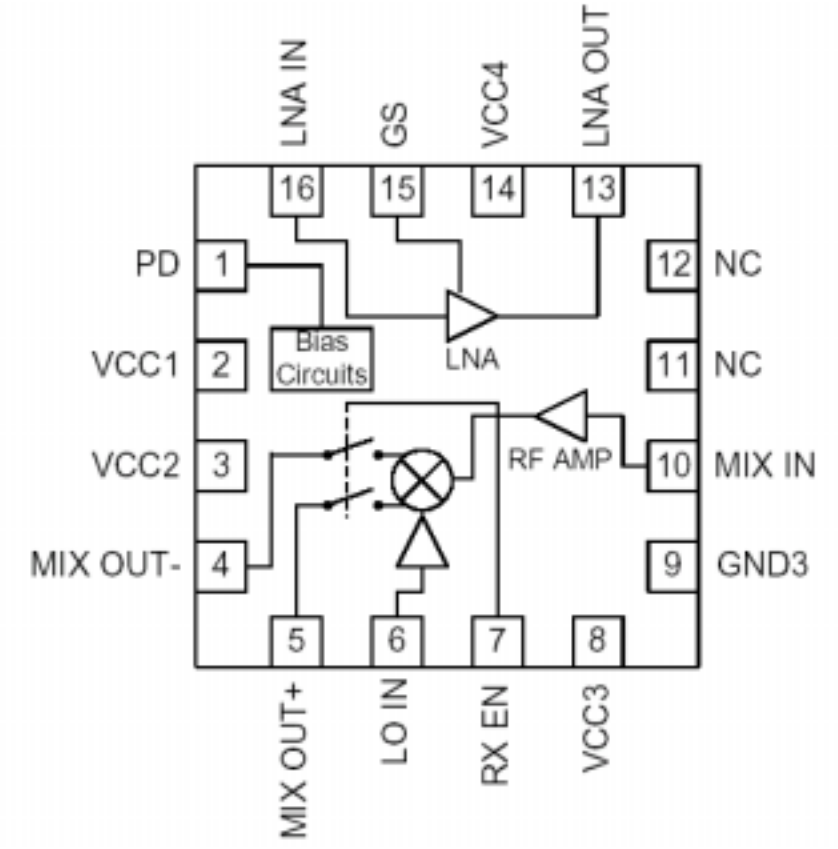

Figure 7. RF2494 Functional Block Diagram

The mixer on the RF2494 is also two stages. The first stage is a common emitter amp used to boost the total power gain prior to the lossy SAW filter, to convert to a differential signal to the input of the mixer, and to improve the noise figure of the mixer. The second stage is a double balanced mixer whose output is differential open collector. It is recommended that a "current combiner" is used (as shown in figure 8) at the mixer output to maximize conversion gain, but other loads can also be used. The current combiner is used to do a differential to single ended conversion for the SAW filter. C1, C2 and L1 are used to tune the circuit for a specific IF frequency. L2 is a choke to supply DC current to the mixer that is also used as a tuning element, along with C3, to match to the SAW filter's input impedance. RL is the SAW filter's input impedance. The cascaded voltage gain of the LNA/Mixer is 35dB, which after insertion loss in the image filter (~2dB) and IF SAW filter (~10dB), still gives 23dB of gain prior to the IF amps. Because of this, the noise figure of the IF amps should not significantly degrade system noise figure.

The LNA input should be matched for a good return loss for optimum gain and noise figure. To allow the designer to match each of these ports, 2-port s-parameter data is available for the LNA, and 1-port data is available for MIXER IN and LO IN. Care must be taken in using this data, as board layout profoundly effects these impedances. It is recommended that designers

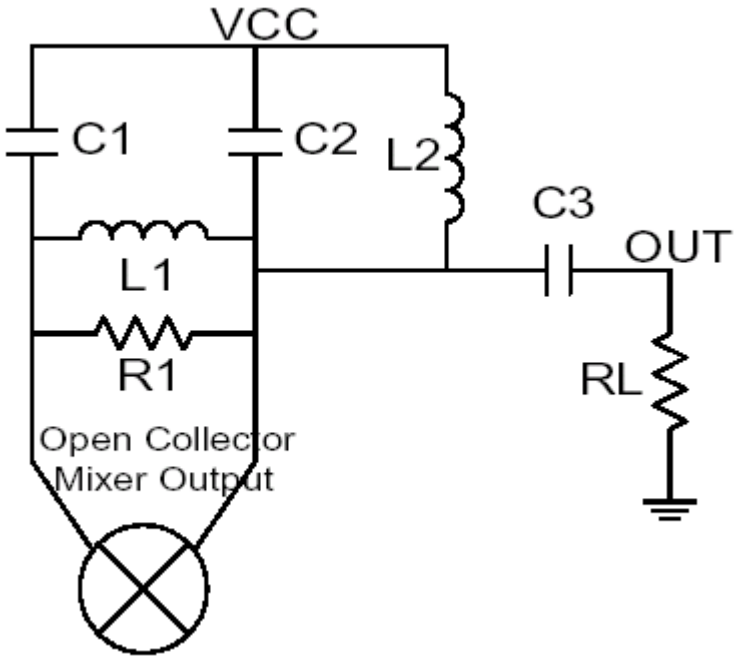

Figure 8. Current Combiner for Mixer Load

5. About RF2948B

Figure 9. shows a simplified block diagram of the RF2948B.

5.1 RECEIVER

RX IF AGC/Mixer

Being essentially high impedance, RX IF IN responds to the input voltage (rather than power), and amplifies that voltage by the gain specified in the datasheet, then presents the output voltage at a high impedance (after downconversion). For characterization purposes, a 50. shunt resistor is placed on the IF signal path, before AC-coupling to the input. A 50. signal source is applied directly across the shunt resistor, through a coaxial test lead. The signal source sees the shunt resistor and therefore a low SWR. Voltage gain is then simply the ratio of the output voltage to the input voltage.

The front end of the IF AGC starts with a single-ended input and a constant gain amp of 15dB. This first amp stage sets the noise figure and input impedance of the IF section, and its output is taken differentially. The rest of the signal path is differential until the final baseband output, which is converted back to single-ended. Following the front end amp are multiple stages of variable gain differential amplifiers, giving the IF signal path a gain range of 4.0dB to 70.0dB. The noise figure (in max gain mode) of the IF amplifiers is 5dB, which should not degrade the system noise figure.

The IF to BB mixers are double-balanced, differential in, differential out, mixers with negligible conversion gain. The LO for each of these mixers is shifted 90° so that the I and Q signals are separated in the mixers.

RX Baseband Amps, Filters, and DC Feedback

At baseband frequency, there are fully integrated gm-C low pass filters to further filter out-of-band signals and spurs that get through the SAW filter, anti-alias the signal prior to the A/D converter, and to band-limit the signal and noise to achieve optimal signal-to-noise ratio.

The 3dB cut-off frequency of these low pass filters is programmable with a single external resistor, and continuously variable from 1MHz to 35MHz. A five-pole Bessel type filter

response was chosen because it is optimal for data systems due to its flat delay response and clean step response. Butterworth and Chebychev type filters ring when given a step input making them less ideal for data systems. The filter outputs drive the
linear 700mVPP signal off-chip.
DC feedback is built into the baseband amplifier section to correct for input offsets. Large DC offsets can arise when a mixer LO leaks to the mixer input and then mixes with itself. DC offsets can also result from random transistor mismatches. A large external capacitor is needed for the DC feedback to set the high pass cutoff.

5.2 LO INPUT BUFFERS

RF LO Buffer

The RF LO input has a limiting amplifier before the mixer on both the RF2494 (RX) and RF2948B (TX).

This limiting amplifier design and layout is identical on both ICs, which will make the input impedance the same as well. Having this amplifier between the VCO and mixer minimizes any reverse effect the mixer has on the VCO, expands the range of acceptable LO input levels, and holds the LO input impedance constant when switching between RX and TX. The LO input power range is -18dBm to +5dBm, which should make it easy to interface to any VCO and frequency synthesizer.

IF LO Buffer

The IF LO input has a limiting amplifier before the phase splitting network to amplify the signal and help isolate the VCO from the IC. Also, the LO input signal must be twice the desired intermediate frequency. This simplifies the quadrature network and helps reduce the LO leakage onto the RX_IF input pin (since the LO input is now at a different frequency than the IF). The amplitude of this input needs to be between -15dBm and 0dBm. Excessive IF LO harmonic content affects phase balance of the modulator and demodulator so it is recommended that IF LO harmonics be kept below -30dBc.

5.3 TRANSMITTER

TX LPF and Mixers

The transmit section starts with a pair of 5-pole Bessel filters identical to the filters in the receive section and with the same 3dB frequency. These filters pre-shape and band-limit the digital or analog input signals prior to the first upconversion to IF. These filters have a high input impedance and expect an input signal of 100mVPP typical. Following these low pass filters are the I/Q quadrature upconverter mixers. Each of these mixers is half the size and half the current of the RF to IF downconverter on the RF2494. Recall that this upconverted signal may drive the same SAW filter (in half-duplex mode) as the RF2494 and therefore share the same load. Having the sum of the two BB to IF mixers equal in size and DC current to the RF to IF mixer, will minimize the time required to switch between RX and TX, and will facilitate the best impedance match to the filter.

TX VGA

Being essentially high impedance, TX IF IN responds to the input voltage (rather than power), and amplifies that voltage by the gain specified in the datasheet, then presents the output voltage at a 50. impedance (after upconversion). For characterization purposes, a 50. shunt resistor is placed on the IF signal path, before AC-coupling to the input. A 50. signal source is applied directly across the shunt resistor, through a coaxial test lead. The signal source sees the shunt resistor and therefore a low SWR. Voltage gain is then the same as power gain, simply the difference in dB between the output power and the input power.

The AGC after the SAW filter starts with a switch and a constant gain amplifier of 15dB, which is identical to the circuitry on the receive IF AGC. This was done so that the input impedance will remain constant for different gain control voltages. Following this 15dB gain amplifier is a single stage of gain control offering 15dB gain range. The main purpose of adding this variable gain is to give the system the flexibility to use different SAW filters and image filters with different insertion loss values. This gain could also be adjusted real time, if desired.

TX Upconverter

The IF to RF upconverter is a double-balanced differential mixer with a differential to

single-ended converter on the output to supply 0dBm peak linear power to the image filter. The upconverted SSB signal should have -6dBm power at this point, and the image will have the same power, but due to the correlated nature of the signal and image, the output must support 0dBm of linear power to maintain linearly.

+6dBm PA Driver

The SSB output of the upconverter is -6dBm of linear power. The image filter should have at most 4dB of insertion loss while removing the image, LO, 2LO and any other spurs. The filter output should supply the PA driver input -10dBm of power.

The PA driver is a one-stage class A amplifier with 10dB gain and capable of delivering 6dBm of linear power to a 50. load, and has a 1dB compression point of 12dBm. For lower power applications, this PA driver can be used to drive a 50. antenna directly.

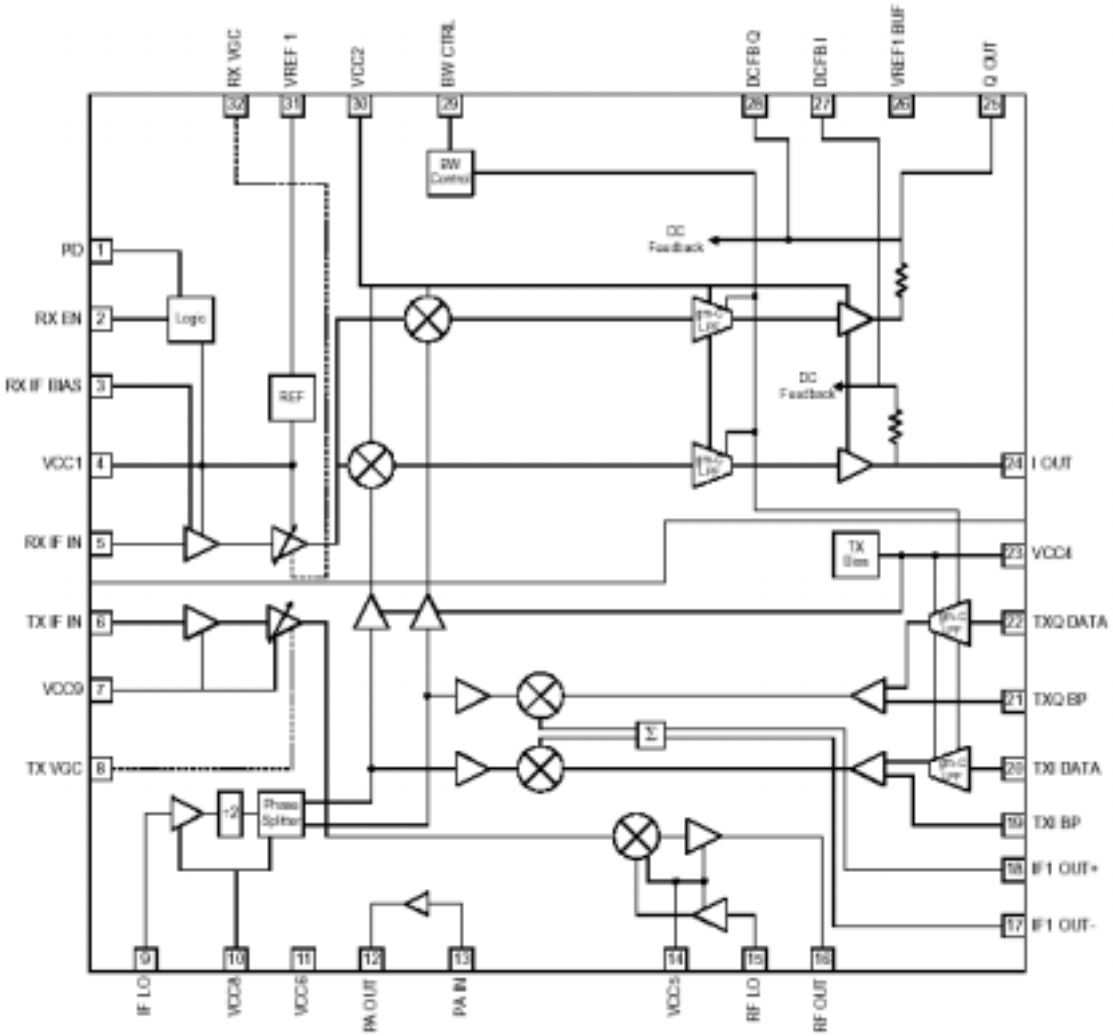

Figure 9. RF2948B Block Diagram

6. About Si4126

6.1 Functional Description

The Si4126 is a monolithic integrated circuit that performs IF and dual-band RF synthesis for many wireless communications applications. This integrated circuit (IC), along with a minimum number of external components, is all that is necessary to implement the frequency synthesis function in applications like W-LAN using the IEEE 802.11 standard.
The Si4126 has three complete phase-locked loops (PLLs), with integrated voltage-controlled oscillators (VCOs). The low phase noise of the VCOs makes the Si4126 suitable for use in demanding wireless communications applications. Also integrated are phase detectors, loop filters, and reference and output frequency dividers. The IC is programmed through a three-wire serial interface.

Two PLLs are provided for RF synthesis. These RF PLLs are multiplexed so that only one PLL is active at a given time (as determined by the setting of an internal register). The active PLL is the last one written. The center frequency of the VCO in each PLL is set by the internal bond wire inductance within the package.

Inaccuracies in these inductances are compensated for by the self-tuning algorithm. The algorithm is run following power-up or following a change in the programmed output frequency. The RF PLLs contain a divide-by-2 circuit before the Ndivider.

As a result, the phase detector frequency is equal to half the desired channel spacing. For example, for a 200 kHz channel spacing ,would equal 100 kHz.The IF PLL does not contain the divide-by-2 circuit before the N-divider. In this case, f is equal to the desired channel spacing. Each RF VCO is optimized for a particular frequency range. The RF1 VCO is optimized to operate from 2.3 GHz to 2.5 GHz, while the RF2 VCO is optimized to operate between 2.025 GHz and 2.3 GHz.

One PLL is provided for IF synthesis. The center frequency of this circuit's VCO is set by an external inductance. The PLL can adjust the IF output frequency by ±5% of the VCO center frequency. Inaccuracies in the value of the external inductance are compensated for by the Si4126's proprietary self-tuning algorithm.
This algorithm is initiated each time the PLL is poweredup (by either the PWDN pin or by software) and/or each time a new output frequency is programmed. The IF VCO can have its center frequency set as low as 526 MHz and as high as 952 MHz. An IF output divider is

provided to divide down the IF output frequencies, if needed. The divider is programmable, capable of dividing by 1, 2, 4, or 8. In order to accommodate designs running at XIN frequencies greater than 25 MHz, the Si4126 includes a programmable divide-by-2 option (XINDIV2 in Register 0, D6) on the XIN input. By enabling this option, the Si4126 can accept a range of TCXO frequencies from 25 MHz to 50 MHz. This feature makes the Si4126 ideal for W-LAN radio designs operating at an XIN of 44 MHz.

The unique PLL architecture used in the Si4126 produces settling (lock) times that are comparable in speed to fractional-N architectures without suffering the high phase noise or spurious modulation effects often associated with those designs. Figure 10 shows a simplified block diagram of the Si4126.

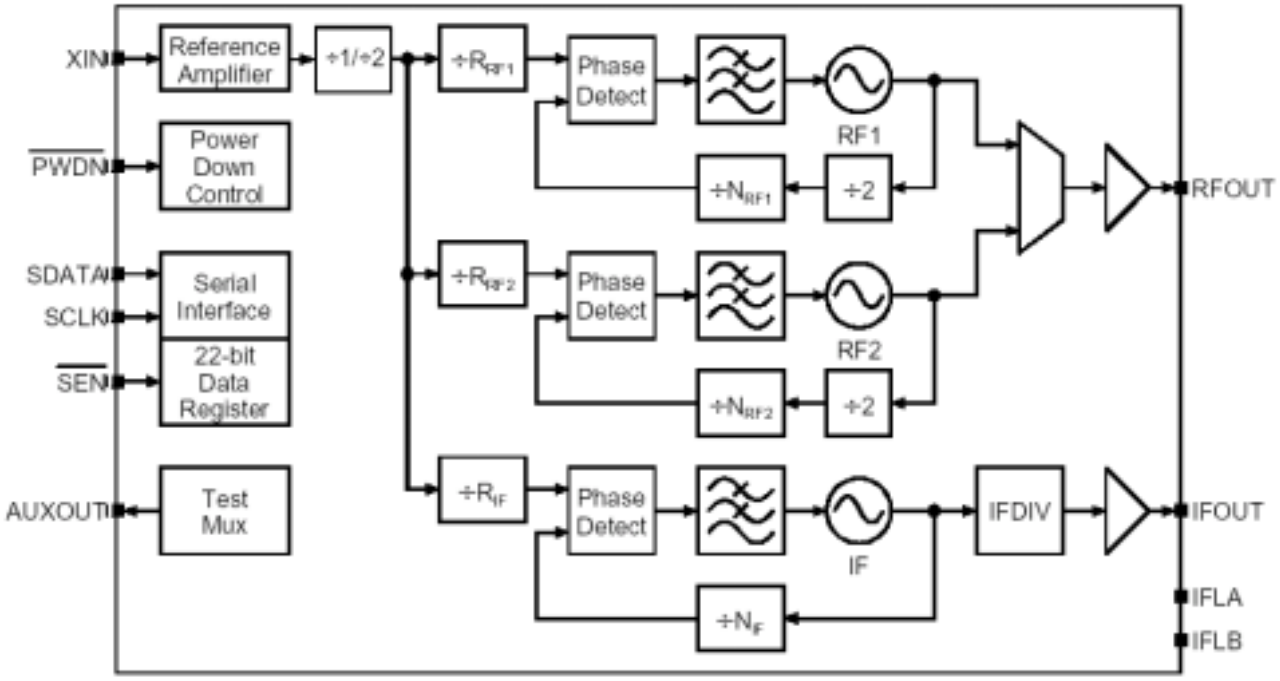

Figure 10. Si4126 Block Diagram

6.2 Serial Interface

The Si4126 is programmed serially with 22-bit words comprised of 18-bit data fields and 4-bit address fields. When the serial interface is enabled (i.e., when SEN is low) data and address bits on the SDATA pin are clocked into an internal shift register on the rising edge of SCLK. Data in the shift register is then transferred on the rising edge of SEN into the internal data register addressed in the address field. The serial interface is disabled when SEN is

high.

6.3 Setting the IF VCO Center Frequencies

The IF PLL can adjust its output frequency ±5% from the center frequency as established by the value of an external inductance connected to the VCO. The RF1 and RF2 PLLs have fixed operating ranges due to the inductance set by the internal bond wires. Each center frequency is established by the value of the total inductance (internal and/or external) connected to the respective VCO. Manufacturing tolerance of ±10% for the external inductor is acceptable for the IF VCO. The Si4126 will compensate for inaccuracies by executing a self-tuning algorithm following PLL power-up or following a change in the programmed output frequency.

6.4 Self-Tuning Algorithm

The self-tuning algorithm is initiated immediately following power-up of a PLL or, if the PLL is already powered, following a change in its programmed output frequency. This algorithm attempts to tune the VCO so that its free-running frequency is near the desired output frequency. In so doing, the algorithm will compensate for manufacturing tolerance errors in the value of the external inductance connected to the IF VCO. It will also reduce the frequency error for which the PLL must correct to get the precise desired output frequency. The self-tuning algorithm will leave the VCO oscillating at a frequency in error by somewhat less than 1% of the desired output frequency.

6.5 RF and IF Outputs (RFOUT and IFOUT)

The RFOUT and IFOUT pins are driven by amplifiers that buffer the RF VCOs and IF VCO, respectively. The RF output amplifier receives its input from either the RF1 or RF2 VCO, depending upon which R- or Ndivider register was last written. For example, programming the N-Divider register for RF1 automatically selects the RF1 VCO output.

Figure 11. shows an application diagram for the Si4126. The RF output signal must be AC coupled to its load through a capacitor.

The IFOUT pin must also be AC coupled to its load through a capacitor. The IF output level

is dependent upon the load. For resistive loads greater than 500 . the output level saturates and the bias currents in the IF output amplifier are higher than they need to be.

The LPWR bit in the Main Configuration register (Register 0) can be set to 1 to reduce the bias currents and therefore reduce the power dissipated by the IF amplifier. For loads less than 500 ., LPWR should be set to 0 to maximize the output level.

For IF frequencies greater than 500 MHz, a matching network is required in order to drive a 50 . load. See Figure 11 below. Typical values range between 8 nH and 40 nH.

For frequencies less than 500 MHz, the IF output buffer can directly drive a 200 . resistive load or higher. For resistive loads greater than 500 . (f < 500 MHz) the LPWR bit can be set to reduce the power consumed by the IF output buffer. See Figure 12 below.

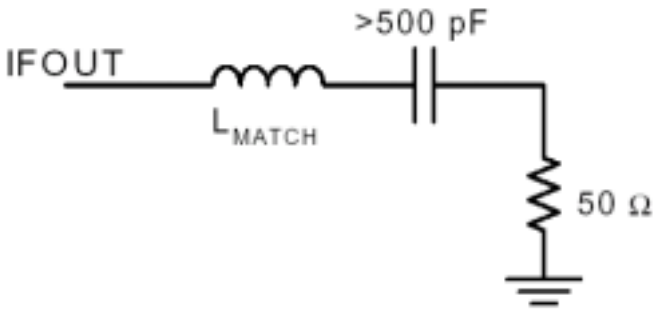

Figure 11. IF Frequencies > 500 MHz

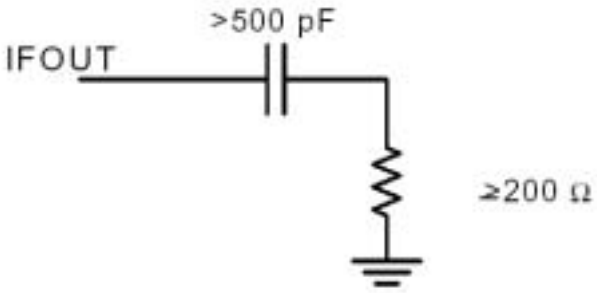

Figure 12. IF Frequencies < 500 MHz

6.6 Reference Frequency Amplifier

The Si4126 provides a reference frequency amplifier. If the driving signal has CMOS levels, it can be connected directly to the XIN pin. Otherwise, the reference frequency signal should be AC coupled to the XIN pin through a 560 pF capacitor.

6.7 Powerdown Modes

The Si4126 can be powered down by taking the PWDN pin low or by setting bits in the Powerdown register (Register 2). When the PWDN pin is low, the Si4126 will be powered down regardless of the Powerdown register settings. When the PWDN pin is high, power management is under control of the Powerdown register bits.
The IF and RF sections of the Si4126 circuitry can be individually powered down by setting

the Powerdown register bits PDIB and PDRB low. The reference frequency amplifier will also be powered up if either the PDRB and PDIB bits are high. Also, setting the AUTOPDB bit to 1 in the Main Configuration register (Register 0) is equivalent to setting both bits in the Powerdown register to 1.

The serial interface remains available and can be written in all power-down modes.

7. About AR0213B

General Description

The AR0213B manufactured on Gallium Arsenide Heterojunction Bipolar Transistor (GaAs HBT) process is a high power, high efficiency amplifier IC designed for wireless data application between 902MHz to 928MHz ISM band and 2.4GHz to 2.5GHz ISM band. The device is packaged in a compact 4mmx4mm QFN-16L. The device features analog gain control to optimize transmit power while maximizing battery life in portable equipment requiring up to 250mW transmit power at the antenna port. Figure 13 shows a simplified block diagram of the Power Amplifier AR0213B.

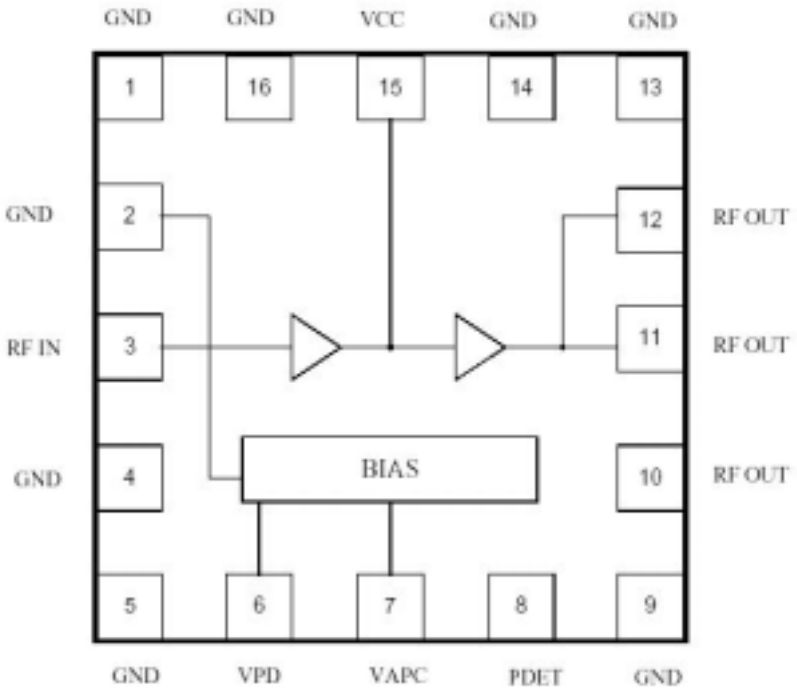

Figure 13. AR0213B Block Diagram