VG300
Theory of operation 1.0
November 14,1999

US Wireless Products Division

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1.0 Purpose

The purpose of this document is to provide a detailed description of the circuitry that makes up Z SQUARE'S product

2.0 Introduction

Exhibit A presents the block diagram of Z SQUARE'S radio.

The radio transceiver provides full-duplex operation with a transmitter architecture employing vector modulation of an offset loop oscillator and a receiver utilizing a dual-conversion, heterodyne architecture. The radio is designed to meet the CDPD specifications and comply with FCC regulations. The radio is controlled by the Ruby II. Communication Processor. It also passes signals to and from the Topaz radio interface IC, and transmits and receives radio signals between the MDBS over the airlink interface.

The Z SQUARE'S Radio provides vector controlled modulation. The radio interface has a radio On/Off Control which is controlled by the Topaz CDPD Radio Interface Chip Port registers. It will control the power to the receiver chain and transmitter chain independently. The radio TX Power is controlled by the Topaz CDPD Radio Interface Chip TX Power D/A. The Ruby II Serial Controller is used to control the radio channel select synthesizers with configuration and synthesizer commands.

3.0 Radio Interface Specification

3.1 Common Interface

AGND(Pin 1) Analog power supply ground returns for the radio.

CLOCK(Pin 6) Synthesizer, serial clock input. This signal requires 5 volt, CMOS compatible levels and is pulled to ground through a 100K ohm resistor. Have attached data sheets.

ENABLE(Pin 5) Synthesizer, data load enable input. This signal requires 5 volt, CMOS compatible levels and is pulled to ground through a 100k ohm resistor. Timing is provided in Figure 5-1 below.

DATA(Pin 7) Synthesizer, serial data input. This signal requires 5volt, CMOS compatible levels and is pulled to ground through a 100K ohm resistor. Timing is provided in Figure 5-1 below.

Note Clock, data and enable timing and control values are compatible with the philips LMA 1015A.

3.2 Receiver Interface

RXDIS(Pin 3) Receiver power supply enable. A low voltage(Vss+0.5 volts max.)applied to this pin powers up the receiver including both receive and transmit synthesizers and VCOs. A high voltage (Vdd-0.5 volts min.) powers down the receiver This signal is pulled up to Vdd through a 10Kohm resistor.

RXPOS(Pin 12) Analog receive data output. This pin is the non-inverting output of the discriminator

detector. This pin has a nominal DC potential of 2.5 volts $\pm$ 1.0 volt and a typical peak-to-peak signal swing of 0.5 volts. The load impedance connected to this pin should be at least 200K ohms.

RXNEG(Pin 13) Analog receive data output. This pin provides one of two functions depending on the configuration of the discriminator output. In the configuration this pin has a nominal DC potential of 2.5 volts $\pm$1.0 volt and a typical peak-to-peak signal swing of 0.5 volts. In this configuration the discriminator output is differential and the OFFDAC input on Pin 2 can be varied to adjust the discriminator offset. Otherwise is used to loop back the comparator voltage to run in a single ended discriminator output configuration. The load impedance connected to this pin should be at least 200K ohms.

RSSI(Pin 4) Receive signal strength indicator. This pin provides an analog voltage indicative of the received signal strength in dB. The signal level on this output has a range from 0.0 to 5.0 volts. The load impedance connected to this pin should be at least 200K ohms. The RSSI response curve is embedded within its corresponding baseband board.

OFFDAC(Pin 2) Offset DAC. This pin will provide one of two functions. One is an input that is used

to adjust the offset between the differential discriminator outputs. The voltage in this case can be varied between 0 and 5 volts. Another is a signal path for the comparator input level that coincides with the discriminator output level of RXPOS.

3.3 Transmitter interface

TXDIS(Pin 8) Transmitter power supply enable. A low voltage (Vss+0.5 volts max.) applied to this pin powers up the transmitter including the I/Q modulator, up-converter and power amplifier. A high voltage (Vdd-0.5 volts min .)powers down the transmitter. This signal is pulled up Vdd through a 10K ohm resistor.

QPOS(Pin 14) Q channel ,non-inverted modulator input. This pin is the non-inverting. Quadrature-phase input to the vector modulator. Its DC level should be 2.5 volts and the peak-to peak signal swing should be 2.5 volts.

ONEG(Pin 15) Q channel, inverted modulator input. This pin is the inverting, quadrature-phase input to the vector modulator. Its DC level should be 2.5 volts and the peak-to peak- to- peak signal swing should be 2.5 volts.

INEG(Pin 11) I channel, inverted modulator input. This pin is the inverting, in-phase input to the vector modulator. Its DC level should be 2.5 volts and the peak-to-teak signal swing should be 2.5 volts.

IPOS(Pin 10) I channel, non-inverted modulator input. This pin is the non-inverting, in-phase input to the vector modulator. Its DC level should be 2.5 volts and the peak-to - peak signal swing should be 2.5 volts.

TXDAC(Pin 9) Analog ,transmit power level control input. This input controls the power level output of the transmitter's power amplifier. The impedance to ground shall be 5.11 kΩ$\pm$1% and the usable voltage range shall be between 0 and 3.3 volts. The voltage in vs power out transfer curve is embedded within its baseband board.

4.0 Radio Theory of Operation

4.1 Receiver Operation

The receiver architecture of the radio is a typical double conversion super-heterodyne receiver. The block diagram of the receiver architecture is presented in Exhibit A. It is also beneficial to relate the following information to the schematic diagram presented in Exhibit A.

The power supply to the receiver chain is controlled with the RXDIX line. A low voltage(<Vss+.5V) enables the RF front end,the IF downconverter /demodulator IC, the dual PLL IC, the TCXO, both the 1st LO and 2nd LO (128.16 MHz discrete design), and the voltage regulator which maintains voltage stability to the oscillators. A high voltage(>Vdd+.5V) to the RXDIS line disables the power supply to the circuitry mentioned above.

In the receive path an antenna is connected to the duplexer which filters out the receive band between 869 and 894 MHz. The duplexer provides 50 dB isolation between the transmit and receive frequencies. The duplexer is followed by a low noise amplifier and Gilbert cell mixer IC. Between the LNA and mixer is an image reject filter.

The 1st LO ranges in frequency from 952.20-977.13 MHz in 30KHz steps and is used to drive the mixer that downconverts the received signal to a first . IF frequency of 83.16 MHz(IF1,). The input level to the mixer is at-6 dBm $\pm$ dB. This LO is generated by, phase locking a voltage controlled oscillator to a temperature compensated crystal oscillator with the dual PLL IC. This ensures the accuracy of the downconverted signal to be within $\pm$2.5 PPM (over temperature and voltage variation)of the 1st LO frequency. The inaccuracy of the second LO is insignificant since it is oscillating at a much lower frequency. The accuracy of the 1st LO is important with respect to the transmitted signal since this same LO is used to generate the transmit signal also.

Following the 83.16 MHz IF filter is a high performance monolithic low-power FM IF system incorporating a mixer/oscillator,two limiting intermediate frequency amplifiers, a quadrature detector,a logarithmic received signal strength indicator(RSSI) with fast rise and fall time, and a voltage regulator receives the 83.16 MHz signal, downconverts it to 455 KHz, amplifies it into limiting to strip off any AM components and then demodulates the remaining FM signal . The signal is taken off chip for two stages of IF filtering by two 455 KHz CERAMIC FILTERS WITH 30 KHz of bandwidth. U16 also generates the RSSI voltage.

The demodulated output can be used as either a single ended or differential signal depending on assembly procedures. In the single ended mode the demodulated signal is present on RXPOS and the OFFDAC signal is looped back on the RXNEG connector pin so that the OFFDAC signal is used as the comparator voltage for the received data. In the differential mode the received data is present on both the RXPOS and RXNEG connector pins 180^{o} out of phase. In this configuration the OFFDAC line is used to control the center frequency of the demodulator tank circuit so that voltage offsets between the differential receive signals can be eliminated.

4.2 Transmitter Operation

The transmitted signal from the radio is generated by mixing a low frequency vector modulated signal(2^{nd} LO)at 128.16 MHz with the 1^{ST} LO. The 1^{st} LO is the same one described in the receiver discussion above. The 1^{ST} LO has it's power divided in two so that 1/2 the power can be used to generate the transmitted signal. Both the 128.16 MHz signal and the 1^{ST} LO are phase locked to the TCXO(U9). A copy of the data sheet for the TCXO can be found in Exhibit A. Phase locking to the TCXO ensures that the output frequencies of the two PLL's are accurate to within $\pm$ 2.5 ppm of their respective frequencies and hence the transmitted signal is within $\pm$2.5 pm of its intended frequency over both temperature and voltage variations. The block diagram of the transmitter chain is presented in Exhibit A.

The output of the transmitter is controlled by two different methods. The TXDIS line controls power supply to the transmitter chain . A low voltage(<GND+.5V) enables the quadrature modulator(U17), the upconverter (U18), and amplifier following the upconverter(a discrete design). A high voltage(>Vdd-.5V) to the TXDIS line disables the power supply to the circuitry mentioned above. By disabling this circuitry there is no RF input to the power amplifier, therefore, there is no transmitted signal power .The TXDAC line also inhibits the transmitted output when the level is below GND+.5 volt. Ether method can be used to disable the output power of the transmitted signal, but in normal operation the TXDAC line is varied between.5 and 3.3 volts to set the output to the desired level.

The 2nd LO is a 128.16 MHz VCO that is phase locked to the 15.36 MHz TCXO. This is used to drive a quadrature modulator. The carrier input to is quadrature modulated by differential I & Q signals IPOS/INEG and QPOS/QNEG. The modulating signal is a GMSK at 19.2 KBPS$\pm$50 ppm

with BT=0.5 and H=0.5$\pm$5%. These modulation characteristics which are generated by the

Geode™ baseband solution ensure that the adjacent and alternate channel emissions spectrums will be well within the emission specifications set forth by FCC regulation. A bit value of lis represented by an instantaneous frequency which is greater than the carrier center frequency and a bit value of 0 is represented by a frequency that is less than the carrier center frequency. The peak carrier deviation as a result of this modulation is 4.8 KHz.

The output of the 128.16 MHz modulator is filtered by a 5 pole chebyshev low pass filter to eliminate harmonics before the signal reaches the upconverter. This filter substantially reduces the level of spurious signals that reach the power amplifier. The 128.16 MHz signal is then upconverted in U18 with the resulting output offset 45 MHz below the received frequency. The output of the mixer is amplified, filtered and routed to the Power amp. A data sheet for the filter is presented in Exhibit A. The filter performs two functions. It is used to filter out the 1 ST AND 2nd LOs MxN mixing products generated in the upconverter and it also filters out the phase noise of the transmitted signal that falls in the receive band. It is necessary to filler the phase noise or it will desensitize the receive signal during transmission.

The filtered signal is then amplified to 1.2 W max by a high gain/high efficiency power amplifier Three stage power amplifier. A copy supply input and typically draws 500 mA, when the TXDAC line sets the power output to maximum. When the TXDAC line is set to transmit at the lowest power level(+8dBm). the power amplifier typically draws 125 mA. The level control control circuit maintains the RF power at a specific level controlled by the TXDAC input voltage. The TXDAC signal accurately controls the output power levels that correspond to the CDPD class III output levels by controlling the gate voltages of the three stages of amplification with the power amplifier. By controlling the gate voltages of each stage the channel current carried by the electrons from the source to the drain is controlled. A higher gate voltage corresponds to higher channel current which results in higher gain.

After passing through the duplexer to the antenna, the remaining power is .6 W max. The duplexer attenuates the hamonics of the transmitted signal and it also increases the attenuation of the transmitted signals phase noise in the receive band.