FCC ID: LU9600746

Technical Description :

The brief circuit description is listed as follows :
- L8, L9, VC1, VC2, C24, C25 and associated circuit act as Loop Antennas.
- U2, Q1, Q5, Q9 and associated circuit act as RF Amplifier and Antenna Driver.
- U1 W55MID50 acts as RFID Reader.
- X1 and associated circuit act as 13.56 MHz Oscillator.
- U3 W588D400 acts as MCU and Sound Synthesizer.
- U4 W551C320 and U5 W551C320 act as ROM.
- Q4 and associated circuit act as Audio Amplifier.

Antenna Used :

Two integral loop antennas have been used.

General Description

Winbond *MFID*^{WB} (Magnetic Field Identification) series is used in all areas of automatic data capture allowing contactless identification of objects using magnetic field. From ticketing to industrial automation and access control, the applications of MFID are burgeoning. In recent years automatic identification procedures have become very popular in many service industries, purchasing and distribution logistics, industry, manufacturing companies and material flow systems.

W55MID50 is one of series in Winbond *MFID*^{WB} family that supports multi-functional Reader solution and especially focus on toy, security, and consumer related applications. The applications with Winbond *MFID*^{WB} Tag series such as W55MID10 that provides read-only mask ROM-ID version transponder for mass production solution in toy industrial, meanwhile W55MID15 provides the other solution for manufacture option, which is 243 bonding-ID selection transponder. Besides the single tag transponder application, W55MID35 offers multi-transponder recognition function for intelligent and smart toy applications.

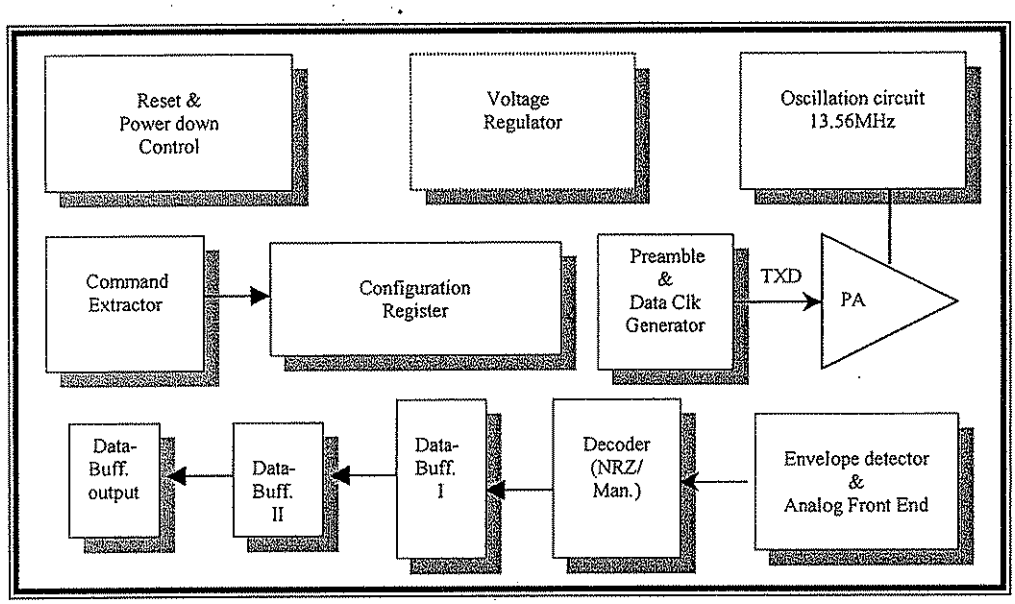
W55MID50 provides a wide variety of applications for toy, security, and consumer market meanwhile the W55MID50 is the most cost effective solution on current *MFID*^{WB} related application market.

1.1 W55MID50 Features

- Magnetic field resonance frequency: 13.56MHz
- Data clock: 22 ~ 66KHz
- Inductive coupled power supplies for transponder's no battery operation
- On-chip rectifier, voltage limiter, clock extraction, power management, uC interface
- Provides NRZ and Manchester coding data format
- Adjustable 4-level of Reader transmission power selection
- Provides serial and parallel mode uC interface
- uC data output rate ≥ 1Mbps
- Low power, low voltage operation
- Supports power-down mode ≤ 1uA
- Operating distance: 0 ~ 10cm
- Operating voltage: 2.4V ~ 5.5V
- Operating temperature: 0 ~ 70 °C
- Package: Dice form, PDIP-20, SOP-20
- Reference design PC board Size: 2.0x2.0cm^2 (without PCB antenna)
- Winbond patented "Automatic Reader Transmission Power Adjustment" for Reader optimum transmission power adjust
- Minimize external components

System Description

2.1 W55MID50 System Block Diagram



2.2 W55MID50 Functional Description

Transmission Power Amplifier (PA)

It provides 4 different selectable transmission power for Reader chip to support *MFID*^{WB} Tag's radiation power supply. The external inductor coupling circuit is designed for 13.56MHz magnetic field resonance. The coupled center frequency will depend on equivalent value of external PCB inductor and capacitor.

Envelope Detector & Analog Front End

The major function of this unit provides *MFID*^{WB} Tag's data can be extracted.

Voltage Regulator

The voltage regulator generates the system needs of device power supply.

Configuration Register

System configuration register controls the all functional settings of W55MID50 such as Tag data

format, Tag detection cycle, output data format, and PA transmission power selection.

Reset and Power-down Control

The function of system power-down control mode is normally used for power consumption saving.

Crystal Oscillation

The 13.56MHz system clock generator generates the need of device system clock.

Decoder NRZ/Manchester

This unit is in charge of Tag data format decoder, which can provide Tag-ID data format decoding of NRZ or Manchester.

Data Buffer and Output

This unit buffers the Tag-ID data, which is under de-frame processing.

1. GENERAL DESCRIPTION

The W588Dxxx is a powerful embedded microprocessor (uP) dedicated to speech and melody synthesis applications. This series chips are suitable for plush toys, educational Q&A toys, or interactive application. W588Dxxx can synthesize multi-channel speech and melody. 3-track of synthesized speech can be in different kinds of format, for example ADPCM and MDPCM. Regarding synthesized melody, W588Dxxx can provide 2-track of Tone melody (T-melody), or 3-track of High-Quality melody (HQ-melody) that can emulate the characteristics of musical instruments. In general speaking, W588Dxxx series can accomplish multi-tasking requirements easily and make toys with more complicated than traditional *PowerSpeech*.

The W588Dxxx provides at most 8 input pins & 24 bi-directional I/Os, maximum 512 bytes RAM, IR carrier, Serial Interface Management, and 32KHz-Divider for more and more sophisticated applications, such as interactive toys, cartridge toys and final count down function. 3 LED output pins with 256-level control means that numerous combination of RGB colors may result in a versatility of colorful effects. W588Dxxx has two kinds of power saving modes: one is Slow mode and the other is STOP mode. In addition, W588Dxxx also provides PWM mode output to save power during playback and Watch Dog Timer to prevent latch-up situation occurring.

ITEM	W588D003	W588D006	W588D009	W588D012	W588D015
*Duration	4 sec.	6 sec.	12 sec.	15 sec.	19 sec.
ITEM	W588D020	W588D025	W588D030	W588D035	W588D040
*Duration	25 sec.	29 sec.	32 sec.	44 sec.	50 sec.
ITEM	W588D045	W588D050	W588D055	W588D060	W588D070
*Duration	53 sec.	58 sec.	62 sec.	66 sec.	86 sec.
ITEM	W588D080	W588D100	W588D120	W588D150	W588D170
*Duration	100 sec.	118 sec.	134 sec.	169 sec.	203 sec.
ITEM	W588D210	W588D260	W588D300	W588D350	W588D400
*Duration	237 sec.	271 sec.	313 sec.	358 sec.	407 sec.

Note:

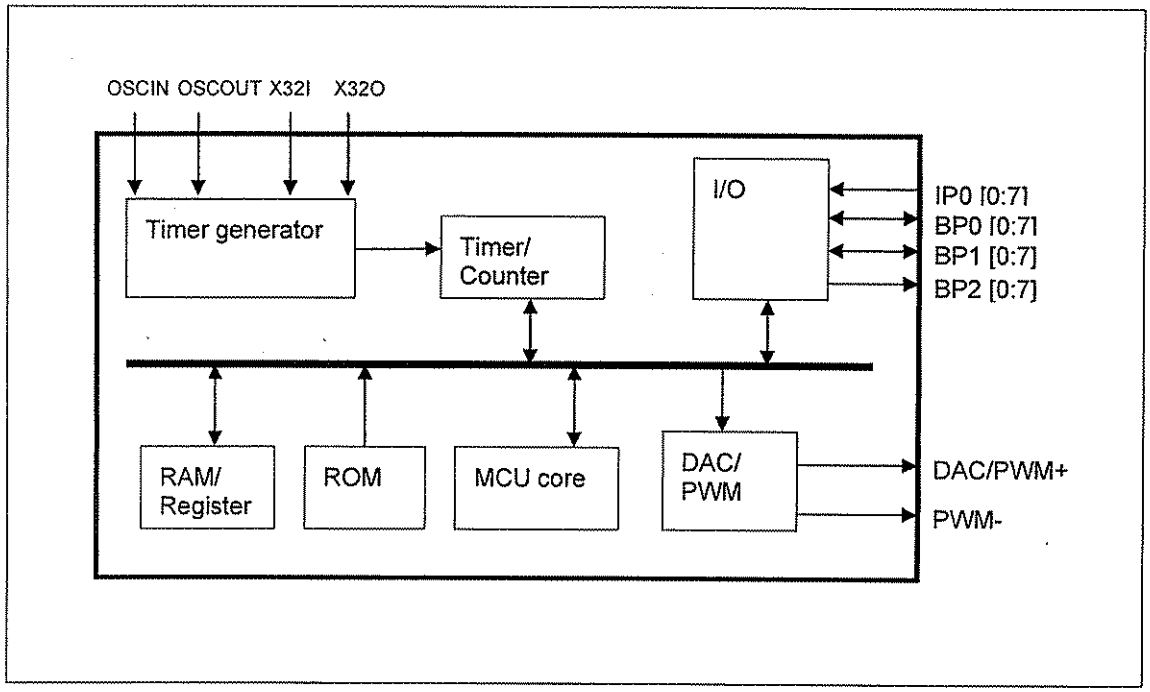
*: The duration time is based on 5-bit MDPCM at 6 KHz sampling rate. The firmware library and program code have been excluded from user's ROM space for the duration estimation.

2. FEATURE

- Wide range of operating voltage:
  - 8 M Hz @ 3.0 volt ~ 5.5 volt
  - 6 M Hz @ 2.4 volt ~ 5.5 volt
- Provide power management to save current consumption:
  - 4 ~ 8 MHz system clocks, with Ring type or crystal type.
  - Slow mode to save power.
  - Stop mode for stopping all IC operations.
- F/W speech synthesis:
  - Multiple format parser that supports
    - ✓ 6-bit MDPCM, 5-bit MDPCM, 4-bit ADPCM, 8-bit Log PCM algorithm can be used
  - Pitch shippable ADPCM for voice changer application
  - Programmable sample rate
- F/W melody synthesizer
  - 2 tracks Tone melody which can emulate envelope of music instruments
  - 3 tracks High-Quality melody that can emulate characteristic of musical instruments
  - Voice melody can be implemented in 2 octaves
- Built-in 3 timers for speech/melody synthesis
  - 3 tracks speech
  - 1 speech channel plus dual-tone melody
  - 3 tracks High-Quality melody
- Harmonized synchronization among MIDI, Speech, LED, and Motor
- I/O configuration:
  - W588D003~D060: 16 I/O pins
  - W588D070~D260: 24 I/O pins
  - W588D300~D400: 8 input pins and 24 I/O pins
- Built-in IR carrier generation circuit for simplification firmware IR application
- Built-in IR receiver counting circuit for simplifying IR decoding
- Build-in 3 LED outputs with 256-level control of brightness.
- Built-in TimerG1 for general purpose applications
- Built-in Watch-Dog Timer (WDT) and Low Voltage Reset (LVR)
- Built-in 32 KHz crystal oscillator with divider for time-keeping application
- Provide serial interface
  - W55Fxx, W551Cxx
  - SPI flash
- Built-in Serial Interface Manager (SIM) in all W588Dxxx series
- 13-bit Current type digital-to-analog converters (DAC) to drive speaker output

- Direct-drive 12-bit PWM output to save power consumption
- Support ***PowerScript***^{TM} for developing codes in easy way.
- Full-fledged development system
  - Source-level ICE debugger (Assembly & ***PowerScript***^{TM} format)
  - ***Ultra I/O***^{TM} tool for event synchronization mechanism
  - ICE system with USB port
  - User-friendly GUI environment
- Available package form:
  - COB is essential

4. BLOCK DIAGRAM



Notes:

1. IP0 is only providing in W588D300, W588D350 and W588D400.
2. BP2 isn't provided in W588D003 ~ W588D060.

Winbond Electronics Corp.

1. GENERAL DESCRIPTION

The W551Cxxx series is a serial voice memory IC designed to interface directly with Winbond *PowerSpeech™*, *BandDirector™*, and *ViewTalk™* family ICs to meet the increasing market demand for longer playback duration. The W551Cxxx uses the same three-pin serial interface that Winbond serial flash memory W55Fxx uses, which makes it easier to simulate and verify the memory contents in advance. In addition, the W551Cxxx also provides a "Self-test mode" to verify the voice memory contents easily and quickly, and some members of the W551Cxxx series allow W551Cxxx chips to be "cascaded" to further lengthen playback duration.

W551Cxxx Serial Voice Memory is used to store pre-determined data. The following table shows the part numbers in the W551Cxxx series and their respective memory density.

PART #	W551C002	W551C005	W551C010	W551C020	W551C040	W551C060	W551C080
DENSITY	256K bits	512K bits	1M bits	2M bits	4M bits	6M bits	8M bits

PART #	W551C160	W551C240	W551C320
DENSITY	16M bits	24M bits	32M bits

1.1 W551Cxxx Features Description

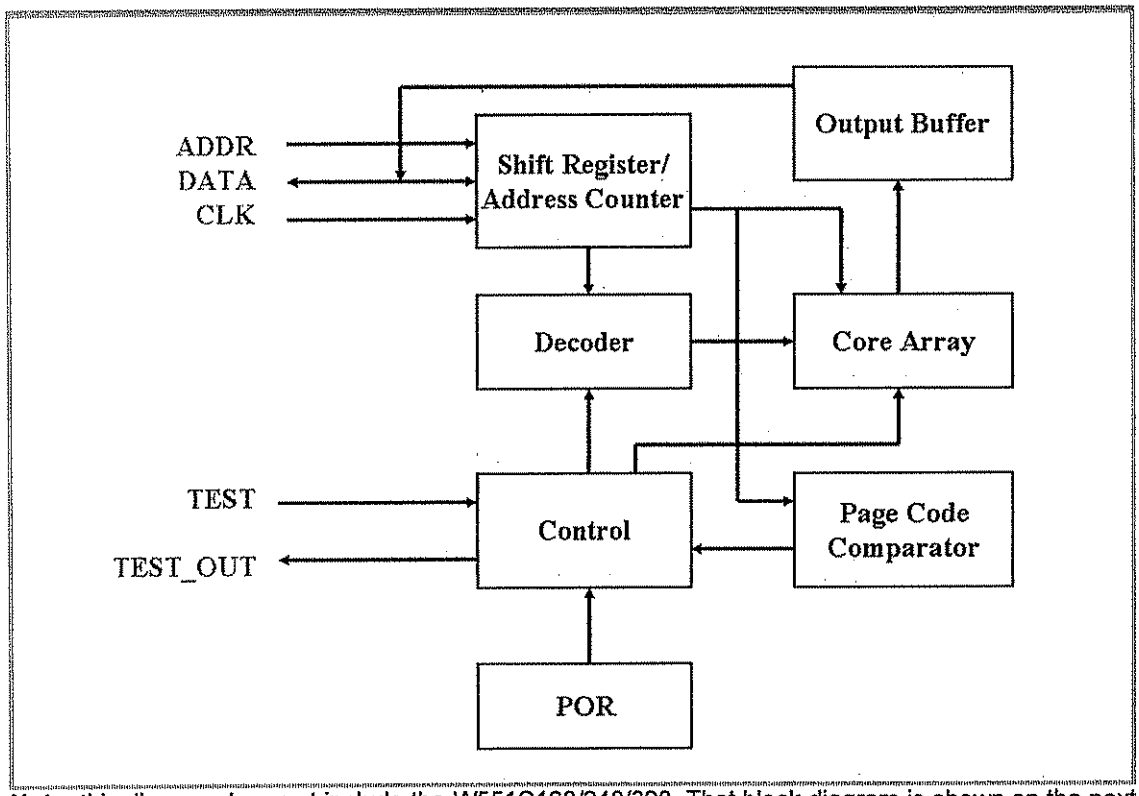
- Wide range of operating voltages: **2.4 V ~ 5.5 V**
- Operating frequency up to **1 MHz** (@VDD = 2.4 V)
- Versatile operating modes
  Serial read mode
  Serial check-sum output mode (used for manufacturing testing only)
  Fast self-test mode
- Cascading for longer duration applications
- Serial shift-in address bus
- Serial data mode
- Three-pin connection interface: CLK, ADDR, DATA
- Read access time: **500 ns**
- Low power consumption
  Operating current: **5 mA (typ.)**
  Standby current: **2 uA (typ.)**

2. FUNCTION DESCRIPTION

This section provides the system block diagrams, followed by explanations of each mode. Note that serial check-sum output mode is not discussed in these latter sections, as it is only used in manufacturing testing.

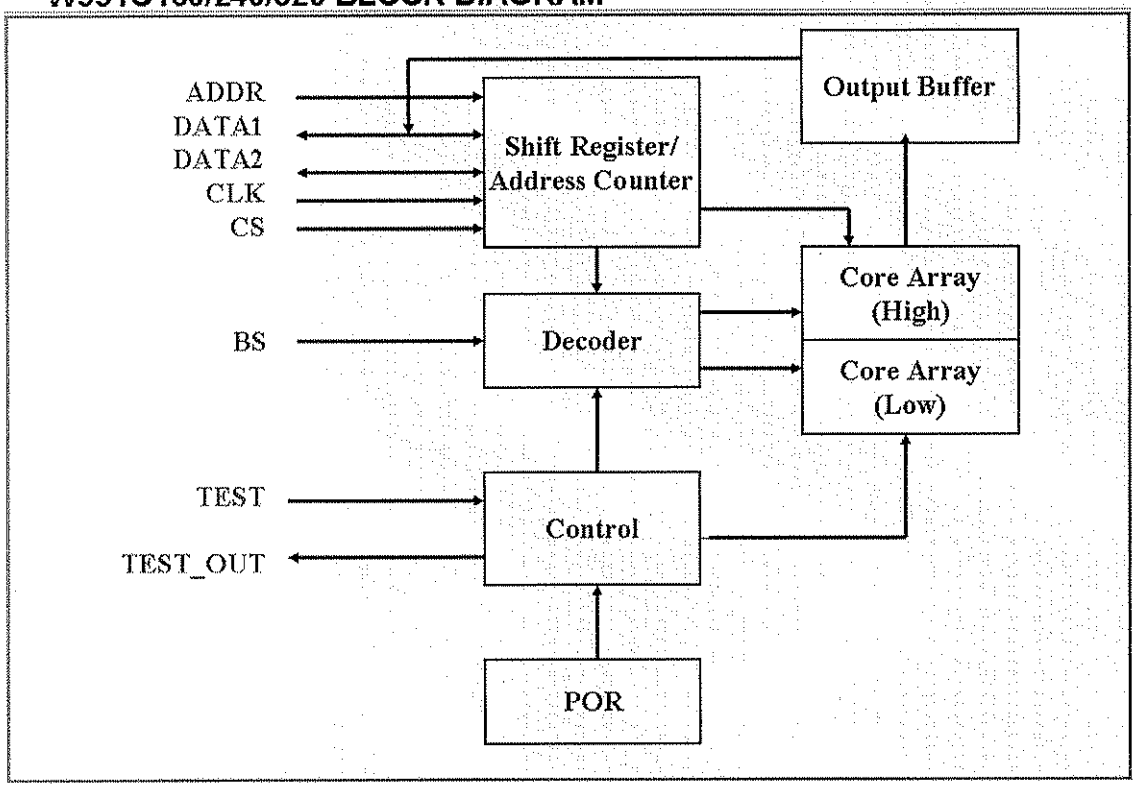
2.1 W551Cxxx System Block Diagram

W551Cxxx BLOCK DIAGRAM



Note: this diagram does not include the W551C160/240/320. That block diagram is shown on the next page.

W551C160/240/320 BLOCK DIAGRAM



2.2 W551Cxxx Serial Read Mode

The default mode is serial read mode.

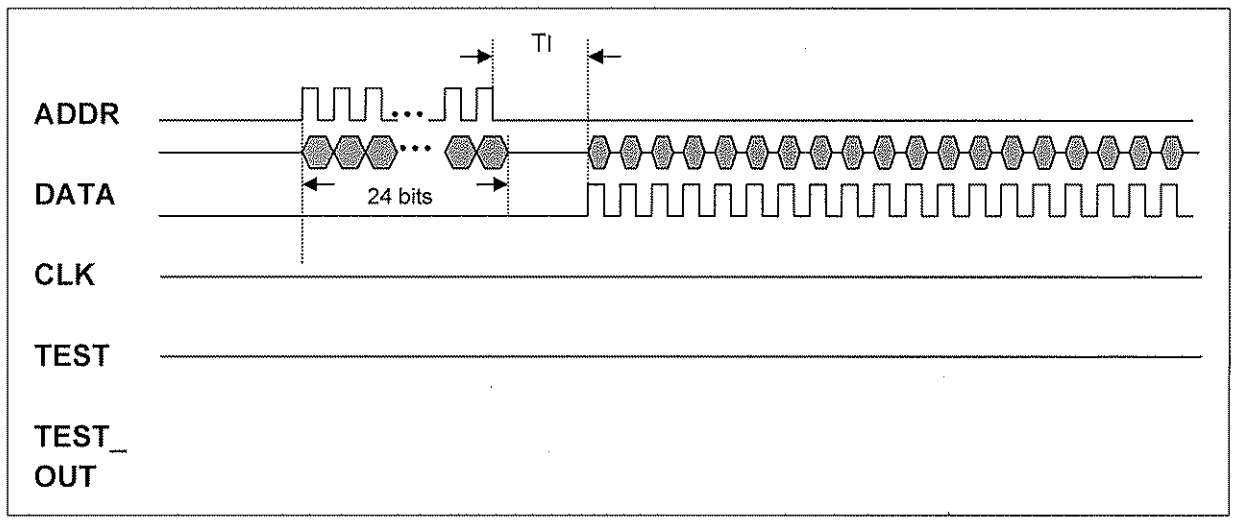
The address is 24 bits long. The MSB x bits are the page code, and the remaining (24 - x) bits are the offset address. The address data is shifted, MSB first, into the address counter by the ADDR clock, and the device is enabled if the page code matches the content of the W551Cxxx page-code cells. The number of bits in the page code varies by part number and is shown below.

PART #	W551C002	W551C005	W551C010	W551C020	W551C040	W551C060	W551C080
DENSITY	256K bits	512K bits	1M bits	2M bits	4M bits	6M bits	8M bits
PAGE CODE	6 bits	5 bits	4 bits	3 bits	2 bits	2 bits	1 bit

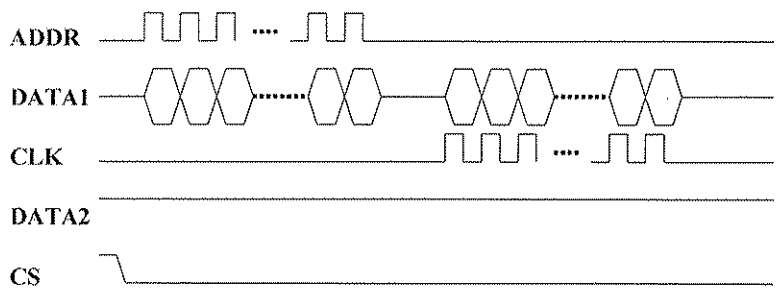
PART #	W551C160	W551C240	W551C320
DENSITY	16M BITS	24M BITS	32M BITS
PAGE CODE	0 BITS	0 BITS	0 BITS

Note: the W551C160/240/320 do not have a page code.

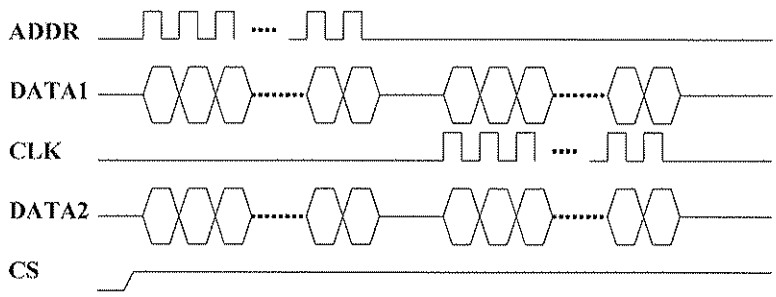
The first rising-edge signal in the ADDR clock resets the address shift registers. Once the address data has been shifted into the address counter (and the page code bit[s] verified), the falling-edge of the CLK clock increments the address counter. As a result, in serial-read mode, the ADDR and CLK clocks should not be active simultaneously. This is illustrated in the timing diagram below.



Serial read-mode also supports cascaded W551Cxxx chips. Cascading allows additional W551Cxxx chips to be connected to a W551C160/240/320 chip and effectively increases the amount of accessible memory. In the connection, all the W551Cxxx chips still share the same ADDR and CLK clock sources, but the data bus is routed through the W551C160/240/320 DATA1 and DATA2 pins. When the /CS pin is low, the W551C160/240/320 ignores any connected chips and responds accordingly on DATA1. When the /CS pin is high, however, the W551C160/240/320 enters cascade mode, and address data and the resulting read-data are passed through the W551C160/240/320. The timing diagrams for the W551C160/240/320 are shown below, and a sample circuit diagram is shown in the **Application Circuits** section.



READ DATA FROM W551C320



READ DATA FROM CASCADE THROUGH W551C320

2.3 W551Cxxx Self-test Mode

The self-test process starts on any falling edge on the TEST pin. The self-test process accumulates every byte of voice memory in the chip. (The actual number of bytes depends on the part number.) If the accumulated result is 00h, no problem was detected, and a logic **'0'** is output on the TEST_OUT pin. Any other result indicates an error, and a logic **'1'** signal is output on the TEST_OUT pin.