FCC ID: LU9322245

Technical Description :

The brief circuit description is listed as follows :
- X1, L1, C2 and associated circuit act as 27.149 MHz Oscillator.
- U1 and associated circuit act as Encoder and Modulator.
- Z1 and associated circuit act as Voltage Regulator (4.3V).
- Q1 and associated circuit act as RF Amplifier.
- SW1-SW3 act as Control Keys.

Antenna Used :

An integral antenna has been used.

FIVE FUNCTIONS REMOTE CONTROL ENCODER/DECODER PAIRS

1. GENERAL DESCRIPTION

These two devices are especially designed is use as paired encoder/decoder in remote control (RC) applications.

The GPRC205A1, a RC encoder, is able to encode five lines of binary information into a serial bit-stream data. When any of the 5-line information is activated, built-in crystal oscillator and power amplifier will be enabled to deliver the encoded bit-stream data. After the 5-line information becomes inactive, the GPRC205A1 will transmit additional fifteen data frames to increase transmission reliability.

The GPRC206A1 is a remote control decoder, which decodes the serial bit-stream data received from the GPRC205A1 and interprets the 5-line information as 5-bit output data to control the corresponding external component. The GPRC206A1 will be activated only when two consecutive and equal frames are received.

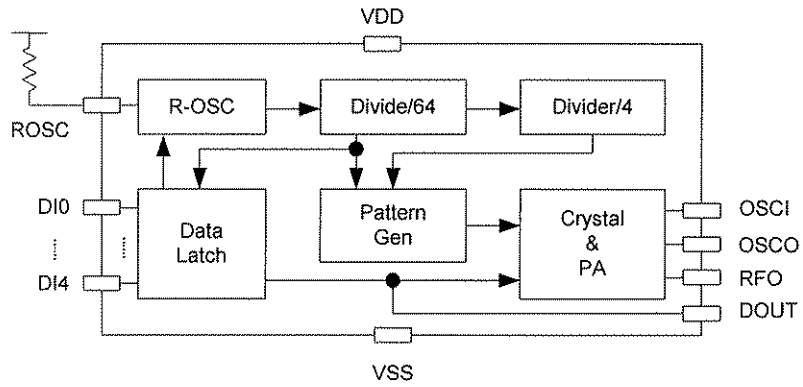
With GENERALPLUS state-of-the-art technology and strong support, GPRC205A1 and GPRC206A1 are the simplest and most suitable products for your RC products.

2. FEATURES

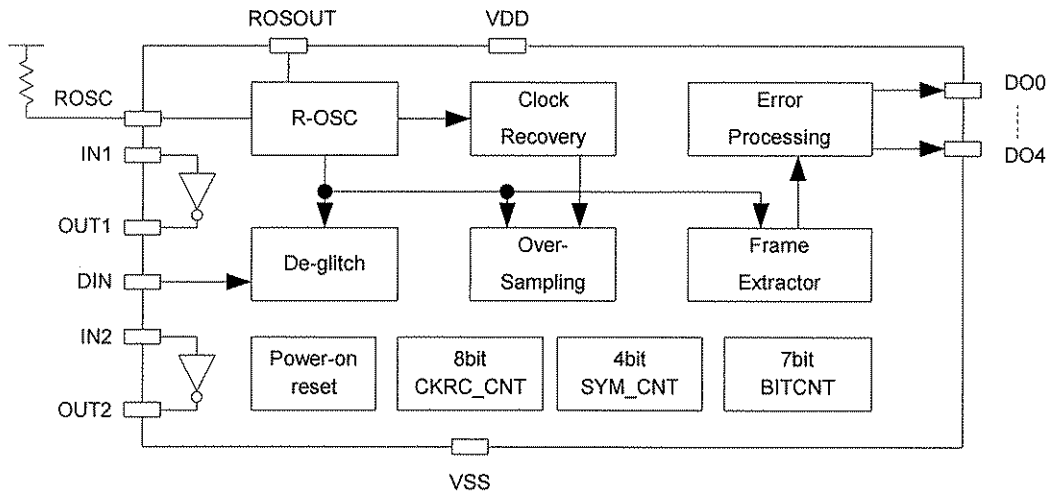
- Operating voltage
  - 2.2V - 5.5V operation
- Built-in R-oscillator (a 5% resistor required)
- Low standby and operating current
  - $I_{STBY,GPRC205A1}$ < 1.0μA, R-oscillator stops
  - $I_{OPERATE,GPRC205A1}$ < 15mA, R-oscillator free run, crystal & PA on
  - $I_{OPERATE,GPRC206A1}$ < 100μA, R-oscillator free run
- Built-in power on reset
- Built-in Crystal & PA in GPRC205A1
- 5-function I/O pins
- 2^5 = 32 encoding in GPRC205A1
- Variable frame rates controlled by external resistor

3. BLOCK DIAGRAM

GPRC205A1



GPRC206A1



5. FUNCTIONAL DESCRIPTIONS

5.1. Frame Format

Preamble						PO	E	D0	D1	D2	D3	D4
P	P	P	P	P	P	A/I	A/I	A/I	A/I	A/I	A/I	A/I

Preamble field: 6 preamble fields

PO field: Even parity check field

E field: Frame polarity indication field; frames are transmitted in positive/negative sequence.

Data field: 5 data fields

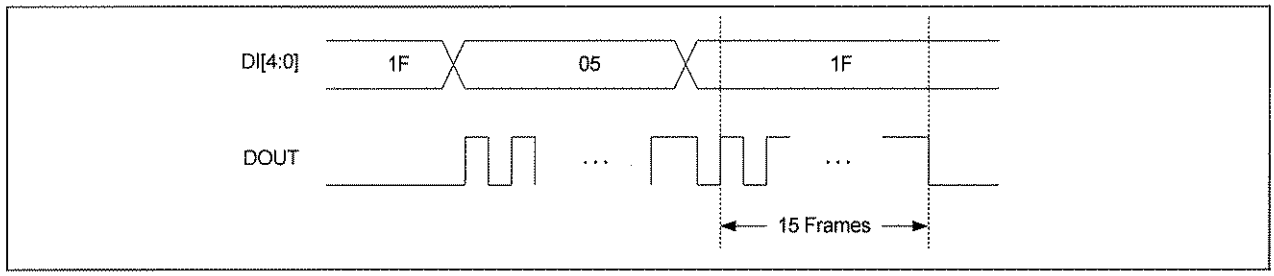
P pattern: encoded as 10

A pattern: encoded as 100

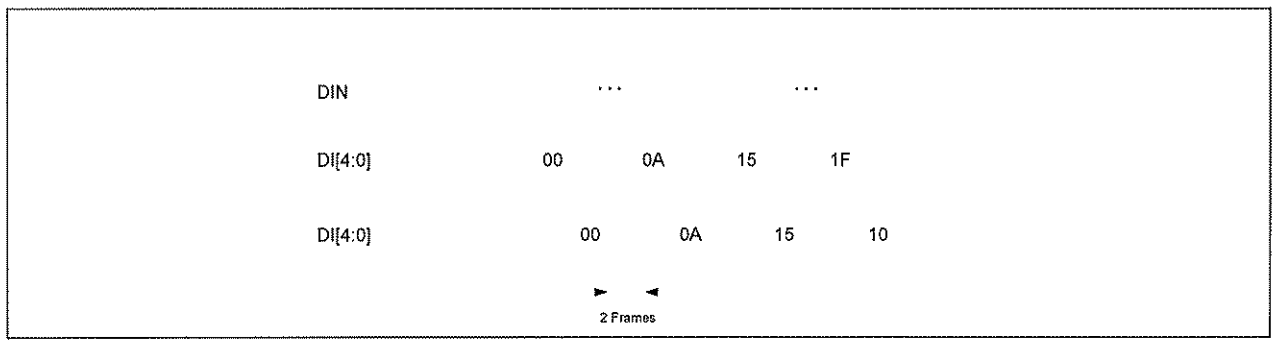
I pattern: encoded as 110

5.2. Operation

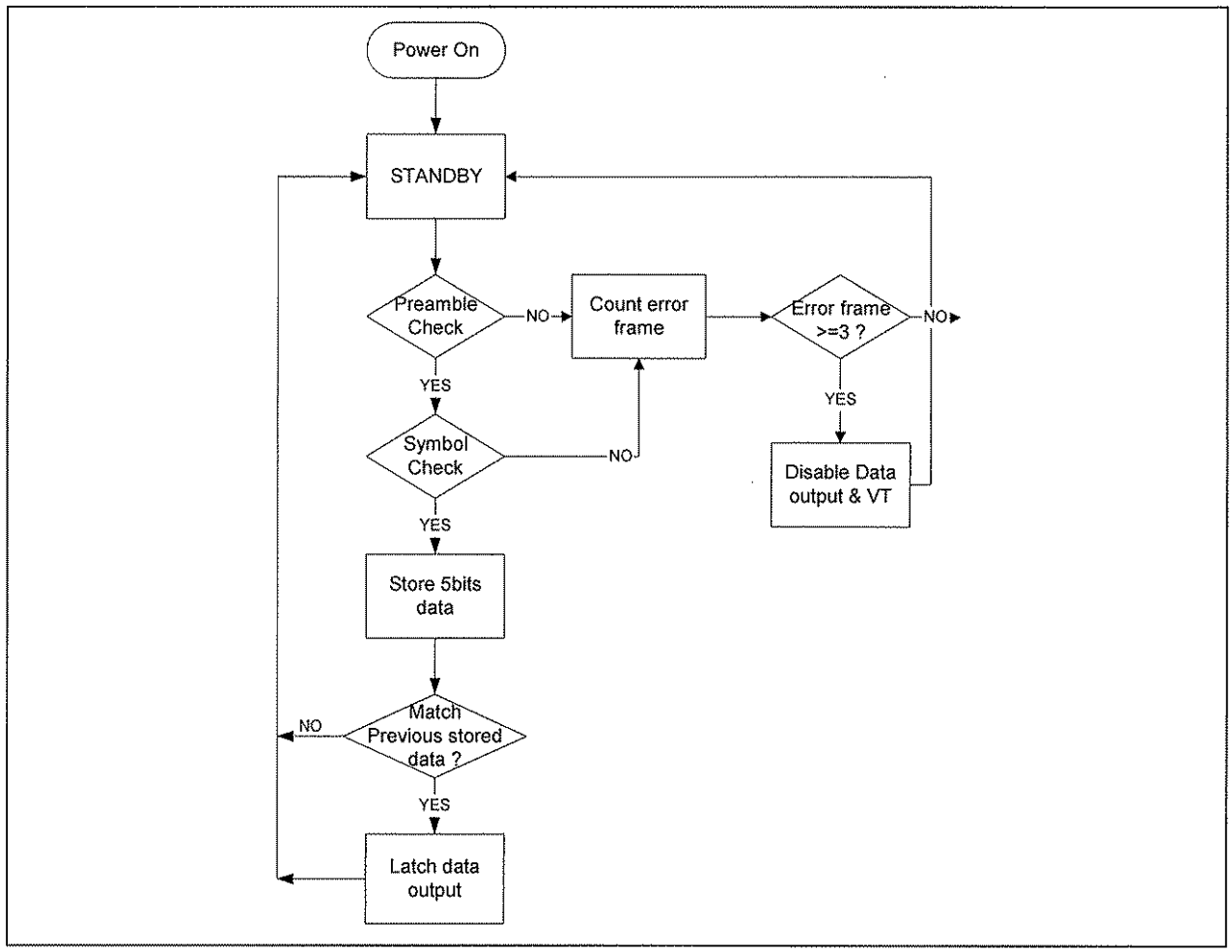
The GPRC205A1 encodes 5-function information into 2^5 series of bit-stream data and transmits the encoded data stream via RFO when any of the 5-function I/Os is activated. The cycle will repeat until all 5-function I/Os become inactive. After these 5-function I/Os become inactive, GPRC205A1 will transmit another 15 all-zero frames to inform GPRC206A1 returning to disabled state. The transmitting timing is shown as follows:



The GPRC206A1 is able to receive serial bit-stream data transmitted from GPRC205A1 and decode the data fields as 5-bits data output. Any signal on DIN pin will activate GPRC206A1 to decode the incoming data. When GPRC206A1 receives two consecutive, correct and equal frames, DO[4:0] is able to control the external component. The DO[1,0] and DO[3:2] are exclusive to each other; that is, DO[1:0] and DO[3:2] cannot be activated at the same time. The receiving timing is shown below:



5.3. Decoder Flow Chart



After power on, it is reset at STANDBY state. When the signal on DIN is received by GPRC206A1, it will check the incoming data frame structure. If preamble or data field errors occur, it will back to STANDBY state to check the next frame. If the receiving frame structure passes the preamble and symbol checks, the 5-bit data is stored and then compared to the previous stored 5-bits data. If the present data matches the previous data, DO[4:0] is active and it is back to STANDBY and ready to check the next frame.

5.4. R-oscillator

Both GPRC205A1 and GPRC206A1 have built in R-oscillator. Users need only one resistor (or a capacitor if needed) to implement the clock input and to change the frame rate by replacing different resistor.

Frame rate = F_{osc} / 64 / 33

In addition, the GPRC206A1 built-in a Clock Recovery block to automatically adjust the ratio of data rate to clock rate. The only limitation is using a 5% accuracy resistor is required in GPRC205A1 and GPRC206A1.

5.5. Super Regeneration Amplifier

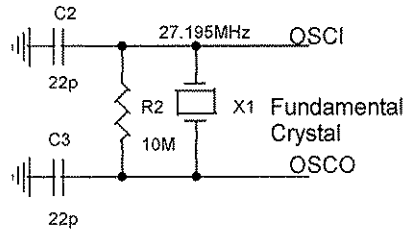
The GPRC206A1 features two inverter inputs and outputs as pins. The two inverters can be used for amplifier of the Super-Regeneration RF receiver data output. Users can change the two inverters' gain by adjusting external resistor and capacitor.

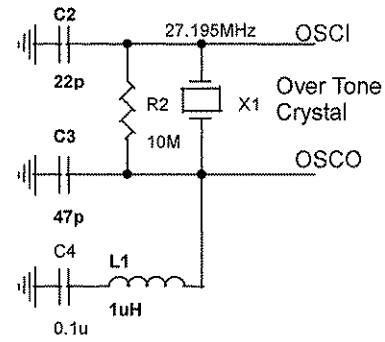
7.6. Crystal Oscillator Example

For over tone type crystal, a LC tank circuit is necessary to prevent base tone oscillating.

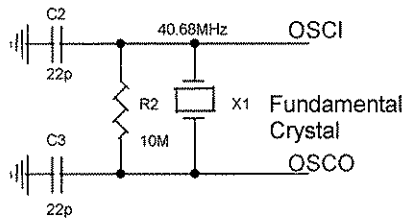
$$Fx > \frac{1}{2\pi\sqrt{LC}}, Fx = \text{crystal frequency}, L = L1, C = C3$$

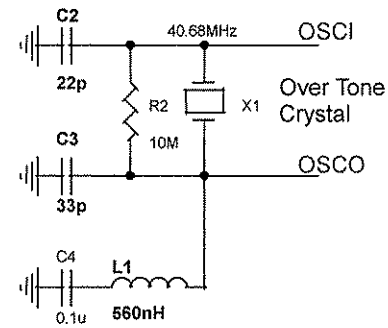
27MHz Oscillator Circuit



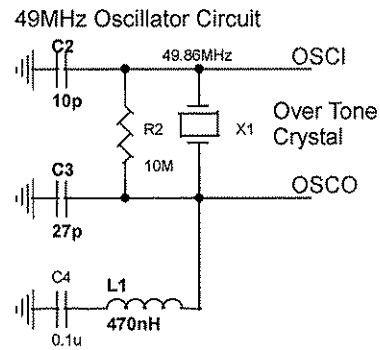


40MHz Oscillator Circuit





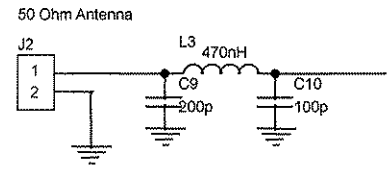
49MHz Oscillator Circuit



Note: There are different values of C2, C3 and L1 for 27MHz, 40MHz and 49MHz. User must use these values correctly, otherwise it possibly casues oscillator circuit malfunction.

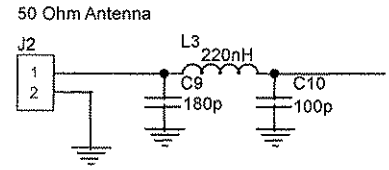
RF Output Matching Example

27MHz Matching Circuit



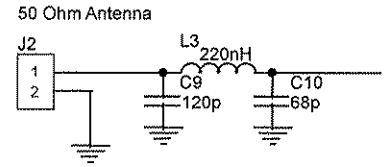
Matching to 50 Ohm load

40MHz Matching Circuit



Matching to 50 Ohm load

49MHz Matching Circuit



Matching to 50 Ohm load