DELPHI
Automotive Systems

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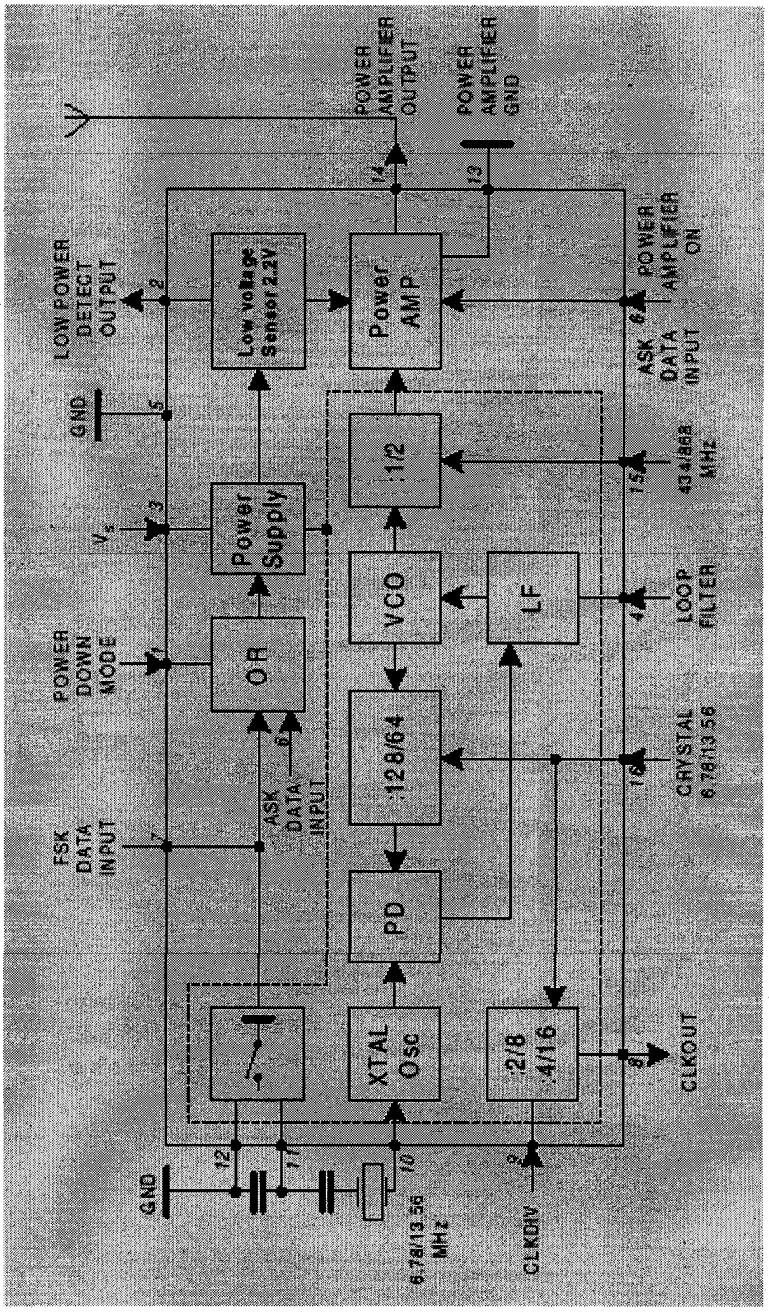
Partner of the Automotive Industry

Technical Description and Block Diagram of the Transmitter IC of SA-AM 433,92MHz

(Source: Infineon Technologies)

Block Diagram



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Technical Description

1. PLL Synthesizer

The Phase Locked Loop synthesizer consists of a voltage controlled oscillator (VCO), an asynchronous divider chain, a phase detector, a charge pump and a loop filter and is fully implemented on chip. The tuning circuit of the VCO consisting of spiral inductors and varactor diodes is on chip, too. Therefore no additional external components are necessary. The nominal center frequency of the VCO is 869 MHz. The oscillator signal is fed both to the synthesizer divider chain and to the power amplifier. The overall division ratio of the asyncronous divider chain is 128 in case of a 6.78 MHz crystal or 64 in case of a 13.56 MHz crystal and can be selected via pin 16 (CSEL). The phase detector is a Typ IV PD with charge pump. The passive loop filter is realized on chip.

Table 1

CSEL	Crystal Frequency
Open	13.56 MHz
Shorted to ground	6.78 MHz

2. Crystal Oscillator

The crystal oscillator operates either at 6.78 MHz or 13.56 MHz. In case of FSK transmission the oscillator frequency can be detuned by a fixed amount determined by an external capacitor via pin 7 (FSKDTA). For both quartz frequency options 847.5 kHz or 3.39 MHz are available as a clock frequency output (CLKOUT) to drive the clock input of a micro controller. The dividing ratio is controlled by the CLKDIV pin.

Table 2

FSKDTA	FSKOUT Switch
Open	OFF
Shorted to ground	ON

Table 3

Crystal Frequency	CLKDIV	Dividing Ratio
6.78 MHz	Shorted to ground	2
13.56 MHz	Shorted to ground	4
6.78 MHz	Open	8
13.56 MHz	Open	16

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3. Power Amplifier

In case of operation in the 868-870 MHz band the power amplifier is fed directly from the voltage controlled oscillator. In case of operation in the 433-435 MHz band the VCO frequency is divided by 2. This is controlled by the FSEL pin as described in the table below. In FSK transmission the power amplifier can be switched on with pin 6 (ASKDTA). In case of ASK transmission the same pin is used as the data input.
The PAOUT pin is an open collector output and requires an external pull up coil to provide bias. The coil is part of the tuning and matching LC circuit to get best performance with the external loop antenna. To achieve the best power amplifier efficiency the high frequency voltage swing at the PAOUT pin should be two times the supply voltage.
The power amplifier has its own ground pin (PAGND) in order to reduce the amount of coupling to the other circuits.

Table 4

FSEL	Radiated Frequency Band
Open	869 MHz
Shorted to ground	433 MHz

4. Low Power Detect

The supply voltage is sensed by a low power detector. If the supply voltage drops below 2.15 V the power amplifier can be turned off via pin 6. To minimize the external component count, an internal pull-up current of 40µA gives the output an high state at supply voltages above 2.15V.

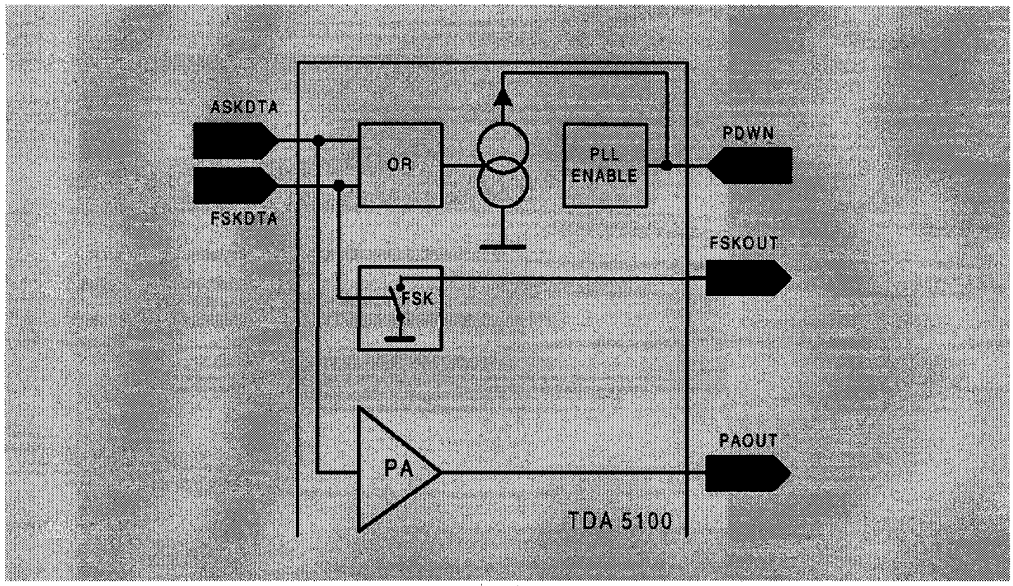
5. Power Modes

The IC provides three power modes, the POWER DOWN MODE, the PLL ENABLE MODE and the TRANSMIT MODE. How to get in this modes is described in the table below.

Table 5

PDWN	FSKDTA	ASKDTA	
L	L	L	POWER DOWN MODE
H	L;H	L	PLL ENABLE MODE
not connected;H	H	L	PLL ENABLE MODE
not connected,H	L;H	H	TRANSMIT MODE

If ASKDTA or FSKDTA gets high, the PDWN pin is pulled up internally via a current source as shown in figure 1. Therefore, in most applications it is not necessary and recommended to connect the PDWN pin.



Power_Mode.wmf

Figure 1 Power mode

6. Power Down Mode

In the POWER DOWN MODE the current consumption is less than 100nA. To switch the IC in this mode, the input pins PDWN (pin1), ASKDTA (pin6) and FSKDTA (pin7) has to be in the low state.

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7. PLL Enable Mode

The turn on time of the PLL is determined by the turn on time of the crystal oscillator and is typically less than 1 msec (dependent on the crystal itself). To save current consumption and to avoid undesired power radiation during this time, the power amplifier is turned off. The current consumption at this mode is typically 3.5 mA.
To have the possibility to control the IC via two data lines from a micro processor, the ASK- and FSK Data inputs are connected via a "logical or" to pull up internally the PDWN input. In this case, it is recommended to leave the PDWN pin unconnected.

8. Transmit Enable Mode

In the TRANSMIT ENABLE MODE the power amplifier is turned on too, and the current consumption of the IC is about 7 mA (transforming network at the PAOUT). To get in this state, the ASKDTA input is to switch to a high level.

9. Recommended timing diagrams for ASK-modulation

ASK Modulation :
(Pin1 (PDWN) not connected)

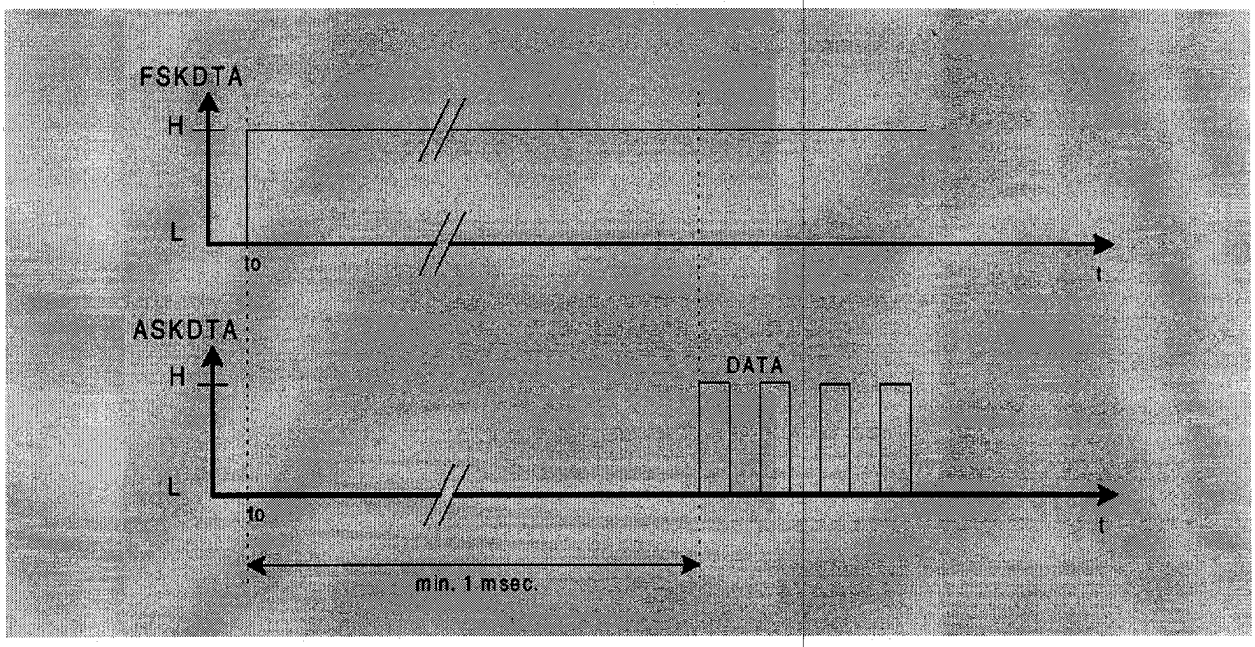

Figure 2 ASK Modulation