Exhibit A

Circuit Description

Receiver

The receiver is a double-conversion superheterodyne type designed for narrow band FM reception in the frequency range of 850-870 MHz. The first local oscillator is derived from the frequency synthesizer. The second LO is crystal controlled.

RF Stage: The incoming RF signal from the antenna jack is directed to the RF input stage by the antenna switch U5. The RF signal is presented to bandpass filter BPF1 and then to the input of RF amplifier U7. The RF signal is then presented to a second bandpass filter BPF2.

First LO: The first LO signal is developed by the synthesizer and output through SAW filter FL6 for mixing with the incoming signal.

First Mixer: The RF signal is amplified by U6 and filtered by SAW filter FL3. The signal is then amplified and mixed with the first LO signal by U6. The difference component (45 MHz) is filtered by FL1A/FL1B and applied to Q1 the 2nd IF amp.

Second LO/Mixer: The first I.F. signal is presented to U2 which performs the functions of second LO, second I.F. amp and mixer, FM discriminator and squelch. X1 (44.545 MHz) is the second LO crystal and is mixed with the 45 MHz first I.F. signal to produce the second I.F. frequency of 455 kHz. Ceramic filter FL2 provides selectivity for the 455 kHz signal.

Detector/Squelch: U2 demodulates the 455kHz signal via quadrature coil L1 to produce the audio and noise components. The output of U2 is the recovered audio and the RSSI voltage (receiver signal strength indicator) which is compared by the controller board with a threshold voltage level for squelch setting.

Transmitter

The output of VCO2 is input to the driver transistor Q3. The collector of Q3 is fed by the switched Vcc line used to control the RF output. The final amp is a three stage Class AB FET power amplifier and drives the output lowpass and harmonic filter FL5. U5 is the transmit antenna switch controlled by Q2.

Exhibit A

Control Board

Power Supply: DC power comes from the mobile radio via P1 pins 1 and 5. Fuse F1 and MOV VAR1 provide over current and voltage spike protection. Q3 is the remote enable/disable pass switch, controlled by Q1 and Q2 via P1 pin 3. Q3 output is switched 12VDC and is presented to audio amp U6, and voltage regulators U7 and U8. Bias voltage for the op-amp circuits is provided by voltage divider R68, R69 and buffer amp U2A.

Transmit audio path: Receiver audio from the mobile is input to the mic amp portion of U4; PC programming of the SVR-200 provides flat response or +6db/octave pre-emphasis. The output of the mic amp is internally connected to the limiter and lowpass filter. When a condition to repeat exists (base to handheld) U4 audio is switched on and audio is presented to amplifier/limiter and lowpass filter to remove audio components above 3kHz. U4 provides -48db/octave of attenuation to out of band signals. Transmit audio is output on pin 22 of U4 and passes through the final lowpass filter U2C to remove any clock noise genearted by U4's switched capacitive filters before being presented to the RF module on P2 pin 6.

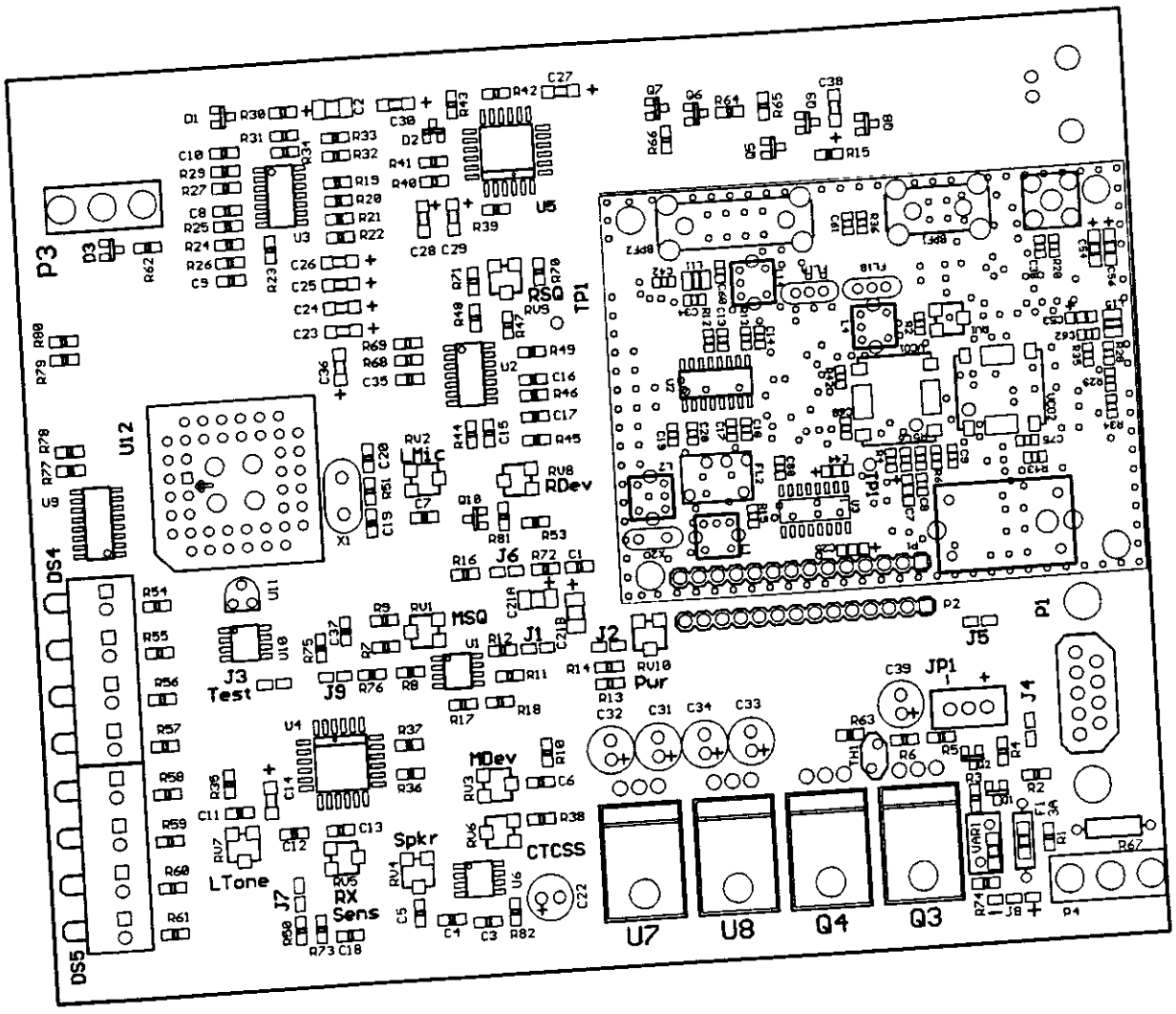
Receive audio path: Receiver audio from the transceiver module is input on P2 pin 13 and presented to U5 pin 10 and pin 16. Pin 10 is the input of the receiver highpass filter to remove any subaudible signals before being output on pin 11 and sent to U4 for receiver audio processsing. Pin 16 is the input to the sub-audible tone decoder section of U5. Receive audio entering pin 7 of U4 is processed as flat, or -6db/octave depending upon PC programming. The receive audio then passes through the internal lowpass filters to remove unwanted noise and output on pin 21, where it is sent to the local receiver audio amp and mobile transmit audio output amp U1B. J1 selects either high sensitivity (open) or low sensitivity (shorted) and J2 selects the output impdedance (600/2.2K Ohms).

Sub-Audible tone siganlling: U5 processes the sub-audible signal from the receiver by comparing the incoming signal to previous samples in a noise correlator. If the signal is sufficently coherent, the output of the comparator is counted by the internal circuitry and an interupt is generated to the main microprocessor. U12 reads the data from U5 in 2 bytes: byte one contains the number of complete cycles detected within 122mS, and byte 2 contains the number of internal clock cycles elapsed for the remainder. U12 performs a comparison of minimum and maximum values allowed in a look up table and determines if the data is within the decode bandwidth for the programmed tone.

In band tone signalling: Audio from the transceiver is also fed to U3B where it is amplified and limited for input to the comutating switched capacitive filter made up by C23-C26 and P0.4-P0.7 of the microprocessor. The microprocessor outputs four identical signals with 90° phase difference on the respective port pins. The resultant wave form will be a function of the difference between the incoming signal frequency and the decode frequency output by the microprocessor. The signal is buffered by U3C and amplified by U3A before being rectified and filtered by D1 and C2. The resulting DC voltageis comparted to the reference voltage by U3D. If the incoming signal is within the decode bandwidth, the output of U3D will be a logic 1 and read by the microprocessor.

Logic and control: U12 provides all of the logic and control functions for the repeater including mobile/repeater PTT output, local mobile PTT sense, mobile transmitter activity sense, audio switching, in-band and CTCSS detect, and repeater status indications via D2 and D3 led arrays.

Exhibit A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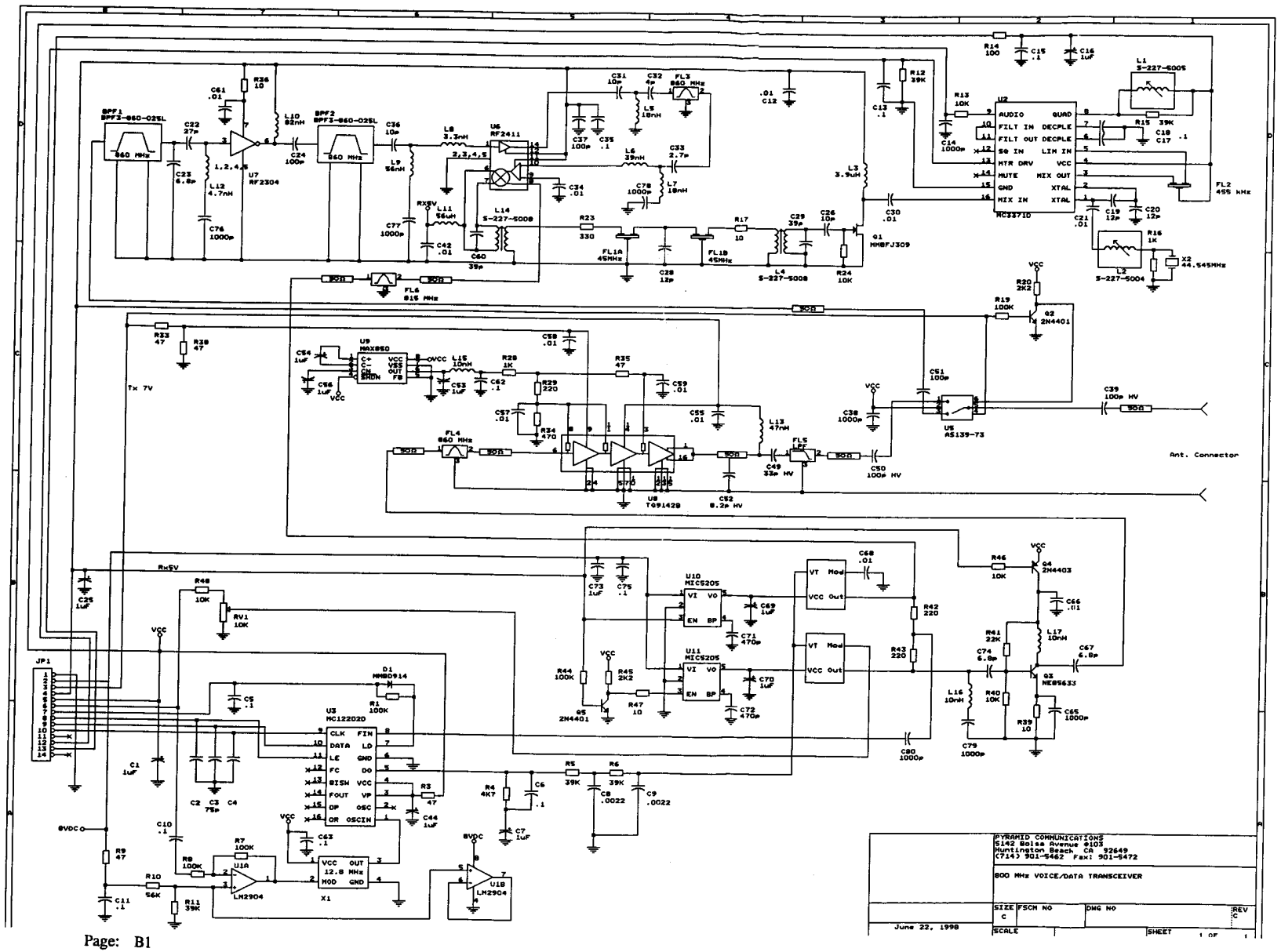
PYRAMID COMMUNICATIONS
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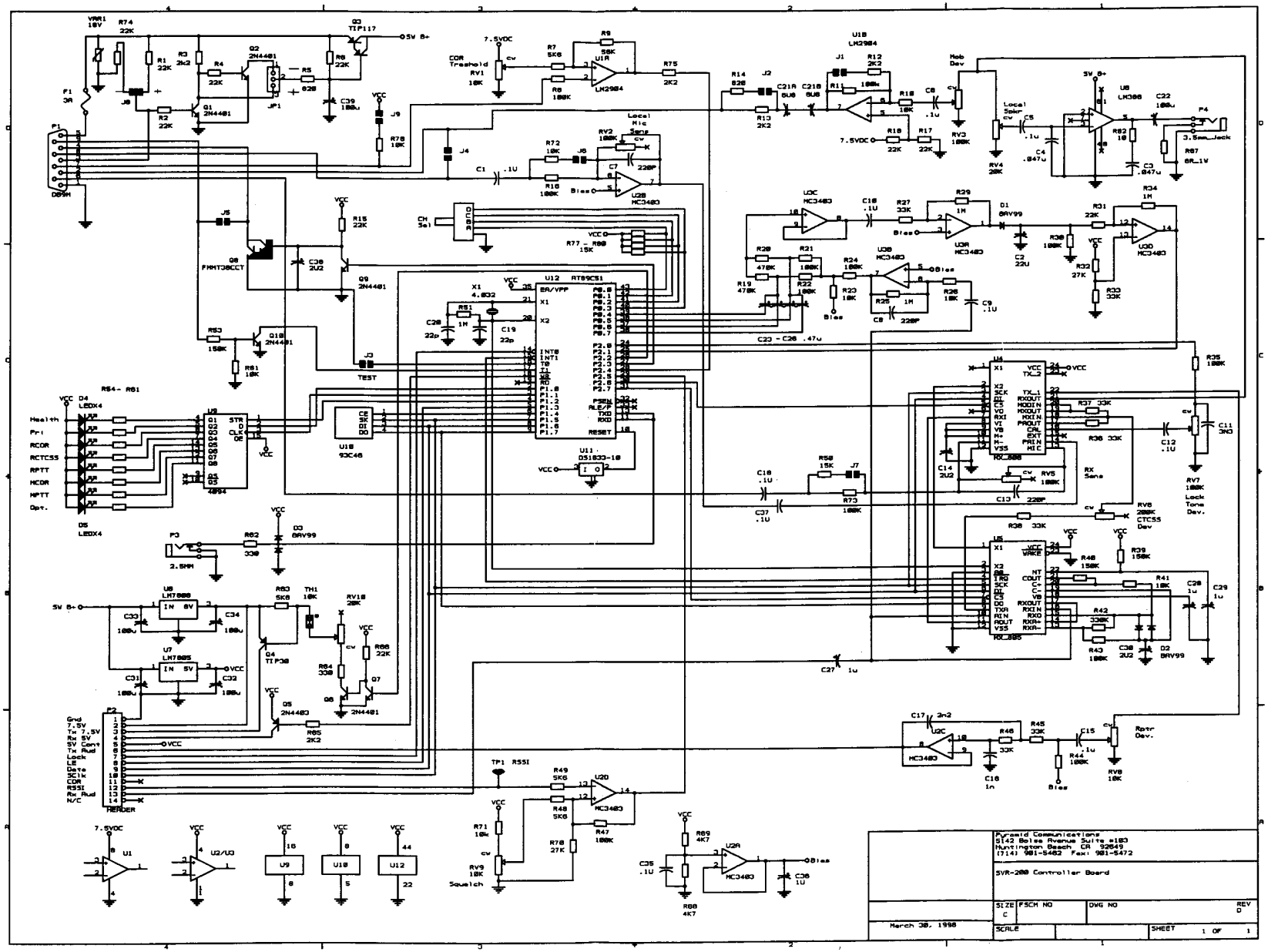
800 MHz VOICE/DATA TRANSCEIVER
SIZE C
FSCH NO
DWG NO
REV C
June 22, 1998
SCALE
SHEET 1 OF 1
Ant. Connector
Tx 7V
RxSV
8VDC
VCC


Pyramid Communications
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SVR-200 Controller Board
SIZE C
FSCH NO
DWG NO
REV D
March 30, 1998
SCALE
SHEET 1 OF 1