To Whom It May Concern:

The antenna for Model Number PCE-302-00-0 is a board etched Omni-directional inverted F – antenna with a gain of approximately 1 dBi.

Freescale IEEE 802.15.4 / ZigBee Package and Hardware Layout Considerations

Reference Manual

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About This Book

This manual describes Freescale's QFN and both LGA packaging considerations, including solder, tape and reel, and design considerations. This manual also provides some information about basic layout and design considerations as they apply to Freescale ZigBee products.

The information in this manual should be used only as a guideline. The user's design may need to be modified depending on the assembly house used and the other components on the board.

Audience

This manual is intended for system and hardware designers responsible for developing products using Freescale ZigBee technology.

Organization

This document is organized into five chapters.

Chapter 1 Introduction — This chapter introduces and provides an overview of the concepts and elements described in this manual.

Chapter 2 QFN Packaging Information — This chapter describe guidelines for a Printed Circuit Board (PCB) footprint and marking for the QFN 32 package used for the MC1319x and MC1320x. Included are layouts of the component copper layer, solder mask, and solder paste stencil.

Chapter 3 71-Pin LGA Packaging Information — This chapter describes Printed Circuit Board (PCB) footprint guidelines for the MC1321x LGA 71 package. Included are layouts of the component copper layer, solder mask, and solder paste stencil.

Chapter 4 99-Pin LGA Packaging Information — This chapter describes Printed Circuit Board (PCB) footprint guidelines for the MC1322x LGA 99 pin package. Included are layouts of the component copper layer, solder mask, and solder paste stencil.

Chapter 5 48-Pin LGA Packaging Information — This chapter describes Printed Circuit Board (PCB) footprint guidelines for the MC1323x LGA 48 package. Included are layouts of the component copper layer, solder mask, and solder paste stencil.

Chapter 6 Layout and Design Considerations — This chapter is intended as a guide for current and future implementations, to smooth the transition from prototype to production.

Revision History

The following table summarizes revisions to this document since the previous release (Rev 1.3).

Revision History

Location	Revision
Chapter 5	Inserted Chapter 5 for public release of MC1323x.

Definitions, Acronyms, and Abbreviations

The following list defines the acronyms and abbreviations used in this document.

ADC	Analog to Digital Converter
AES	Advanced Encryption Standard
ARM	Advanced RISC Machine
CTS	Clear to Send
DAC	Digital to Analog Converter
DMA	Direct Memory Access
I2C	Inter-Integrated Circuit is a multi-master serial computer bus
ISM	Industrial Scientific Medical 2.4 GHz radio frequency band
JTAG	Joint Test Action Group
LGA	Land Grid Array
MAC	Media Access Controller
MCU	Microcontroller Unit
NEXUS	An embedded processor development tool interface that helps design engineers identify software and hardware-level issues.
PCB	Printed circuit board
PiP	Platform in Package
PWM	Pulse-width modulation
RTS	Request to Send
SMA Connector	SubMiniature version “A” connector
SPI	Serial Peripheral Interface
SSI	Synchronous Serial Interface
TACT Switch	A switch that provides a slight “snap” or “click” to the user to indicate function.
TELCO	Telephone Company
USB	Universal Serial Bus
VCP	Virtual Com Port

Recommended Reading

- Freescale Application Note AN2731, Compact Integrated Antennas Designs and Applications for the MC1319x, MC1320x, and MC1321x.
- *Introduction to Choosing MLC Capacitors For Bypass/Decoupling Applications*, http://bears.ece.ucsb.edu/class/ece124d/real_world_decoupling.pdf
- *Via Inductance II High-speed Digital Design*, online newsletter, Vol. 6 Issue 8, Signal Consulting, Inc., http://sigcon.com/Pubs/news/6_08.htm
- *Chip Monolithic Ceramic Capacitors*, Murata Manufacturing Company, Ltd, http://www.murata.com/catalog/c02e13.pdf

Chapter 1
Introduction

Wireless nodes based on the IEEE 802.15.4 Standard are used to implement ZigBee and custom applications. The Freescale highly integrated devices for the 2.4 GHz Instrument, Scientific, and Medical (ISM) band makes it reasonably straight forward to do this high frequency RF design. However, care must still be taken to get reliable, repeatable, and efficient RF performance. Second, these device packages have small physical footprints with small pad sizes. These can affect reliable board assembly, especially with the higher temperature reflow processes required for RoHS-compliant hardware.

This reference manual is intended to give the user pertinent information on the available packages and how to use them. The following paragraphs briefly introduce the available packages and information available in this manual.

1.1 32-Contact Quad Flat Pack No Lead (QFN32)

The Quad Flat Pack No Lead (QFN) package is a lead-less, near Chip Scale Package (CSP) with low profile (1.0 mm and less), moderate thermal dissipation and good electrical performance. The QFN is a surface mount plastic package with leads located at the bottom of the package.

The QFN package is an alternative to the fine-pitch ball grid array (FBGA), the laminate-based chip scale packages (CSP), micro BGA, and flex ball grid array (FxBGA) packages. In comparison to these packages, the QFN provides:

- Better performance in RF environments
- Higher efficiency
- Superior heat dissipation
- Excellent thermal performance
- Better electrical performance

The MC1319x and MC1320x families of IEEE 802.15.4 devices use this package. Chapter 2, “QFN Packaging Information” provides;

a) Package dimensions
b) Printed circuit board (PCB) information including copper layer, solder layer, and reflow recommendations
c) Device marking details
d) Tape and Reel information

1.2 71-Contact Land Grid Array (LGA)

The Land Grid Array (LGA) package is a standard flip-chip Ball Grid Array (BGA) shipped with no spheres.

Some benefits of the LGA package over a BGA package include:

- LGA devices can be used for either lead containing or lead-free assemblies depending on the surface mount technology (SMT) assembly solder paste used.
- LGA eliminates the risk that customers receive components with missing or damaged spheres due to shipping or handling.
- LGA devices have a lower mounted height than a BGA. This can allow for more space above the device for a heat sink solution or for small form-factor applications.
- Board-level reliability significantly exceeds customer requirements when the design and process recommendations are followed.

The MC1321x family of IEEE 802.15.4 devices use this package. Chapter 3, “71-Pin LGA Package Information” provides;

a) Package dimensions
b) Printed circuit board (PCB) information including copper layer, solder layer, and reflow recommendations
c) Device marking details
d) Tape and Reel information

1.3 99-Contact Land Grid Array (LGA)

The Land Grid Array (LGA) package is a standard flip-chip Ball Grid Array (BGA) shipped with no spheres.

Some benefits of the LGA package over a BGA package are the same as shown in Section 1.2, “71-Contact Land Grid Array (LGA)”.

The MC1322x family of IEEE 802.15.4 devices use this package. Chapter 4, “99-Pin LGA Packaging Information” provides;

a) Package dimensions
b) Printed circuit board (PCB) information including copper layer, solder layer, and reflow recommendations

1.4 Layout and RF Design Considerations

In addition to the actual package layout and design considerations, the RF component and interconnect is critical to repeatable, best RF performance. Chapter 6, “Layout and RF Design Considerations” addresses these issues giving excellent guidance for early, first design success and easy transition to production. The RF impact of PCB layout, PCB layer stackup, components, signal harmonics, and antennas are discussed.

Freescale also has a number of available RF reference designs that provide an excellent starting point for the majority of customer applications. Most often the user can make minor modifications to a known good RF design and be on the fast track to early RF success.

Chapter 2
QFN Packaging Information

The following sections describe guidelines for a Printed Circuit Board (PCB) footprint and marking for the QFN32 package used for the MC1319x and MC1320x. Included are layouts of the component copper layer, solder mask, and solder paste stencil. These recommendations are guidelines only and may need to be modified depending on the assembly house used and the other components on the board.

A general description for QFN packages can be found in AN1902 at the Freescale web site:

http://www.freescale.com/files/32bit/doc/app_note/AN1902.pdf

2.1 QFN Component Copper Layer

Figure 2-1 shows a recommended component copper layer. This layer is also referred to as the top metal layer and is the layer to which the components are soldered. The footprint for the QFN-32 package consists of 32 IC contact pads and a centered ground pad. The centered ground pad is partitioned into 9 conjoined pads. There should be 0.25 mm via holes through at least four of the center pads connected to the ground plane layers. These are required for RF grounding.

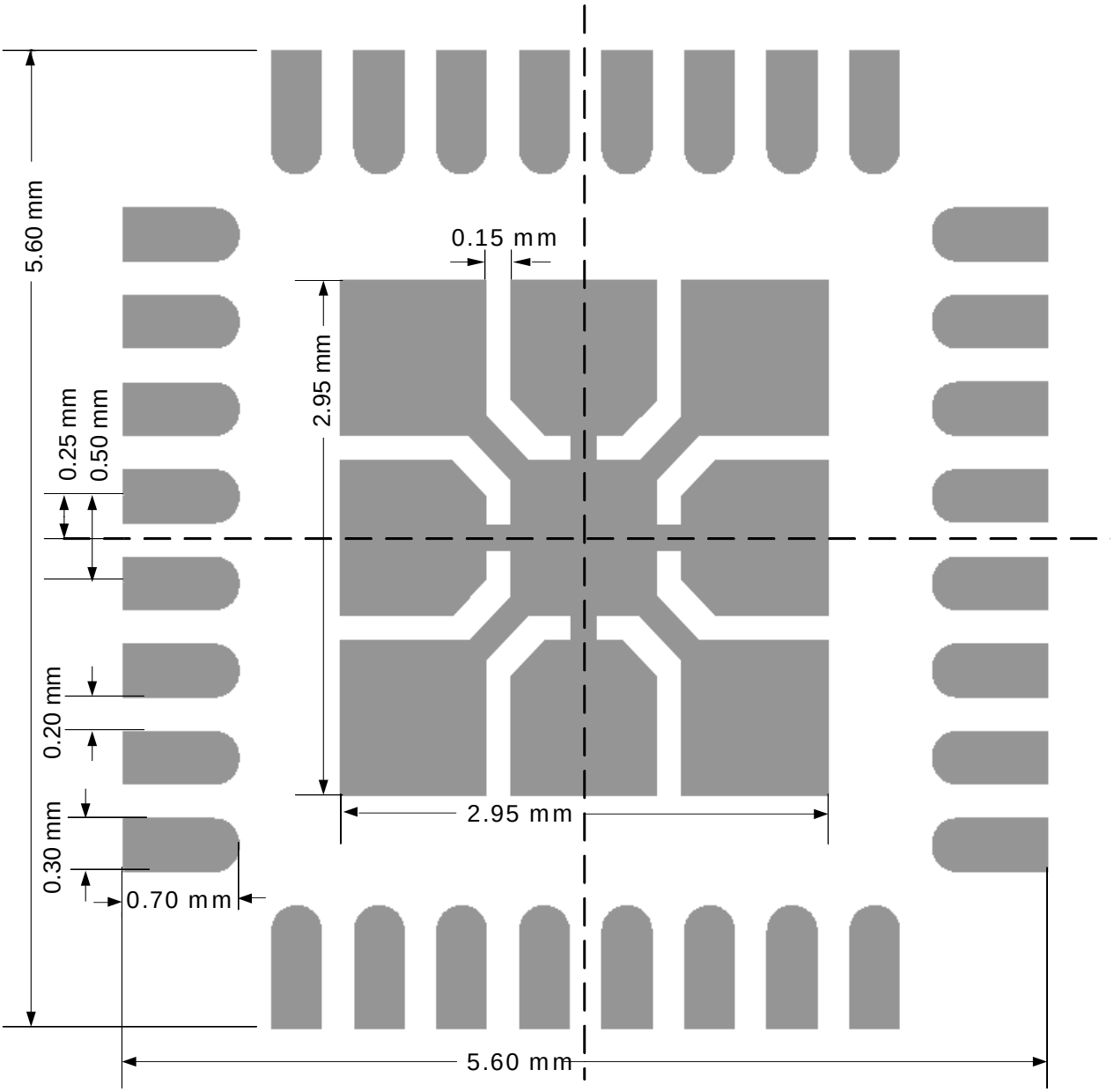


Figure 2-1. QFN Component Copper Layer

2.2 QFN Solder Mask

The solder mask limits the flow of the solder paste during the reflow process. Figure 2-2 shows a recommended solder mask pattern. The pattern represents the openings in the solder mask. The IC contact openings actually touch, so there is no septum between openings. The lines shown are an artifact of the CAD drawing.

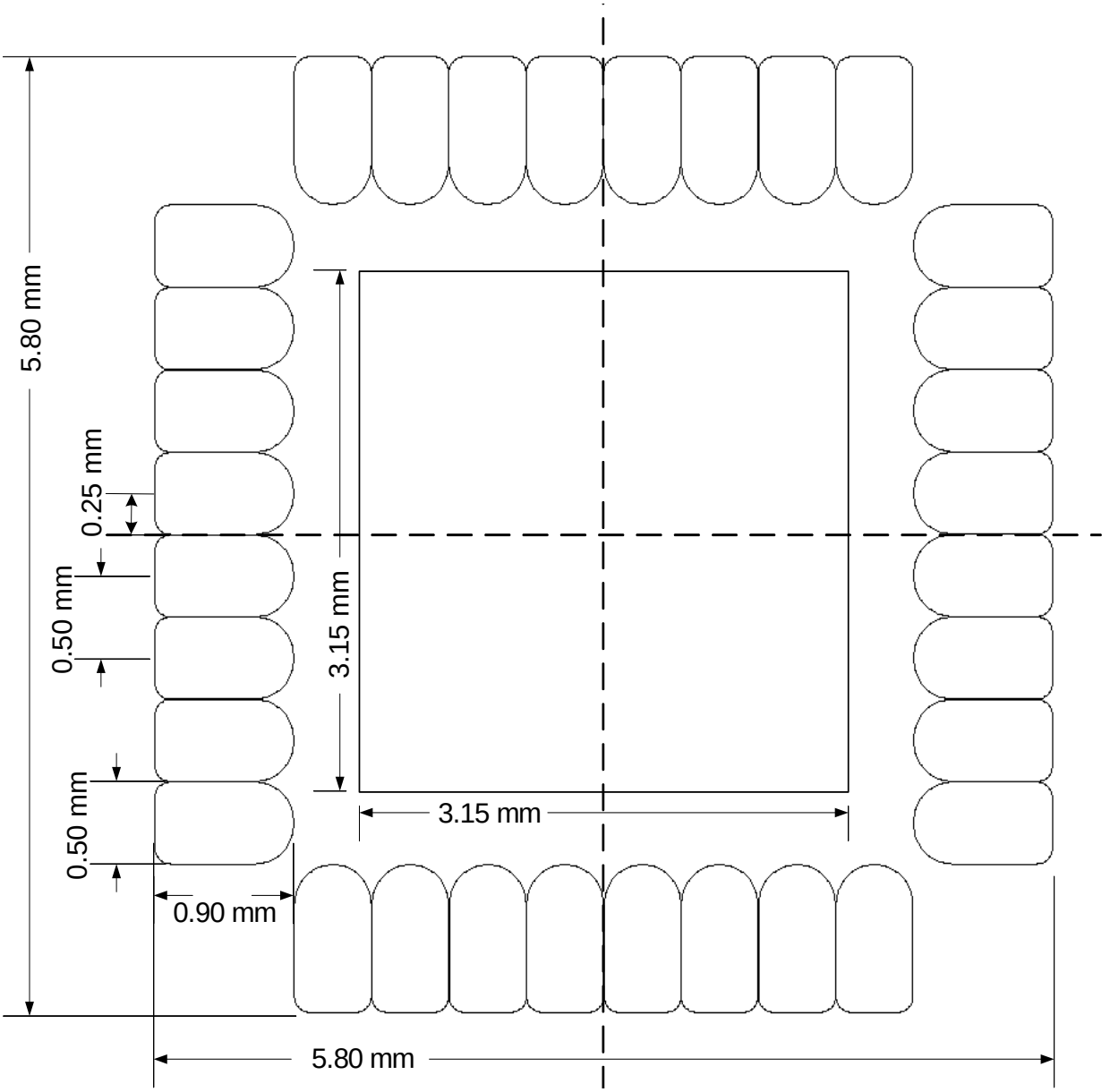


Figure 2-2. QFN Solder Mask Pattern

2.2.1 QFN Solder Paste Stencil

The solder paste stencil controls the pattern and thickness of the solder paste dispensed on the board. Figure 2-3 shows a recommended solder stencil pattern. Stencil thickness should be 0.13 - 0.15 mm. Other patterns and opening sizes can be used if too much solder is being applied. See Section 2.2.2, "QFN Problems with Excess Solder" for more information.

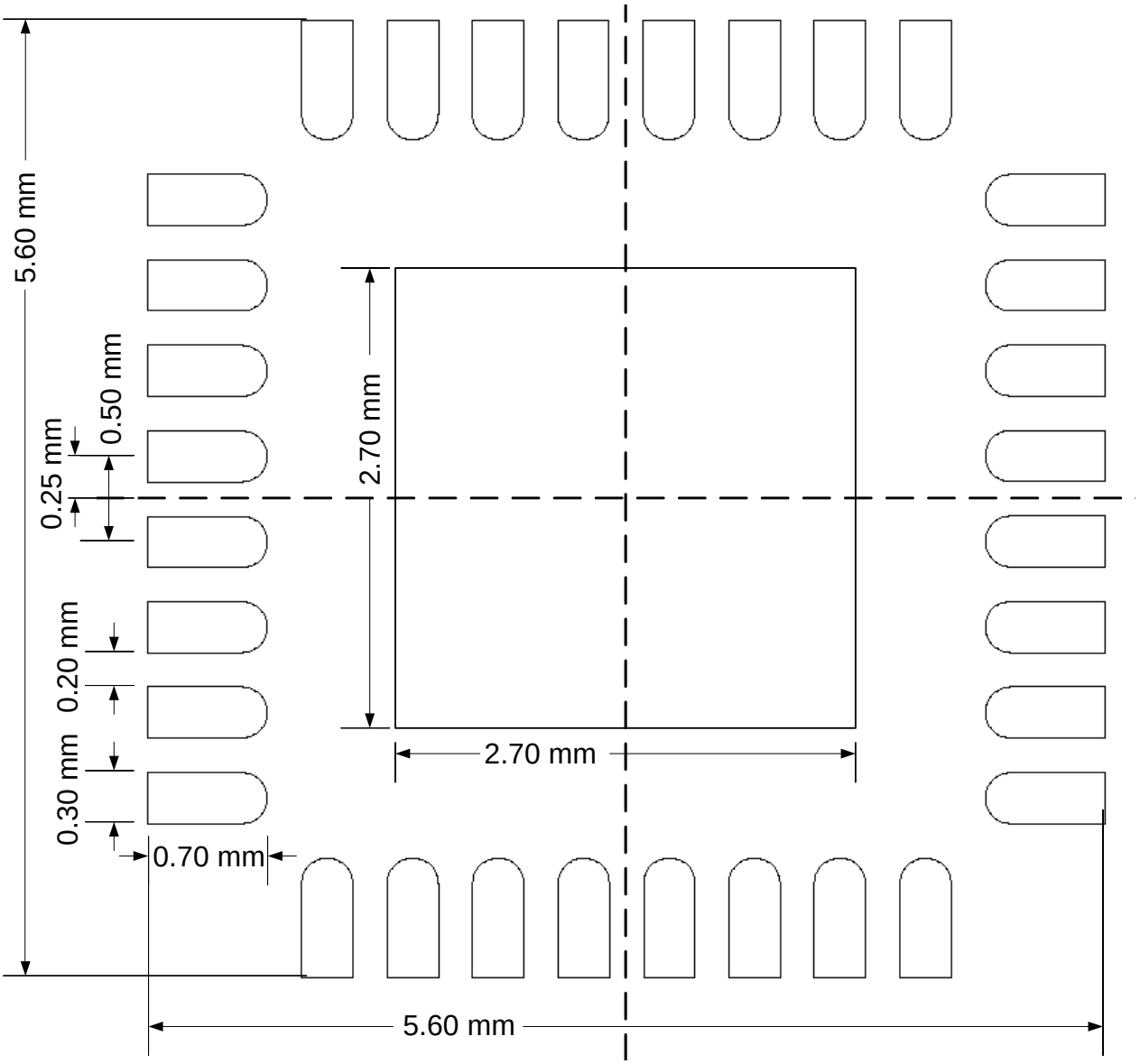


Figure 2-3. QFN Solder Stencil Pattern

2.2.2 QFN Problems with Excess Solder

Excess solder may cause the QFN to “float” or bridge between the package contacts. To use the correct amount of solder paste applied to the PCB, take into consideration the following:

- Stencil thickness
- Other components mounted on the PCB
- Manufacturing equipment
- Assembly house experience

Package floating can be eliminated by reducing the area of solder paste on the centered pad. Figure 2-4 shows alternative solder stencil patterns to reduce the amount of solder paste applied to the centered pad.

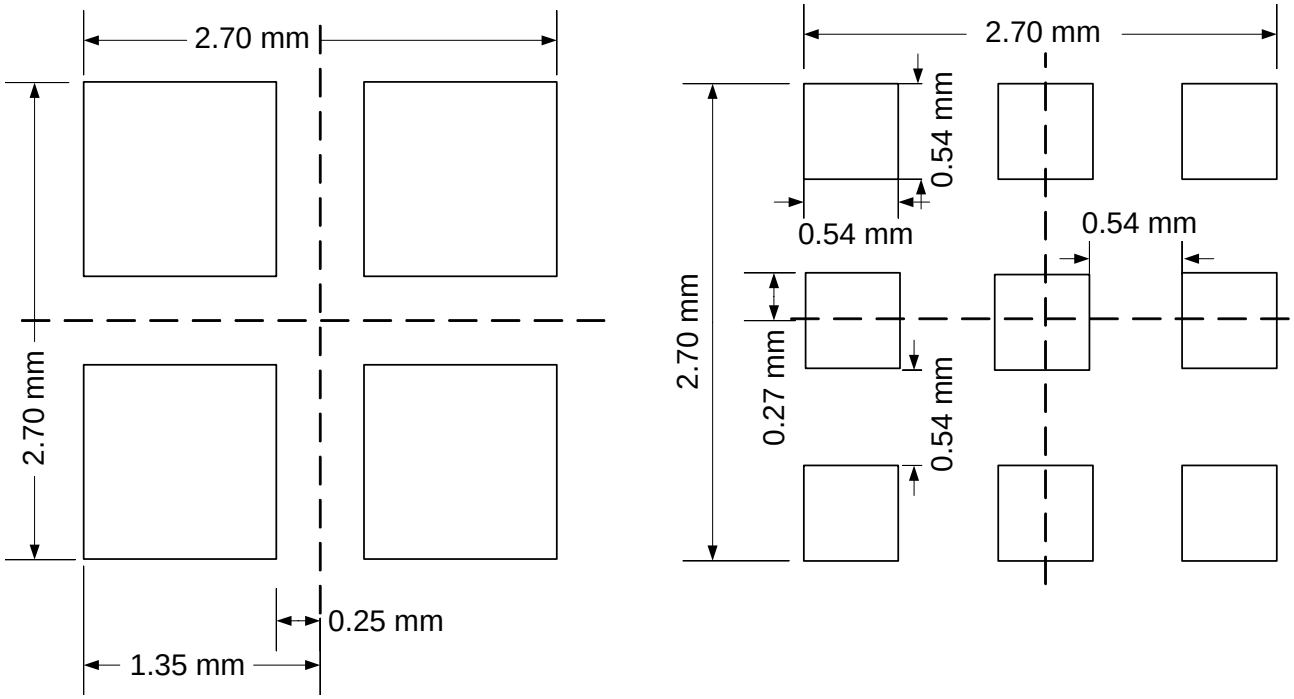


Figure 2-4. QFN Alternative Solder Stencil Patterns

Solder bridging between package contacts can be reduced by adjusting the metal contact pad widths in Figure 2-1 from 0.3 mm to 0.25 mm and the solder mask pad openings from 0.5 mm to 0.4 mm. This allows for a 0.1 mm septum of solder mask between the pads. However, this approach may not be feasible for all board houses and may increase assembly cost.

2.2.3 QFN32 Package Dimensions

Figure 2-5 shows the QFN32 package dimensions. The package information shown in Figure 2-5 is available from the Freescale web site at:

http://www.freescale.com/files/shared/doc/package_info/98ARH99035A.pdf

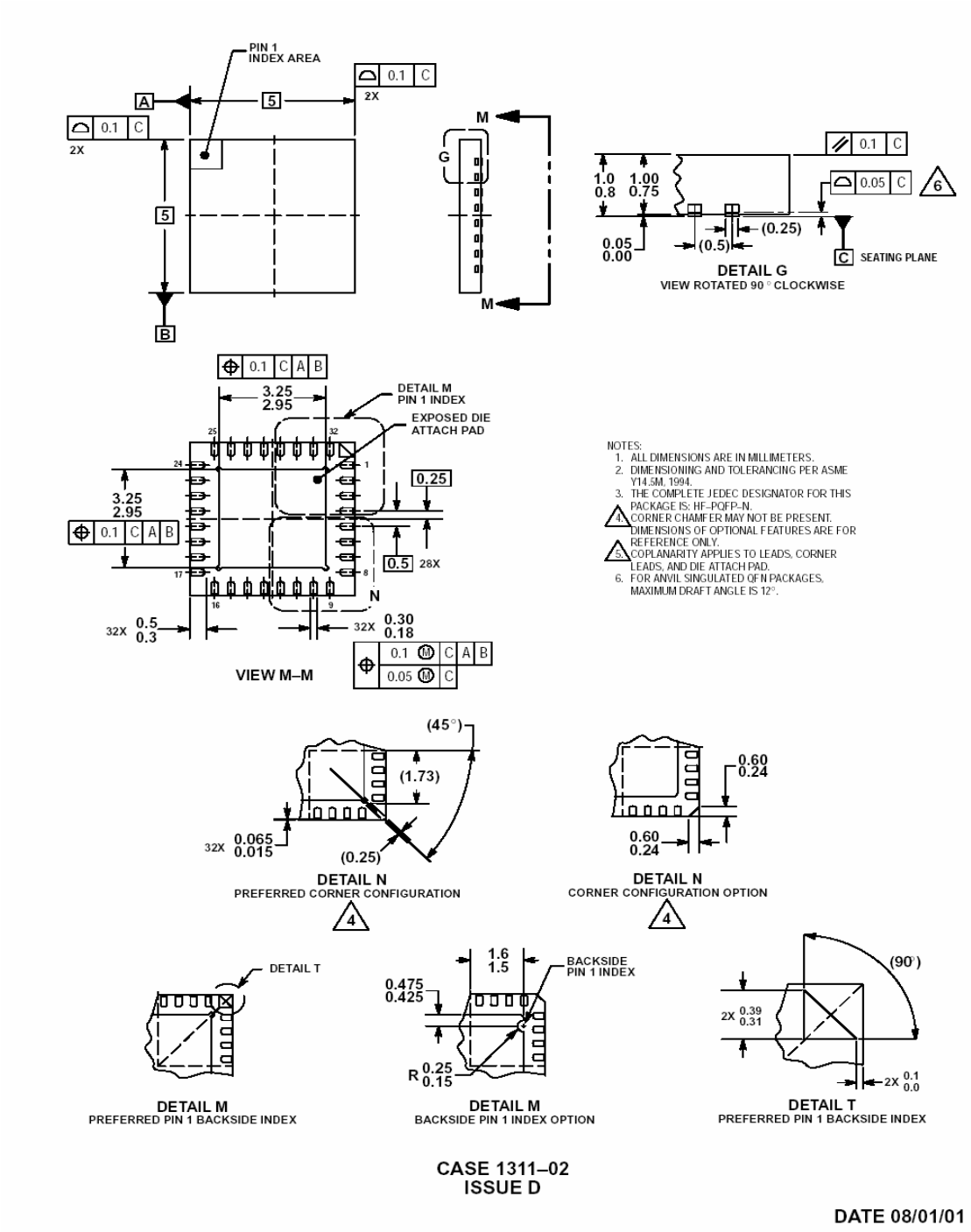


Figure 2-5. QFN Package Dimensions

2.2.4 QFN Device Marking Details

The MC1319x and MC1320x devices are in the QFN-32 plastic package, Case 1311-03.

Figure 2-6 shows an example of QFN-32 device marking for MC1320x devices.

NOTE

Revision information was added to the MC1320x device marking starting with version 1.3.

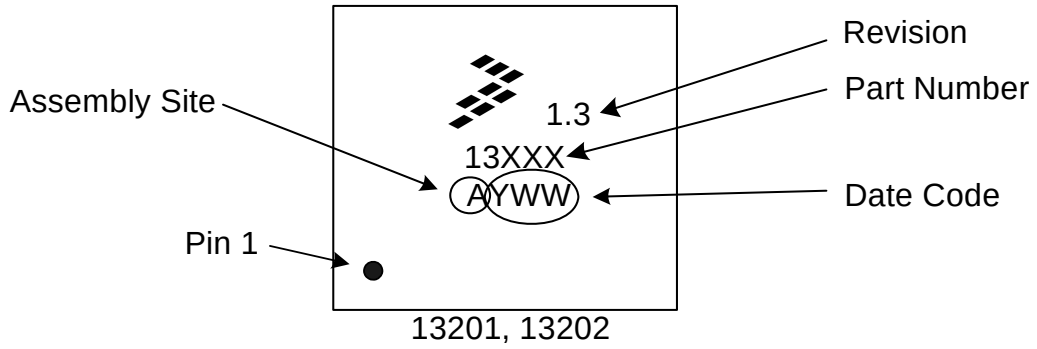


Figure 2-6. Example QFN-32 Device Marking MC13201 and MC13202

Figure 2-7 shows an example of QFN-32 device marking for MC1319x devices.

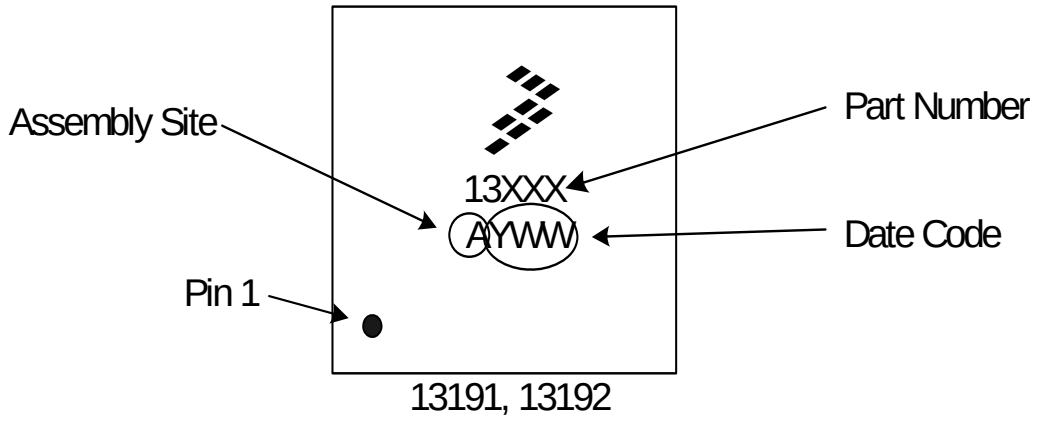


Figure 2-7. Example QFN-32 Device Marking MC13191 and MC13192

2.2.5 QFN Tape and Reel

Tape and Reel packaging is available for the QFN-32 package. Reels are available to support the requirements of both first and second generation pick–and–place equipment. The packaging fully conforms to the latest EIA–481A specification. The antistatic embossed tape provides a secure cavity, sealed with a peel–back cover tape.

Embossed Tape and Reel facilitates automatic pick and place equipment feed requirements. The tape is the shipping container for various products and requires a minimum of handling. The antistatic/conductive tape provides a secure cavity for the product when sealed with the peel.back cover tape.

- Two Reel Sizes Available (7 inch and 13 inch)
- Used for Automatic Pick and Place Feed Systems
- Minimizes Product Handling
- EIA 481, -1, -2
- PQFN 5x5 in 16 mm Tape

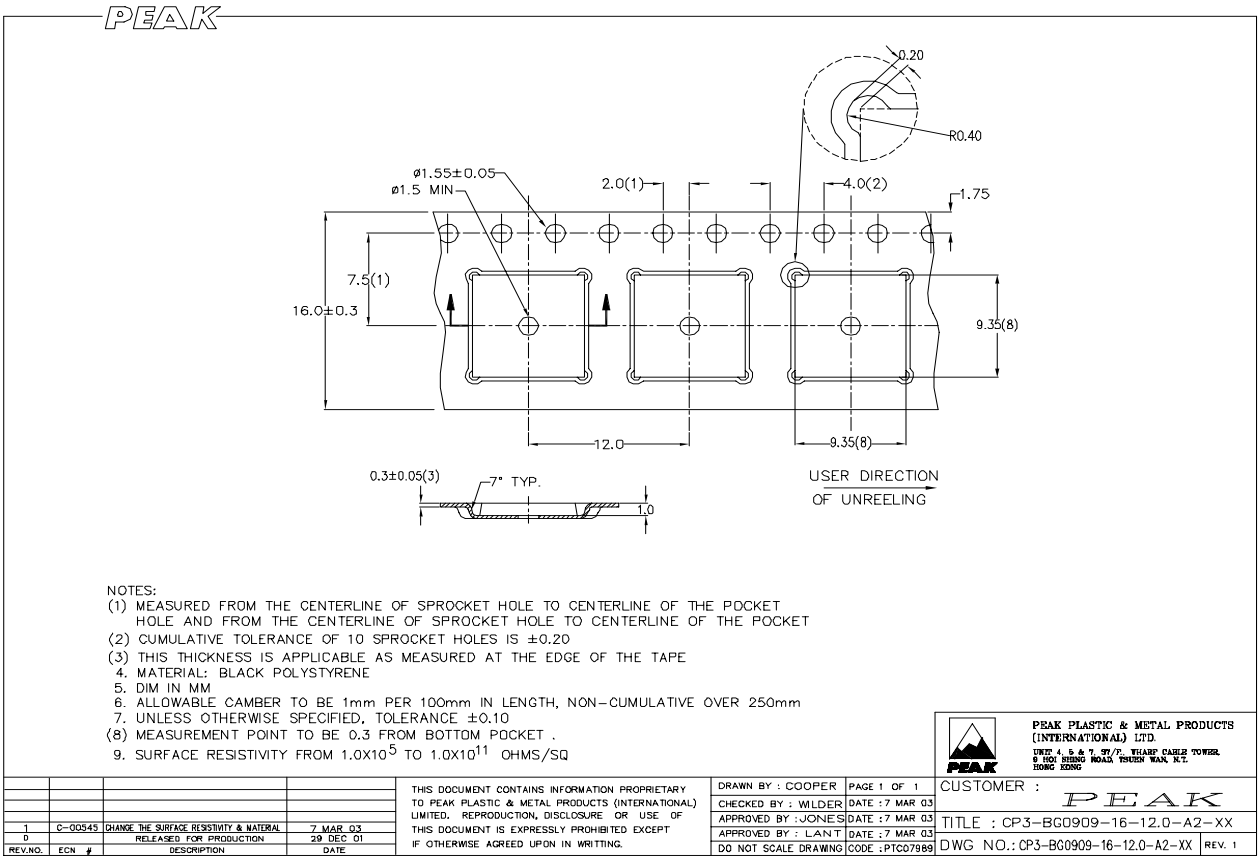


Figure 8. Example QFN-32 Tape and Reel Detailed Mechanical

Chapter 3
71-Pin LGA Package Information

The following sections describe Printed Circuit Board (PCB) footprint guidelines for the MC1321x LGA71 package. Included are layouts of the component copper layer, solder mask, and solder paste stencil. These recommendations are guidelines only and may need to be modified depending on the assembly house used and the other components on the board.

3.1 71-Pin LGA Component Copper Layer

Figure 3-1 shows a recommended component copper layer. This layer is also referred to as the top metal layer and is the layer to which the components are soldered. The footprint for the LGA-71 package consists of 71 IC contact pads and a centered ground pad. The centered ground pad is partitioned into 8 conjoined pads. There are two 0.30 mm via holes per square in the center pads connected to the ground plane layers. These are required for RF grounding and help prevent solder float.

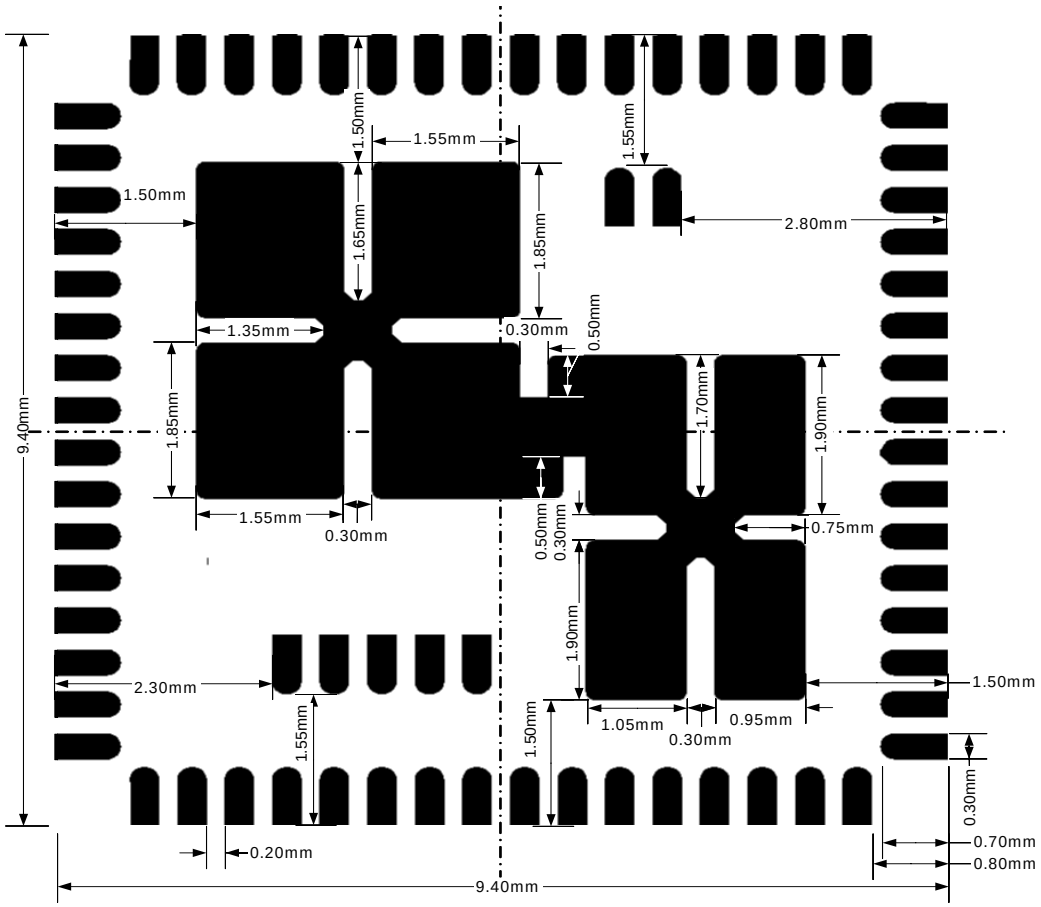


Figure 3-1. LGA Component Copper Layer

3.2 71-Pin LGA Solder Mask

The solder mask limits the flow of the solder paste during the reflow process. Figure 3-2 shows a recommended solder mask pattern. The pattern represents openings in the solder mask. The IC contact openings actually touch, so there is no septum between openings. The lines shown are an artifact of the CAD drawing.

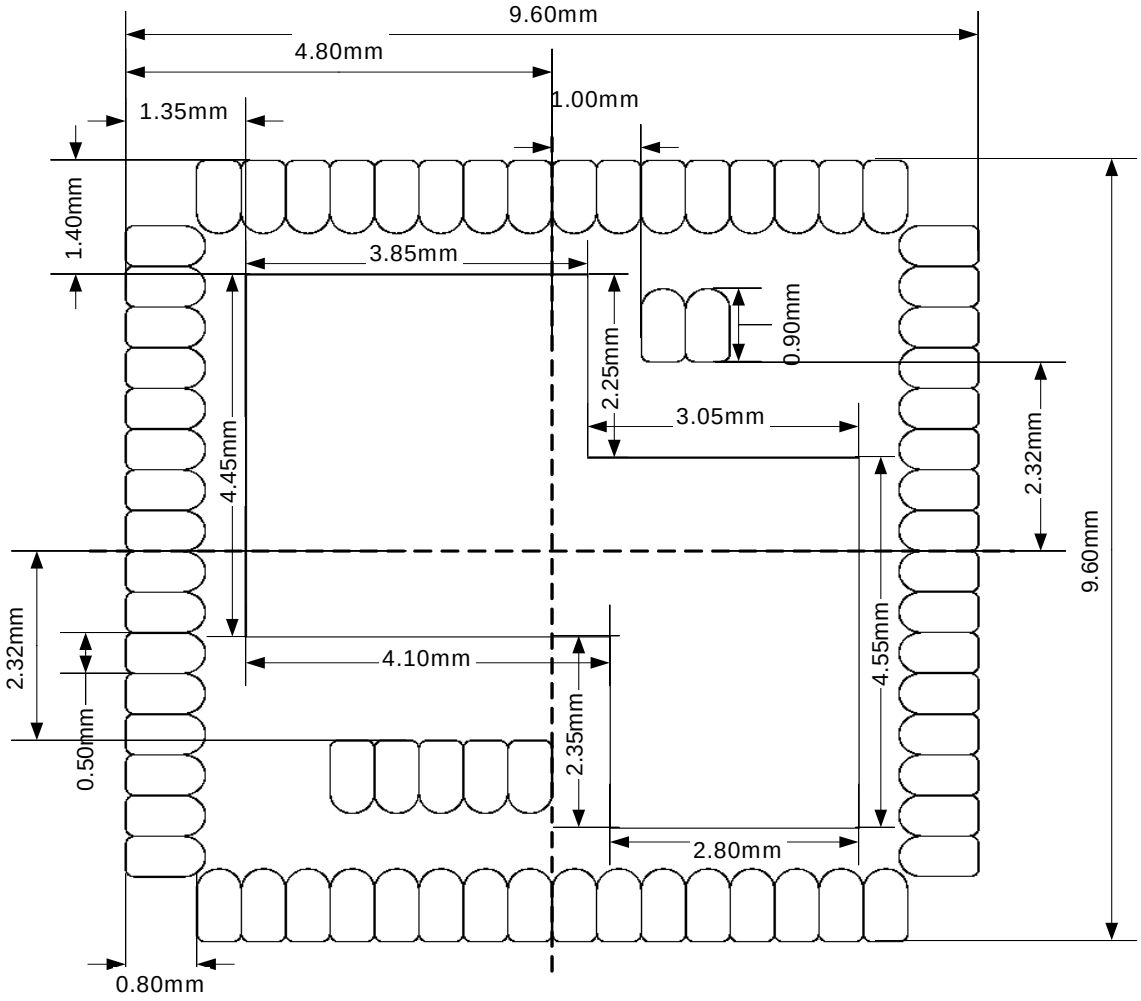


Figure 3-2. 71-Pin LGA Solder Mask Pattern

3.2.1 71-Pin LGA Solder Paste Stencil

The solder paste stencil controls the pattern and thickness of the solder paste dispensed on the board. Figure 3-3 shows a recommended solder stencil pattern. Stencil thickness should be approximately 0.1 mm.

Other patterns and opening sizes can be used if too much solder is being applied. See Section 2.2.2, “QFN Problems with Excess Solder” for more information.

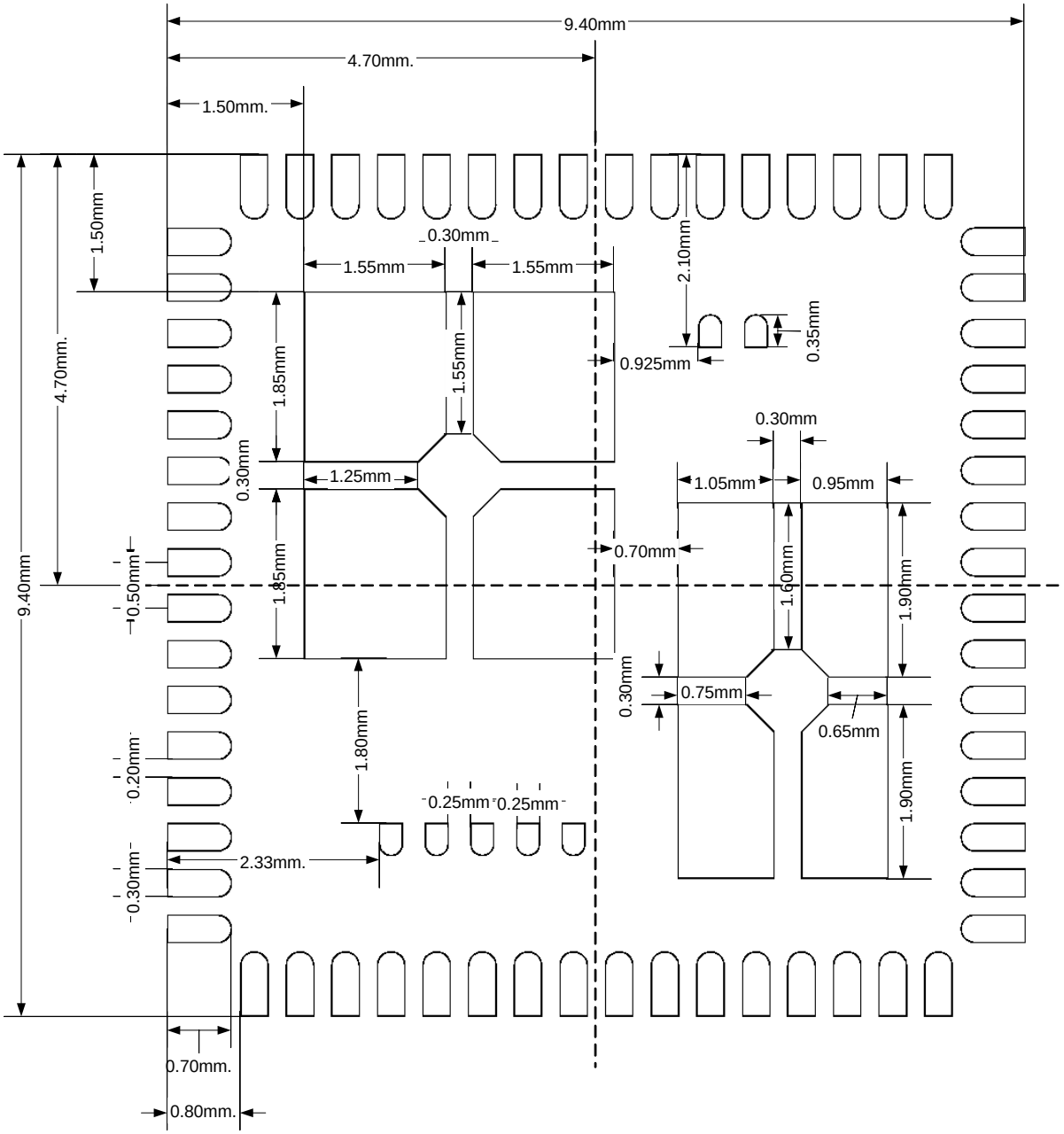


Figure 3-3. 71-Pin LGA Solder Stencil Pattern

3.2.2 LGA Problems with Excess Solder

Excess solder may cause the LGA to “float” or bridge between the package contacts. To use the correct amount of solder paste applied to the PCB, take into consideration the following:

- Stencil thickness
- Other components mounted on the PCB
- Manufacturing equipment
- Assembly house experience

3.2.3 LGA-71 Package Dimensions

Figure 3-4 shows the LGA71 package dimensions.

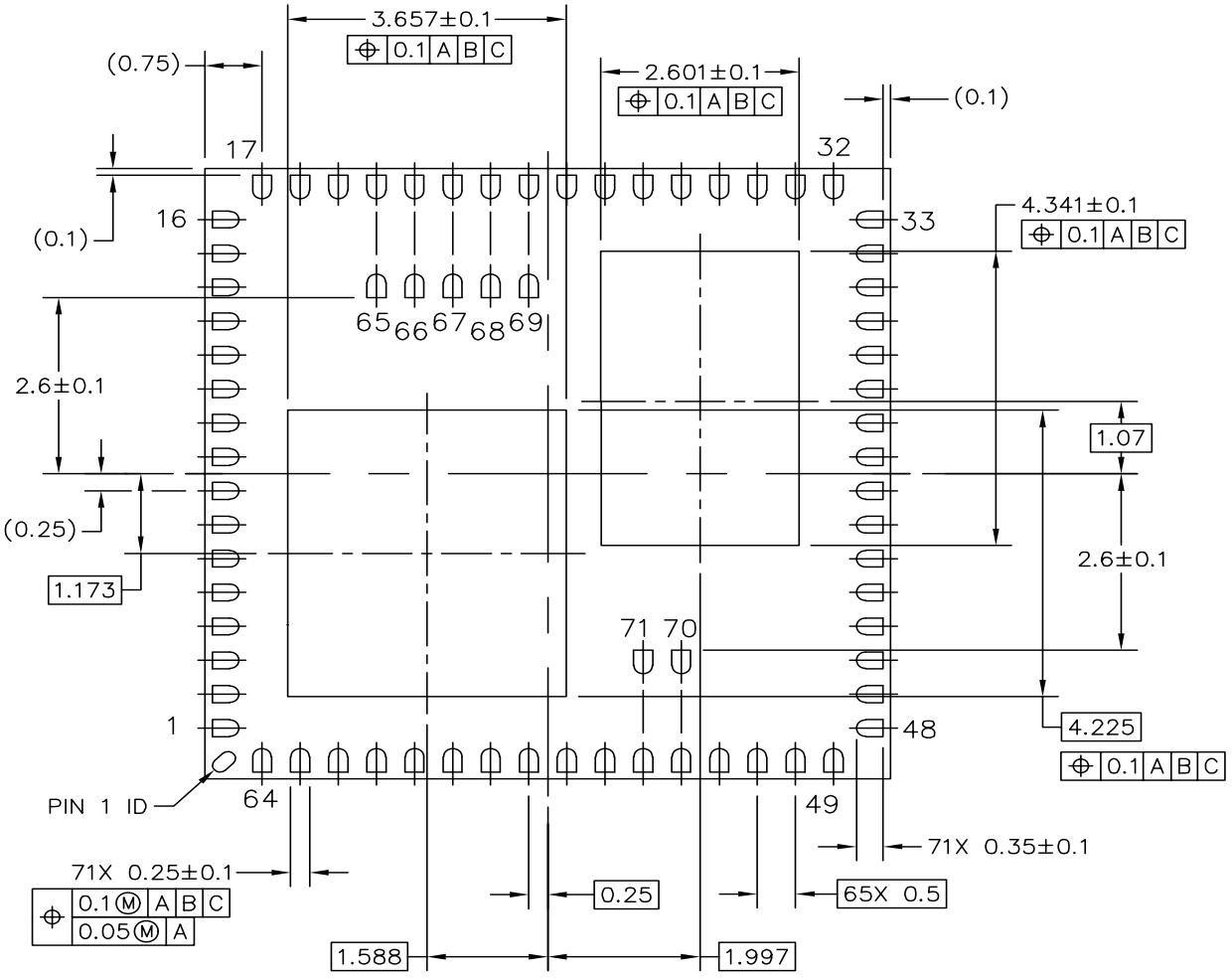


Figure 3-4. LGA Package Dimensions

3.2.4 71-Pin LGA Device Marking Details

The MC1321x devices are in the 71-pin LGA (9x9mm), Case 1664-01. The following figures show device marking examples for the LGA device. Figure 3-5 shows the marking for silicon revision 1.1 and newer.

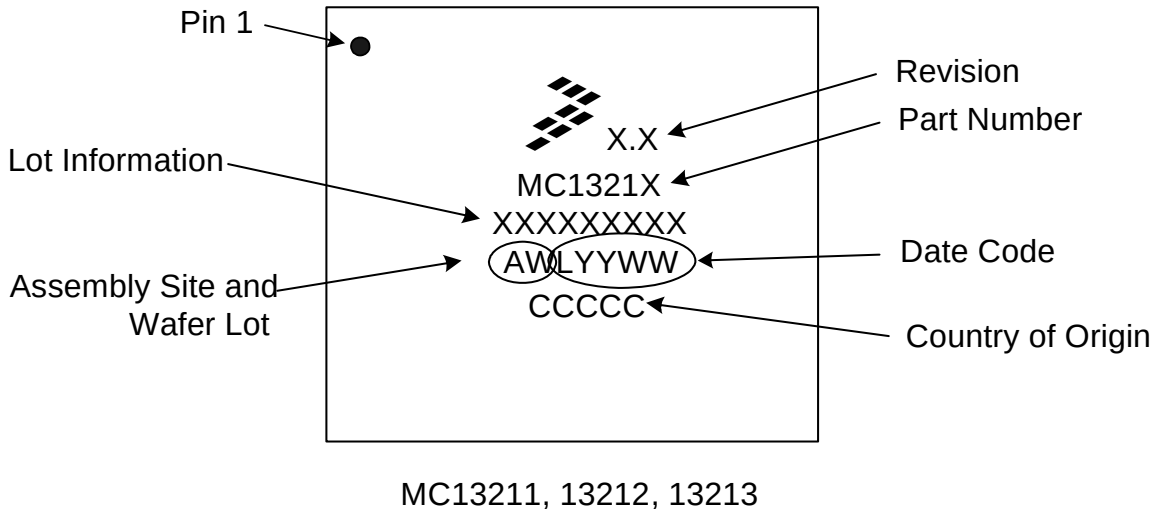


Figure 3-5. Example LGA-71 Device Marking Revision 1.1 and Newer

Figure 3-6 shows the marking for silicon revisions for revision 1.0 and older.

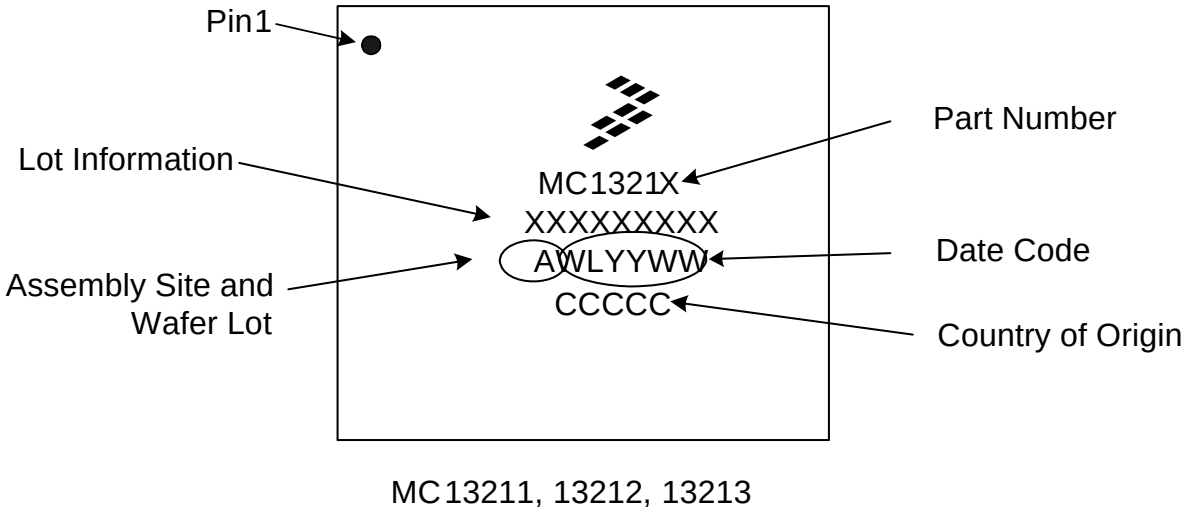


Figure 3-6. LGA-71 Device Marking Revision 1.0 and Older

3.2.5 71-Pin LGA Tape and Reel

Tape and Reel packaging is available for the LGA-71 package. Reels are available to support the requirements of both first and second generation pick–and–place equipment. The packaging fully conforms to the latest EIA–481A specification. The antistatic embossed tape provides a secure cavity, sealed with a peel–back cover tape.

Embossed Tape and Reel facilitates automatic pick and place equipment feed requirements. The tape is the shipping container for various products and requires a minimum of handling. The antistatic/conductive tape provides a secure cavity for the product when sealed with the peel.back cover tape.

- Two Reel Sizes Available (7 inch and 13 inch)
- Used for Automatic Pick and Place Feed Systems
- Minimizes Product Handling
- EIA 481, -1, -2

Figure 3-7 shows an example tape and reel mechanical drawing.

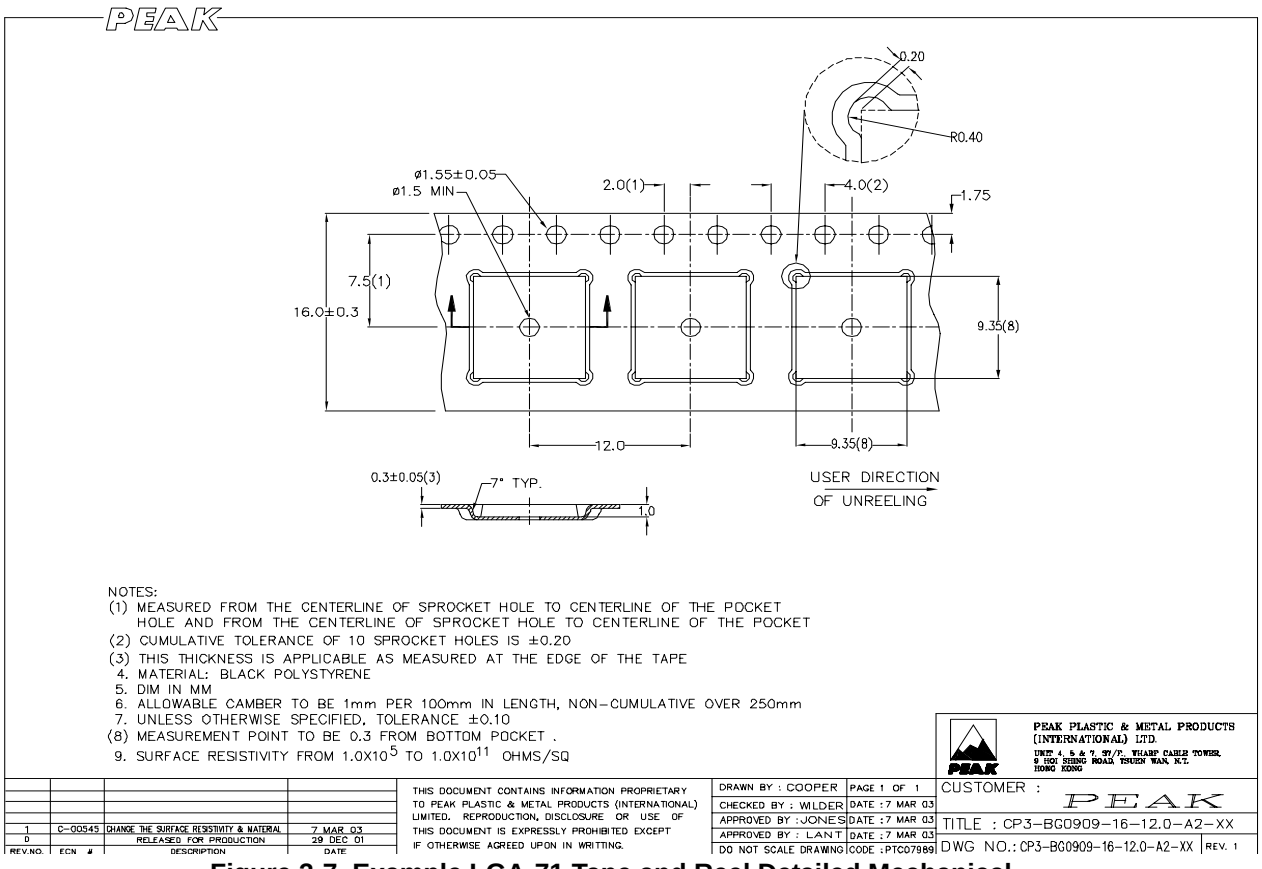


Figure 3-7. Example LGA-71 Tape and Reel Detailed Mechanical

Chapter 4
99-Pin LGA Packaging Information

The following sections describe guidelines for a Printed Circuit Board (PCB) footprint and marking for the 99-pin LGA package which the MC1322x uses and is designated Case 1901-01(non-JEDEC). Included are layouts of the component copper layer, solder mask, and solder paste stencil. These recommendations are guidelines only and may need to be modified depending on the assembly house used and the other components on the board.

NOTE

All dimensions as shown or referenced in this chapter are in millimeters.

4.1 99-Pin LGA Component Copper Layer

The MC1322x pad usage is somewhat unusual and requires some consideration.

4.1.1 Bottom Pad Definitions

Figure 4-1 shows the bottom pad locations for the 99-pin LGA. Observe the following:

- The footprint for the LGA package consists of 64 peripheral contact pads (0.35x0.25 mm) at the outside boundary of the package and 81 square pads (0.4x0.4 mm) located within the peripheral pad ring.
- The total pad count is 145 of which 99 are actual electrical contacts and the remaining 46 (all square pads) are mechanical only and have no contact, i.e., they are electrically isolated. These additional mechanical pads are added for greater attach strength for applications requiring higher g-forces.
- The inner square pad array is on a 0.8x0.8 mm grid.
- The peripheral pads are spaced 0.5 mm between center lines

4.1.2 MC1322x Bottom Pad Usage

The inner square pad usage on the MC1322x requires additional discussion. Figure 4-1 shows just the inner pads for the MC1322x. Observe the following

NOTE

This drawing is TOP VIEW and not to scale.

- The MC1322x substrate GROUND pads are limited to Pads 75-79, 84-88, 93-97, 104-106, and 115.
- Active signal area - GPIO / Debug Port pins are limited to PAds 102-103, 111-114, 120-124 and 129-133.
- All remaining pads are fully electrically isolated and are No Connect (NC) on the MC1322x. These are included only for mechanical strength

In Figure 4-1 the individual usage areas are outlined.

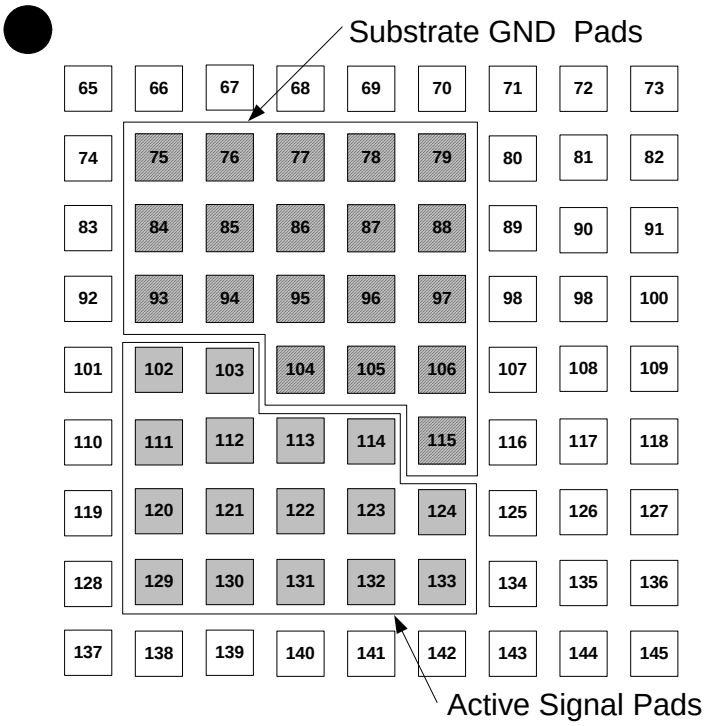


Figure 4-1. MC1322x Bottom Pad Usage

4.1.3 Recommended Copper Layout

The recommended component copper layer is shown in Figure 4-2. A complete layout is not shown, but a representative corner area of the layout is given.

- The copper for the inner pad array consists of 0.5x0.5 mm squares that are located on the same 0.8 x 0.8 mm grid as the package pads. The copper pads are larger and provide an extension of the package pad dimension of 0.05 mm in each direction.
- The copper peripheral pad width is increased from 0.25 mm (on the package) to 0.3 mm. The copper peripheral pad length is increased from 0.35 mm (on the package) to 0.6 mm.

NOTE

The extra length of the peripheral pad is extended toward the outside of the package, not centered about the package pad dimension. In Figure 4-2, the 1.1 mm distance from the inner edge of the peripheral pad to the center line of the inner pad array is the same dimension as the inner edge of the package peripheral pad to the center line of the array. The extra length of the copper pad allows for excess solder to move toward the outside of the package and for easier visual inspection.

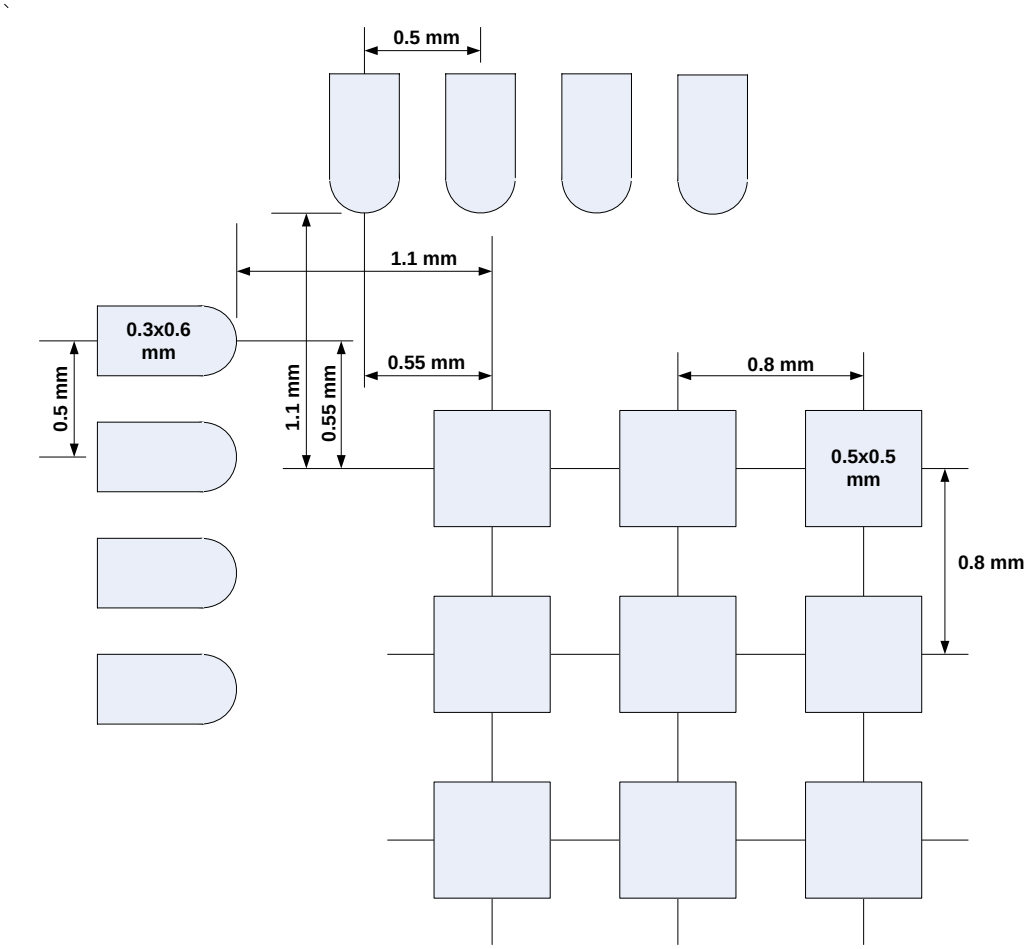


Figure 4-2. 99-Pin LGA Component Copper Layer

- Via use for inner pads - Because of the pad size and their pitch, particular attention should be paid to via use.
  - — It is recommended to use a 0.15mm via located in the center of the pad.
  - — Standard recommended industry practice is to use filled vias although this does add additional board cost.
  - — It is not required that vias be present in all ground pads; an alternating pattern is sufficient. Component copper layer pads without vias can be simply connected to an adjacent ground pad.

NOTE

If vias are used in adjacent pads, the user is cautioned about a potential tools problem. Some CAD tools by default provide a contact pad (on the non-component copper layer) of a diameter that may infringe on the adjacent via and cause potential shorting problems.

  - — The use of adjacent pads tied together, one with a via and one without has been used in some layouts to eliminate the use and cost of filled vias. The concept can be used in the ground substrate area and with some of the pads in the active signal area.

NOTE

The use of filled vias certainly adds additional cost to the pcb. Although discussed here, the ultimate use or non-use of filled vias is strictly the user’s responsibility and should be determined in co-ordination with the user’s board manufacturer.

4.2 99-Pin LGA Solder Mask

The solder mask limits the flow of the solder paste during the reflow process. Figure 4-3 shows a recommended solder mask pattern where the pattern represents openings in the solder mask.

- For the inner pads, the solder mask opening is 0.6x0.6 mm (centered on the 0.5x0.5 mm copper pad). One metal pad is shown for reference.
- The peripheral pad solder mask size is increased to 0.5x0.8 mm. The peripheral pad contact openings actually touch, so there is no septum between openings. The lines shown are an artifact of the CAD drawing. One metal pad is shown for reference.

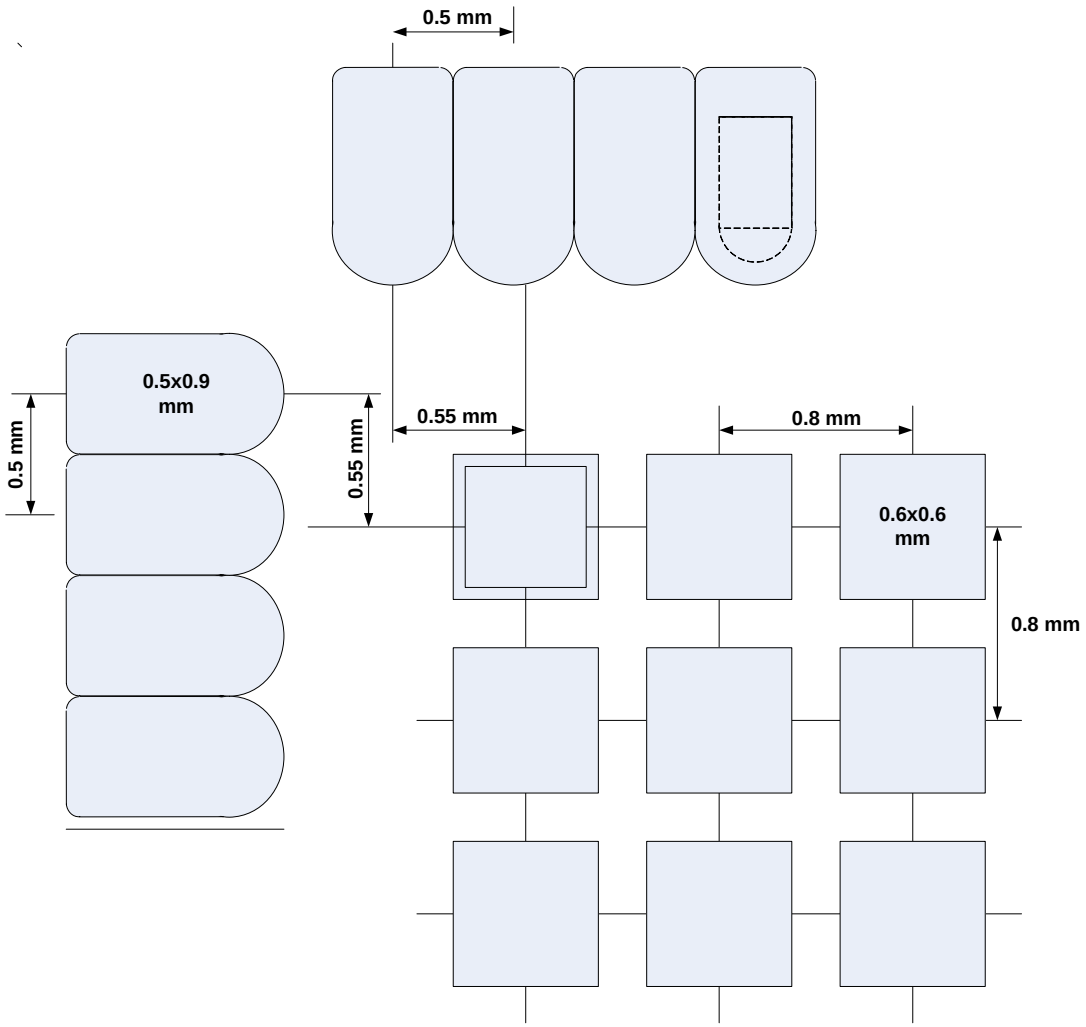


Figure 4-3. 99-Pin LGA Solder Mask Pattern

4.3 99-Pin LGA Solder Paste Stencil

The solder paste stencil controls the pattern and thickness of the solder paste dispensed on the board. Figure 4-4 shows a recommended solder stencil pattern. A copper metal pattern each for a peripheral pad and an inner pad are shown for reference.

- Recommended stencil thickness is 5 mils (0.127 mm).
- Manufacturing variances from different venders may require some modification of stencil thickness
- The peripheral pads have a stencil opening of 10x18 mil (0.254x0.457 mm)
- Observe location of peripheral pad stencil opening with respect to metal
- The inner square pads have a stencil opening of 17x17 mil (0.43x0.43 mm)
- Other patterns and opening sizes can be used if too much solder is being applied. See Section 4.5, “99-Pin LGA Issues with Solder Reflow” for more information.

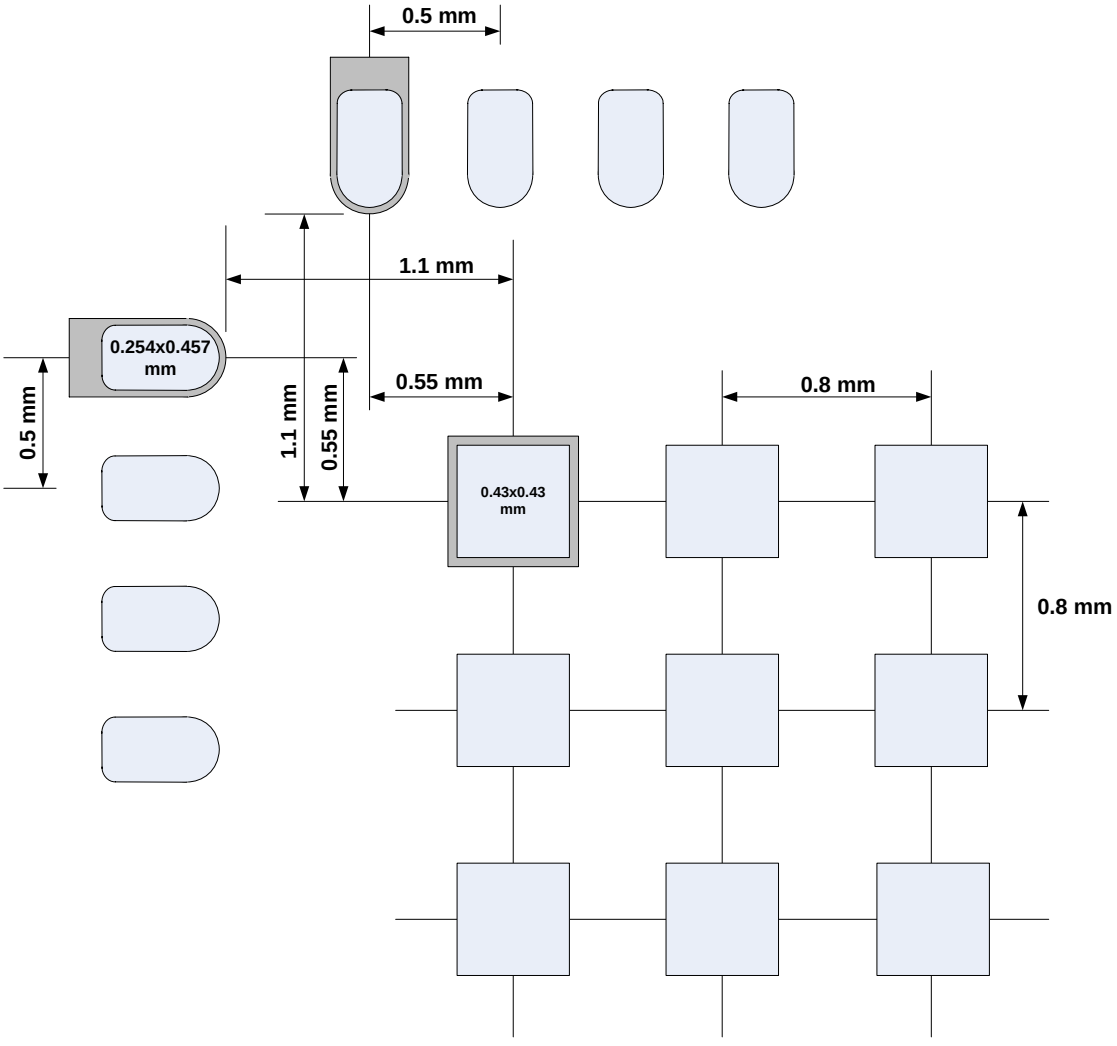


Figure 4-4. 99-Pin LGA Solder Stencil Pattern

4.4 99-Pin LGA Peripheral Pad Summary Reference

For sake of convenience, a peripheral pad geometry stackup is shown in Figure 4-5.

- The largest, dark gray area is the solder mask
- The next inner area (light gray) is the copper
- The inner most area (white) is the solder stencil.

Additionally, layer dimensions are summarized in Table 4-1.

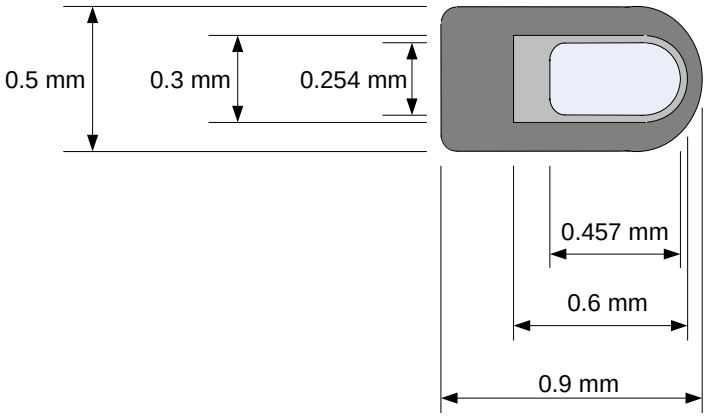


Figure 4-5. 99-Pin LGA Peripheral Pad Overlay Reference

Table 4-1. Peripheral Pad Layer Dimensions

Layer	Width		Length (shaped)	
	Millimeters	Mils	Millimeters	Mils
Copper	0.3 mm	11.8 mils	0.6 mm	23.6 mils
Solder Mask	0.5 mm	19.6 mils	0.9 mm	35.3 mils
Solder Stencil	0.254 mm	10 mils	0.457 mm	18 mils

4.5 99-Pin LGA Issues with Solder Reflow

Problems can occur with solder reflow with use of the LGA package. A number of items can impact the quality of the solder assembly causing solder starvation, excess solder, or poor contact. These include:

- The amount of solder applied to the board
  - — Stencil thickness
  - — Stencil openings
- Other components mounted on the PCB (surface mount and/or through-hole)
- Manufacturing equipment
- Assembly house experience
- Reflow temperatures

Freescale provides reference design and layout information that follows the guidelines in this document, and it is strongly recommended that the user start with the provided material.

4.5.1 99-Pin LGA Device Marking Details

The MC1322x devices are in the 99-pin LGA Case 1901-01(non-JEDEC). shows a device marking example for the LGA device.

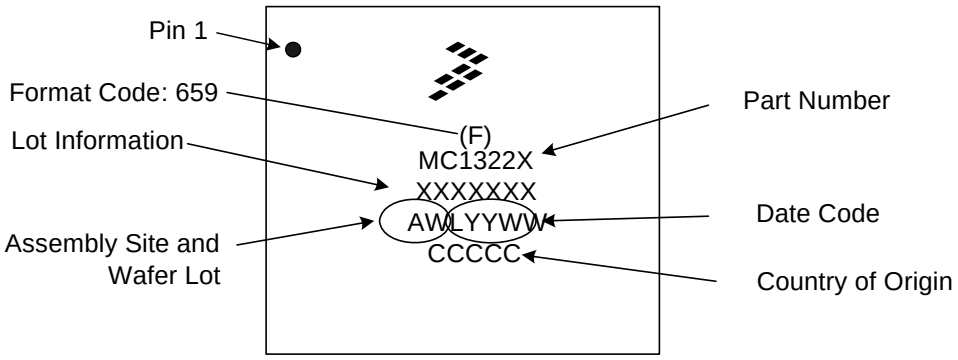


Figure 4-6. Example LGA-99 Device Marking

4.5.2 99-Pin LGA Tape and Reel

Tape and Reel packaging is available for the LGA-99 package. Reels are available to support the requirements of both first and second generation pick–and–place equipment. The packaging fully conforms to the latest EIA–481A specification. The antistatic embossed tape provides a secure cavity, sealed with a peel–back cover tape.

Embossed Tape and Reel facilitates automatic pick and place equipment feed requirements. The tape is the shipping container for various products and requires a minimum of handling. The antistatic/conductive tape provides a secure cavity for the product when sealed with the peel.back cover tape.

- Two Reel Sizes Available (7 inch and 13 inch)
- Used for Automatic Pick and Place Feed Systems
- Minimizes Product Handling
- EIA 481, -1, -2

Figure 4-7 shows an example tape and reel mechanical drawing.

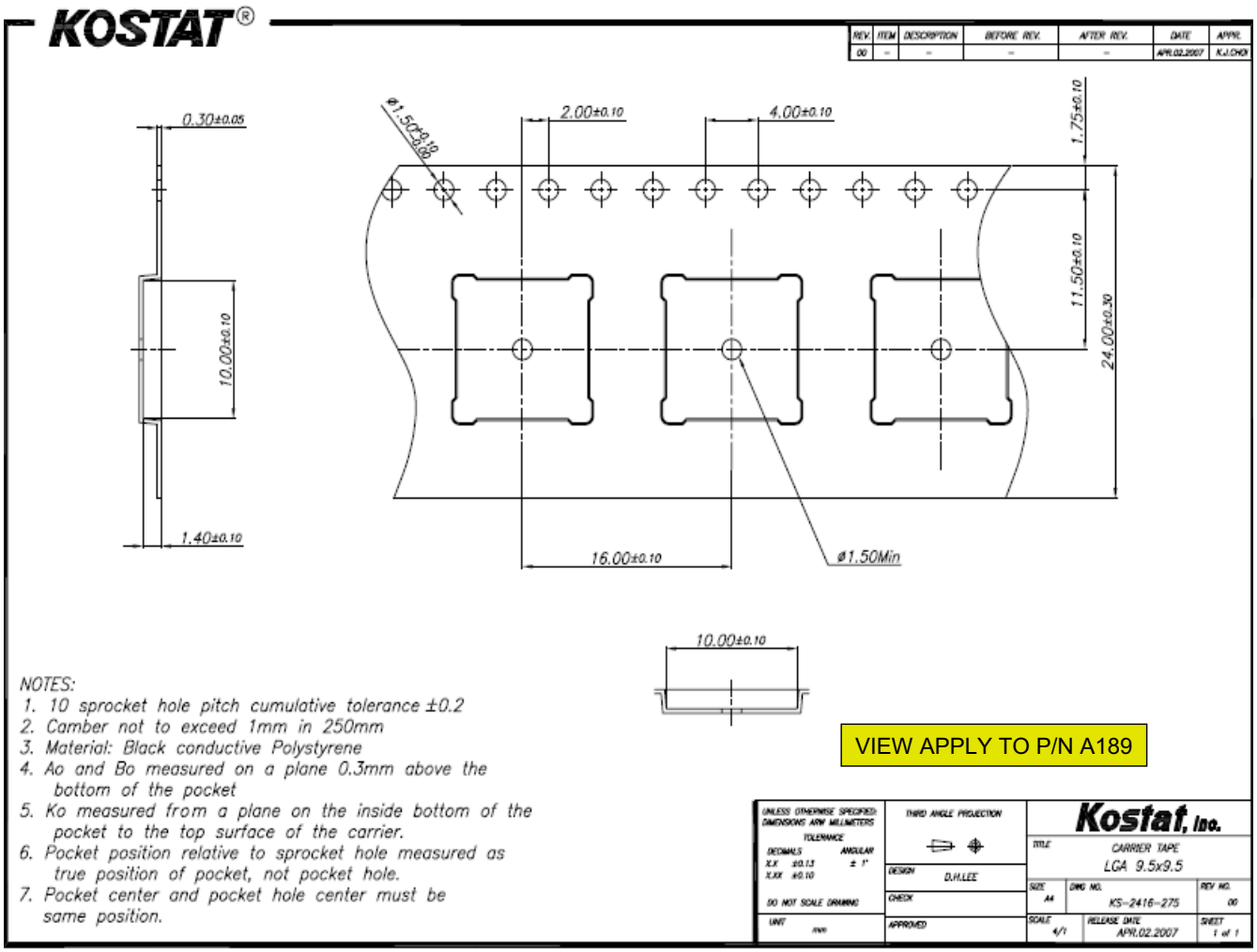


Figure 4-7. Example 99 Pin LGA Tape and Reel Detailed Mechanical

Chapter 5
48-Pin LGA Package Information

The following sections describe Printed Circuit Board (PCB) footprint guidelines for the MC1323x LGA48 package. Included are layouts of the component copper layer, solder mask, and solder paste stencil. These recommendations are guidelines only and may need to be modified depending on the assembly house used and the other components on the board.

5.1 48-Pin LGA Component Copper Layer

Figure 5-1 shows a recommended component copper layer. This layer is also referred to as the top metal layer and is the layer to which the components are soldered. The footprint for the LGA-48 package consists of 48 IC contact pads and a centered ground pad. The centered larger ground pad is partitioned into 9 smaller conjoined pads. There are two 0.30 mm via holes per square in the center pads connected to the ground plane layers. These are required for RF grounding and help prevent solder float.

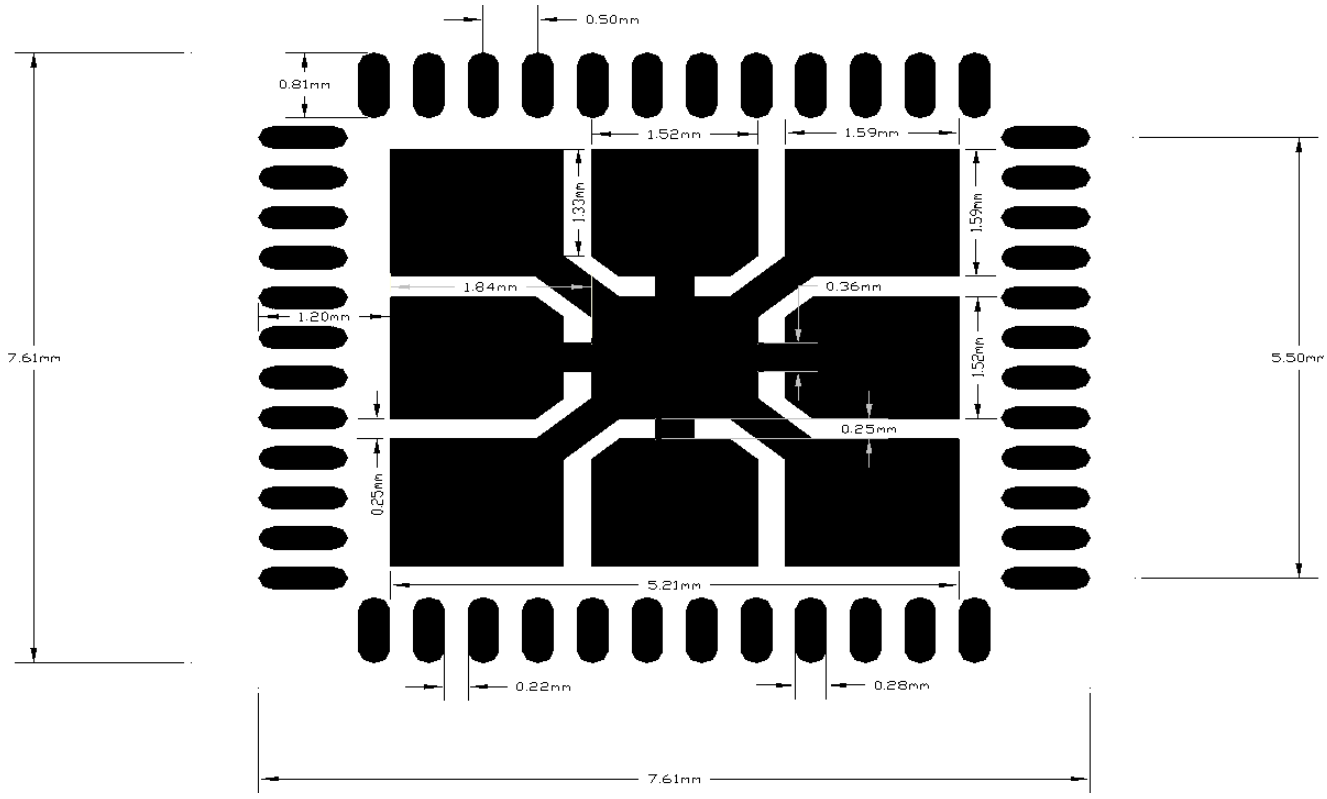


Figure 5-1. LGA Component Copper Layer

5.2 48-Pin LGA Solder Mask

The solder mask limits the flow of the solder paste during the reflow process. Figure 5-2 shows a recommended solder mask pattern. The pattern represents openings in the solder mask.

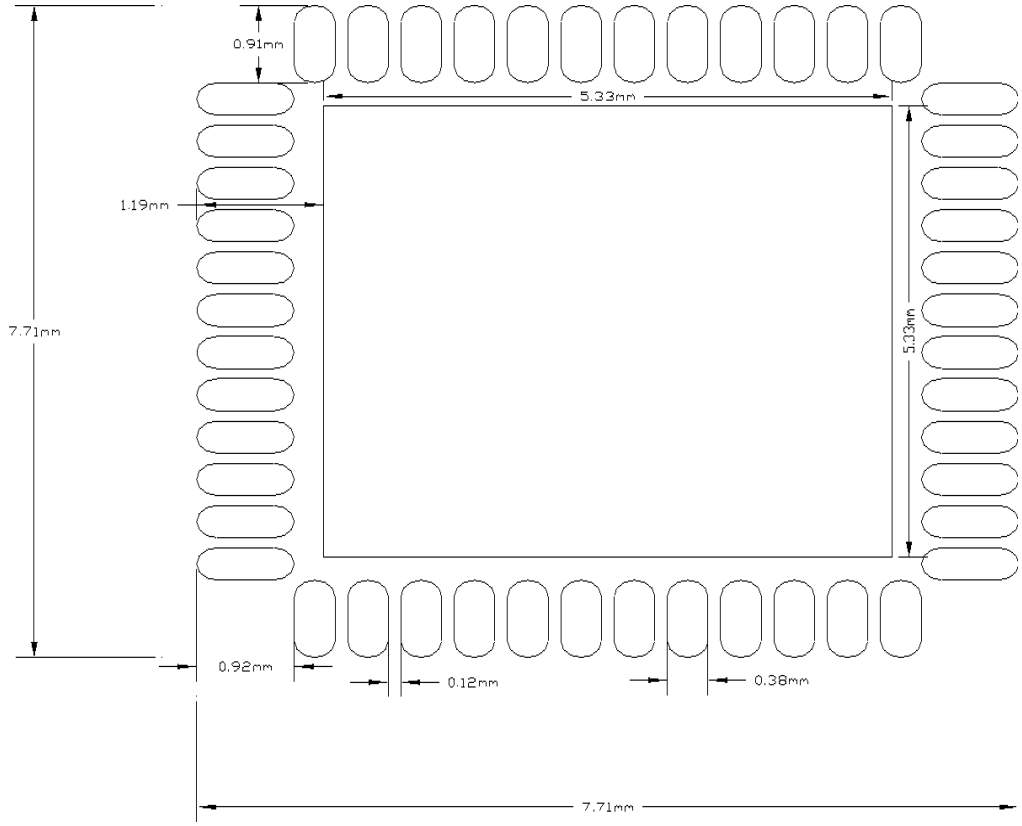


Figure 5-2. 48-Pin LGA Solder Mask Pattern

5.2.1 48-Pin LGA Solder Paste Stencil

The solder paste stencil controls the pattern and thickness of the solder paste dispensed on the board. Figure 5-3 shows a recommended solder stencil pattern. Stencil thickness should be approximately 0.1 mm.

Other patterns and opening sizes can be used if too much solder is being applied. See Section 5.2.2, “LGA Problems with Excess Solder” for more information.

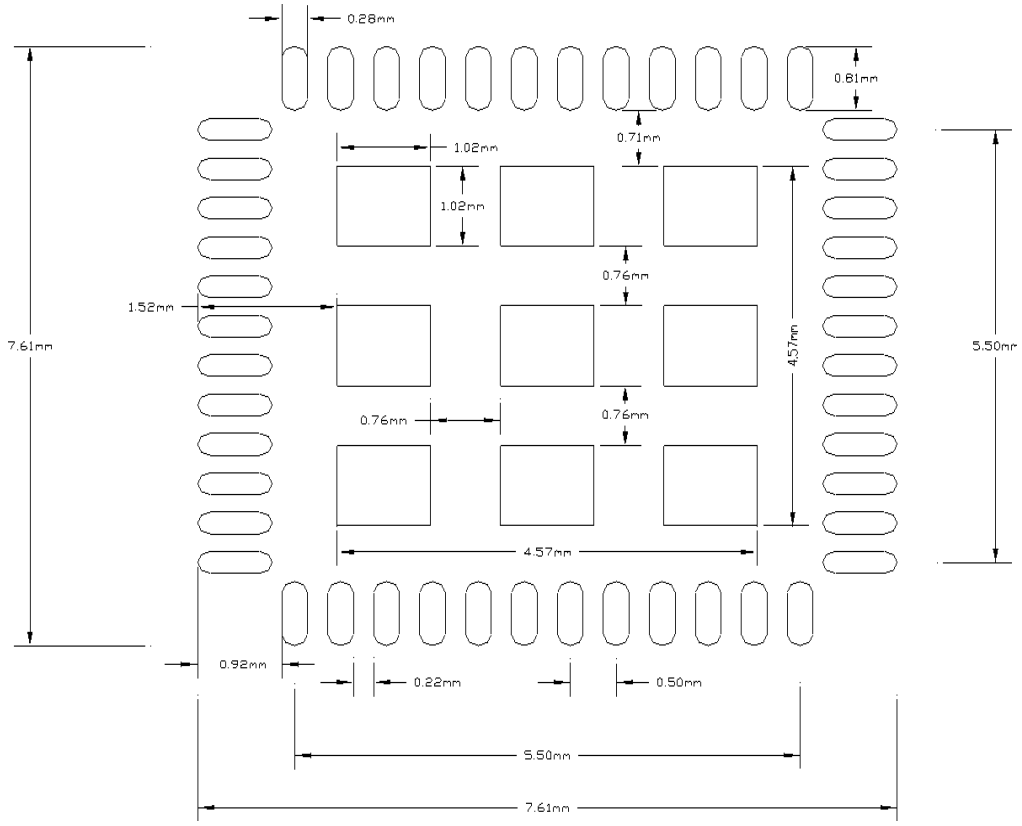


Figure 5-3. 48-Pin LGA Solder Stencil Pattern

5.2.2 LGA Problems with Excess Solder

Excess solder may cause the LGA to “float” or bridge between the package contacts. To use the correct amount of solder paste applied to the PCB, take into consideration the following:

- Stencil thickness
- Other components mounted on the PCB
- Manufacturing equipment
- Assembly house experience

5.2.3 LGA-48 Package Dimensions

Figure 5-4 shows the LGA48 package dimensions.

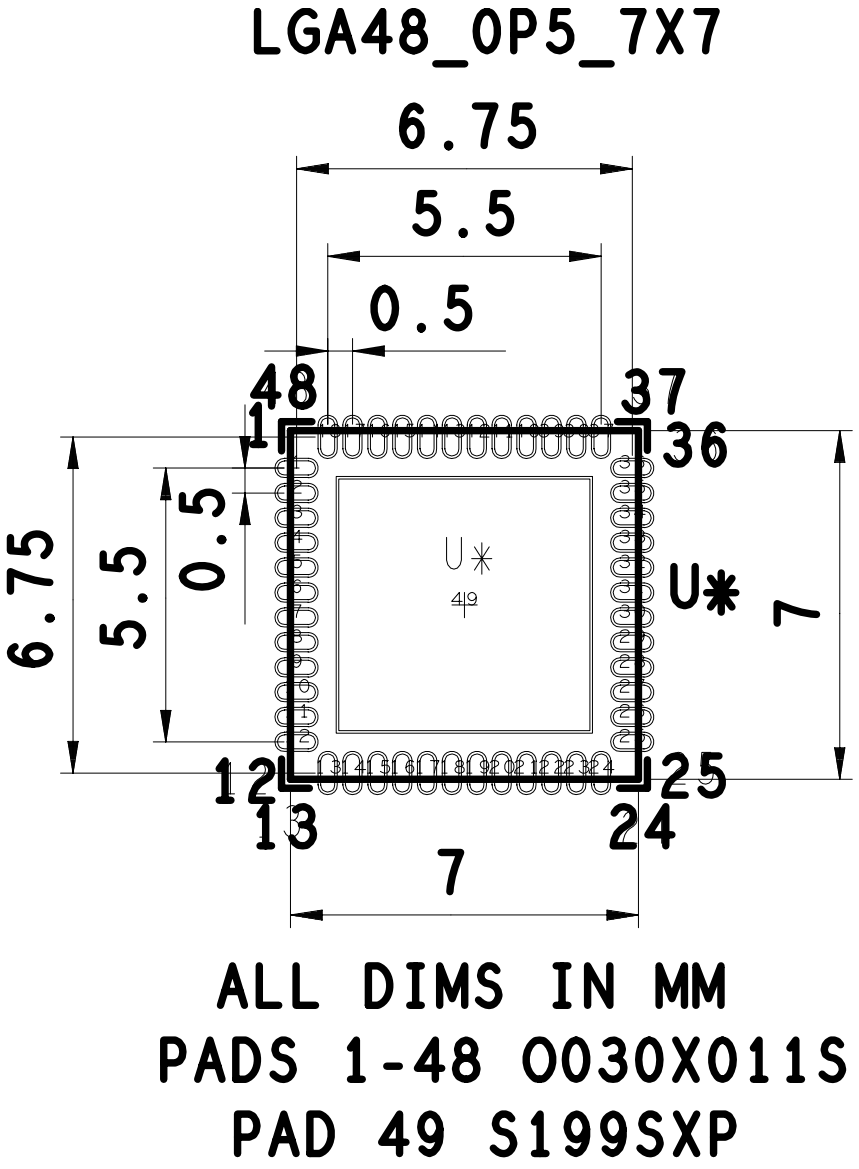


Figure 5-4. LGA Package Dimensions

5.2.4 48-Pin LGA Device Marking Details

The MC1323x devices are in the 48-pin LGA (9x9mm), Case 1664-01. The following figure show device marking examples for the LGA device.

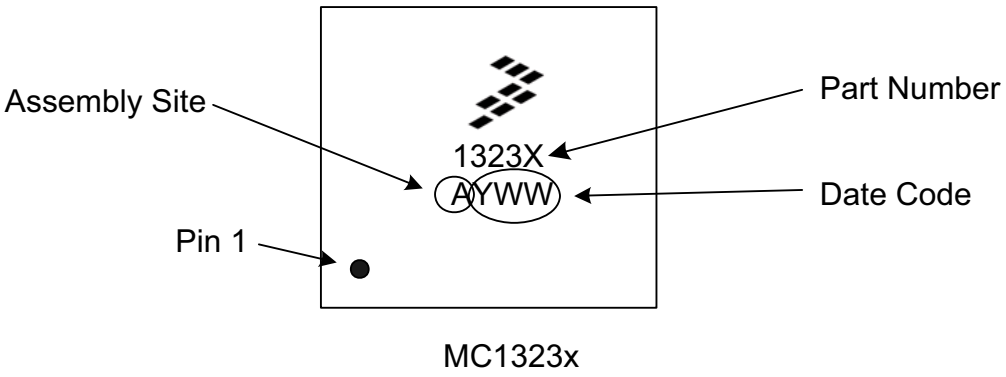


Figure 5-5. LGA-48 Device Marking

5.2.5 48-Pin LGA Tape and Reel

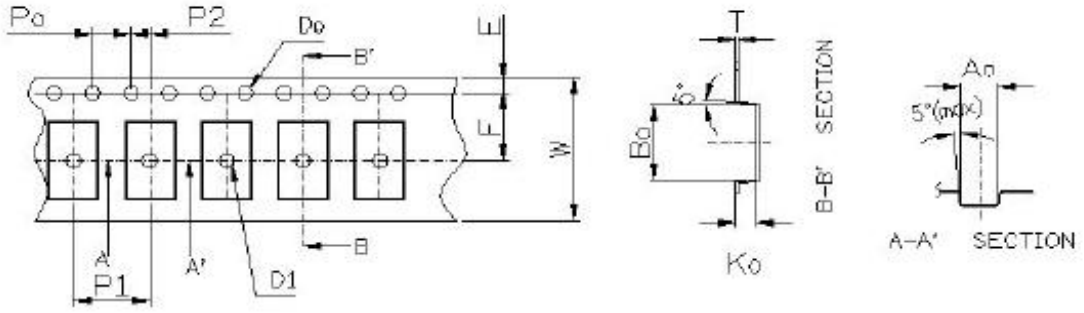
Tape and Reel packaging is available for the LGA-48 package. Reels are available to support the requirements of both first and second generation pick–and–place equipment. The packaging fully conforms to the latest EIA–481A specification. The antistatic embossed tape provides a secure cavity, sealed with a peel–back cover tape.

Embossed Tape and Reel facilitates automatic pick and place equipment feed requirements. The tape is the shipping container for various products and requires a minimum of handling. The antistatic/conductive tape provides a secure cavity for the product when sealed with the peel.back cover tape.

- Two Reel Sizes Available (7 inch and 13 inch)
- Used for Automatic Pick and Place Feed Systems
- Minimizes Product Handling
- EIA 481, -1, -2
- Tape
  - Freescale part number L10001A055
  - Supplier Part number ML0707-AC
- Reel
  - Freescale part number 57ARL10510D004
  - Supplier Part number TX16-07-W1
  - Reel Critical Dimensions:
    - A -13" diameter
    - B- 7" hub
    - W1 - to suit 16mm width

Figure 5-6 shows an example tape and reel mechanical drawing.

a.) Dimensions of Carrier Tape



Symbol	Ao	Bo	Ko	Po	P1	P2	T
Spec	3.60±0.1	5.40±0.1	1.40±0.1	4.0±0.1	8.0±0.1	2.0±0.05	0.30±0.05
Symbol	E	F	Do	D1	W	10Po	
Spec	1.75±0.1	5.50±0.05	1.55±0.05	1.50(min)	12.0±0.2	40.0±0.1	

b.) Dimensions of Reel

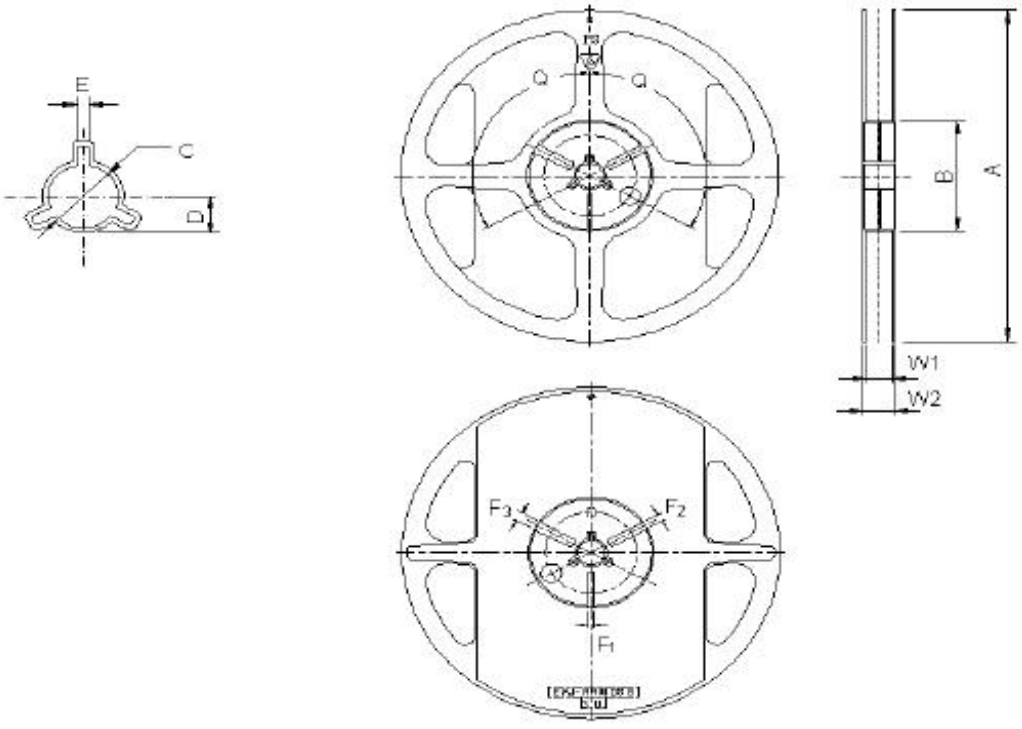


Figure 5-6. Example LGA-48 Tape and Reel Detailed Mechanical

Chapter 6
Layout and RF Design Considerations

6.1 Introduction

The Freescale IEEE 802.15.4/ZigBee product line (MC1319x, MC1320x, MC1321x , and MC1322x families) have been used in hundreds of successful designs worldwide. While every application has its own unique details, the basic RF circuitry can be copied directly from an as-is Freescale reference design for a large percentage of applications.

In the course of assisting customers with testing and initial production of IEEE 802.15.4 products based on these devices, Freescale has seen many common recurring issues that can cause initial problems. This chapter is intended as a guide to help design implementation and to smooth the transition from prototype to production.

Freescale always recommends that designers start by copying an existing Freescale reference design. This applies to both the circuit portion (schematic) of the design, and the PCB layout. For all RF designs, particularly for designs at frequencies as high as 2.4 GHz, the PCB traces are a part of the design itself. Even a very short trace has a small amount of parasitic impedance (usually inductive), which has to be compensated for in the remainder of the circuit.

The circuits used on Freescale reference designs are all tuned and optimized on the actual layout of the reference design, such that the final component values take into account the effects of the circuit board traces, and other parasitic effects introduced by the PCB. This includes such issues as parasitic capacitance between components, traces, and/or board copper layers, inductance of traces and ground vias, the non-ideal effects of components, and nearby physical objects.

The following paragraphs are not meant as a full RF design resource, but rather are intended to introduce concepts and give recommendations for Freescale circuits. The RF design process can be greatly simplified and be more successful by using the supplied reference designs.

NOTE

The RF characteristics of the PCB traces are controlled by both the trace physical size (layout length and width) AND the trace proximity to adjacent PCB metal layers (set by dielectric thickness). The PCB stackup is critical to PCB layer thicknesses and should not be overlooked.

6.2 Printed Circuit Board Layout

Freescale strongly recommends that new designs “drop in” the appropriate reference design to the greatest extent possible. Even small changes in the location of components can mistune the circuit.

What may seem like a minor change to the layout, or what would certainly be a minor change at a lower frequency of operation, can actually be a significant change at 2.4 GHz. For example, the inductance of a straight 22 gauge wire in air is approximately 0.5 nH per mm. This means that a change in length of 2-3 mm would result in a change in inductance of over one nanohenry. At lower frequencies, this would have no impact, but at 2.4 GHz this would have a significant impact in any matching circuits.

On a printed circuit board, there are no wires suspended in air, but there are metal traces over dielectric material; in RF circuits these connections typically are called microstrip lines. Microstrip is a form of transmission line, similar to a coaxial cable, except that it is unshielded. Microstrip is formed by placing a copper trace over a wider ground plane area with a substrate (the top layer of PCB dielectric material) in between.

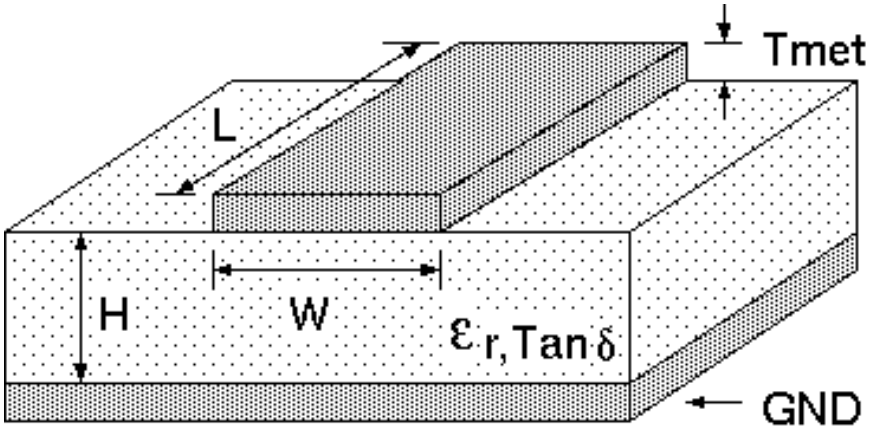


Figure 6-1. Embedded Microstrip Line

The characteristic impedance of the transmission line is controlled by:

- The width the copper trace
- The thickness of the copper trace
- The height of the line above the ground plane (that is, the thickness of the top layer of dielectric material)
- The dielectric constant of the dielectric material

By a judicious selection of materials and parameters, a line of a desired specific impedance (usually 50 ohms) can be fabricated.

NOTE

Short lengths of 50 ohm microstrip line are used in all Freescale reference designs for 802.15.4/ZigBee applications.

While it is possible for a designer to perform the calculations needed to determine the correct microstrip dimensions, it should not be necessary if the design uses FR4 material. Freescale has several existing

designs for both 2 metal layer and 4 metal layer PCB stackups, and it should only be necessary to copy the appropriate reference design.

NOTE

If the PCB material is something other than FR4 material, the dielectric constant can change, and the line width must be modified to provide the same desired characteristic impedance.

Table 6-1. Lines Used in Freescale Reference Designs

PCB Type	Top Layer "Height" (Thickness in mils)	Nominal 50 ohm Trace Width (mils)
2-layer	32	55
4-layer	10	18
4-layer	200um (7.87 mils)	14

For a typical 50 ohm microstrip line on FR4, a 1 mm length segment, is about 5 electrical degrees in length at 2.45 GHz., which is not insignificant.

The width of a line as impedance changes is not linear, that is, a line that is intended to be of 100 or 200 ohms impedance will be much narrower than a 50 ohm line. A 50 ohm line is approximately 18 mils wide over a top layer dielectric thickness of 10 mils of FR4. On the same substrate, a 100 ohm line is 3.15 mils wide, and a 150 ohm line is less than one mil.

It is not practical to use 100 or 200 ohm lines in most current-day FR4 applications because the line width would be too narrow for reliable manufacture, where the overall PCB thickness is usually 0.032" or less. The only solution is to make the lines as narrow as current PCB technology will allow (usually 4- 5 mils) and also make them as short as possible. Finally, the values of the matching components are tuned on the actual layout for optimum performance, which compensates for any deviations in the actual circuit from the ideal. This has been done on all of the Freescale 802.15.4/ZigBee reference designs, and that is why it is so vital to copy the reference design exactly for this portion of the circuit.

Reference designs are available from the Freescale ZigBee web site at www.freescale.com/zigbee.

6.3 PCB Stackup

As shown in Figure 6-1 regarding microstrip transmission lines, it is important to copy not just the physical layout of the circuit, but also the PCB stackup. Any small change in the thickness of the dielectric substrate under the microstrip will have a significant change in impedance. In the example above, a 50 ohm trace was 18 mils wide over 10 mils of FR4. If that thickness of FR4 is changed from 10 to 6 mils, now the impedance will be only about 36 ohms.

Also when the top layer dielectric becomes too thin, the layers will not act as a true transmission line; even though all the dimensions are correct. There is not universal industry agreement on which thickness at which this occurs, but Freescale prefers to use a top layer thickness of no less than 8-10 mils.

There is a also a limit to the ability of PCB fabricators to control the minimum width of a PCB trace and the minimum thickness of a dielectric layer. Plus or minus one mil will have less impact on an 18 mil wide trace and a 10 mil thick dielectric layer, than it will on a much narrower trace and thinner top layer.

This can be an especially insidious problem. The design will appear to be optimized with the limited quantity of prototype and initial production boards, in which the bare PCB's were all fabricated in the same lot. However, when the product goes into mass production there can be variations in PCB fabrication from lot-to-lot which can degrade performance.

There is no theoretical limitation on maximum PCB thickness, except for physical size constraints. However, as the PCB becomes thicker, the ground vias by necessity become much longer, and much more inductive. Freescale recommends a maximum thickness of 32 mils for a 2-layer PCB stackup.

Table 6-2. Approximate Via Inductance and Length at Various Via Diameters

Approximate Inductance (PH)	Length (mils) at 8 mil Via Diameter	Length (mils) at 10 mil Via Diameter	Length (mils) at 12 mil Via Diameter	Length (mils) at 14mil Via Diameter
1000	60			
950		60		
900			60	
825				60
600	40			
575		40		
550			40	
500				40
375	25			
350		25		
300			25	
325				25
150	10			
140		10		
130			10	
120				10

All Freescale IEEE 802.15.4/ZigBee reference designs come with complete PCB stackup and fabrication details.

6.4 Components

All electronic components have parasitic characteristics that cause the part to act in a non-ideal way. Typically, these effects become worse as the frequency of operation is increased.

For most component suppliers, this quality is expressed by the Self Resonant Frequency (SRF) specification. For example, a capacitor has parasitic inductance introduced by the metal leads of the components. As frequency increases, at some point the impedance due to the parasitic inductance is greater than the impedance of the capacitor, and at that frequency and higher, the component no longer acts as a capacitor and now acts as an inductor. At the point at which the impedance from both inductive and capacitive components is the same, the part will resonate as a LC parallel resonant circuit, and this is called the Self Resonant frequency. Figure 6-2 shows some typical response curves.

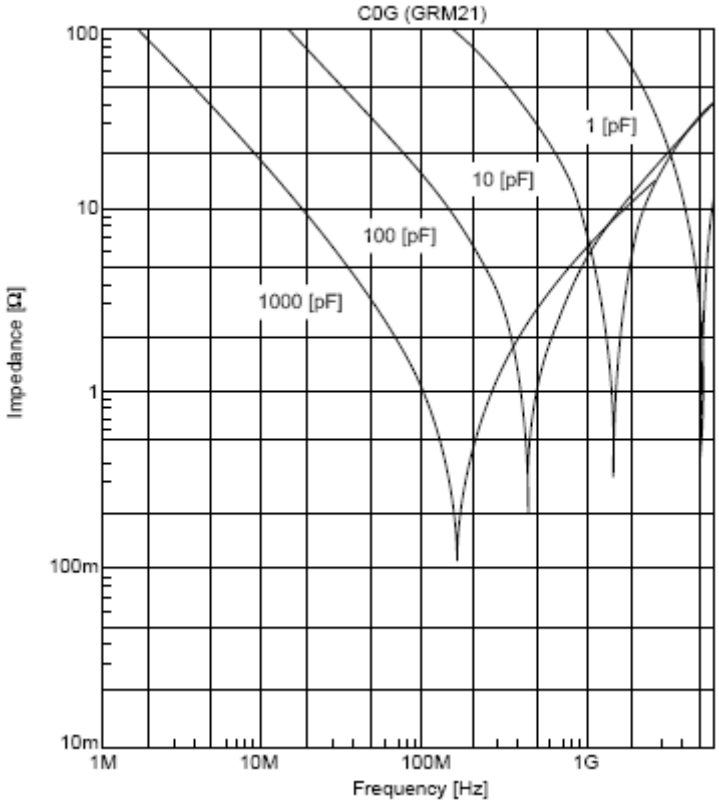


Figure 6-2. RF Plots for 0805 Ceramic Capacitors (Typical)

The same is true of inductors. There is parasitic capacitance in an inductor, mainly due to capacitive coupling between the turns of wire. At some point in frequency, this capacitance will have a higher impedance than the inductance of the part. From this frequency and higher the part acts as a capacitor and not as an inductor.

The Bill of Materials (BOM) is available for all Freescale reference designs. The BOM shows the specific vendors and part numbers used on Freescale designs. It is certainly possible to substitute another vendor's parts, but it may impact the performance of the circuit, therefore, it may be necessary to use different component values when parts from another vendor are used.

If there is a performance issue on a new design, and part substitutions were made on that design, then it is strongly recommended that components identical to those used in the Freescale reference design be placed on the new design for test purposes. Once the design is working properly with components that are identical to those used by Freescale, then it will be possible to substitute components from other vendors one at a time, and test for any impact on circuit performance.

6.5 Antenna

Freescale has tested many types of antennas. For a PCB-based design, Freescale has seen the best and most consistent performance from the Inverted-F antenna. The Inverted-F antenna is used on all current Freescale IEEE802.15.4/Freescale reference designs.

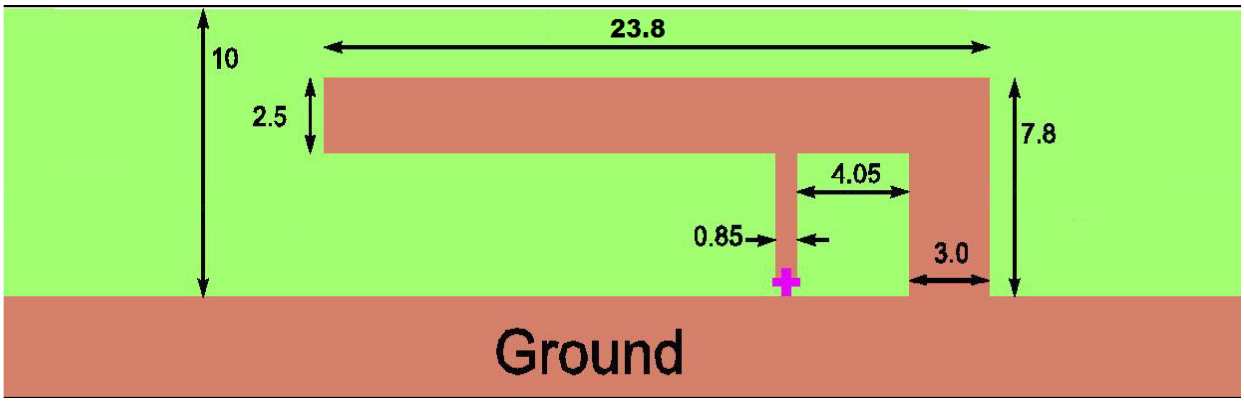


Figure 6-3. Inverted-F Antenna

Freescale reference designs show the ideal dimensions for the Inverted F antenna at 2.45 GHz. However, there are many conditions under which the length of the antenna may need to be adjusted.

- The ground plane area behind the main antenna element is a part of the antenna, and it cannot be eliminated from the layout. If the ground plane area behind the antenna is much wider or much narrower than what Freescale reference designs use, then the overall length of the main antenna element may need to be adjusted to compensate.
- The response of the antenna is impacted by the amount of FR4 material that surrounds it. Many designers, in order to save PCB area, have eliminated the strip of FR4 between the antenna element and the front edge of the board. While the antenna will still work with this approach, it is necessary to adjust the length of the antenna to compensate.
- Any objects other than air which are near the antenna will have an impact on it. While it may seem obvious that the antenna will be affected by any metal objects near the antenna, it is also true that any objects which do not have the dielectric constant of air, such as a plastic case or a human hand, will also detune the antenna. In some cases the antenna may need to be optimized with the final enclosure in place around the PCB.

6.6 Harmonics

All of the design considerations discussed above definitely apply to the transmitter harmonics. Since the desired in band signal is at ~2.45 GHz, this places the second harmonic at almost 5 GHz., and the third harmonic at well over 7 GHz. The parasitic effects of components will have a greater impact at these frequencies. If component substitutions are made, it is very possible that the in-band performance is fine, but that the harmonic suppression has been degraded and must be evaluated.

For example, the inductors or capacitors used from one vendor may have an SRF that is well above 10 GHz., while parts from another vendor may not function as expected at the second or third harmonic.

Experience at Freescale has shown that this is particularly true of ceramic monolithic baluns. Generic baluns or even specific part numbers from some vendors have inherent harmonic suppression as a by-product of the component's design, while a similar balun from another vendor (or even from the same vendor) may not.

The same concept applies to the PCB layout. A trace that is very short from an electrical standpoint at 2.4 GHz may actually have a significant impact at the second or third harmonic frequency. So, just as with components, it is possible that a change in layout does not impact performance in-band will degrade harmonic suppression and must be checked.