
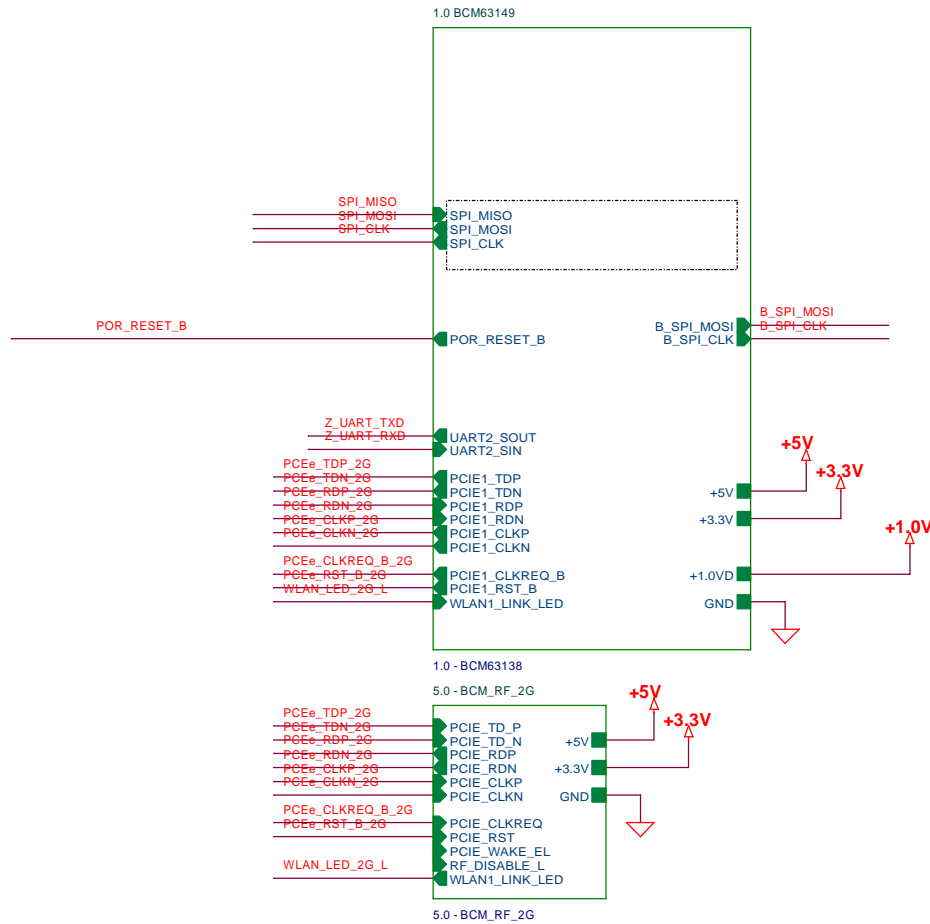



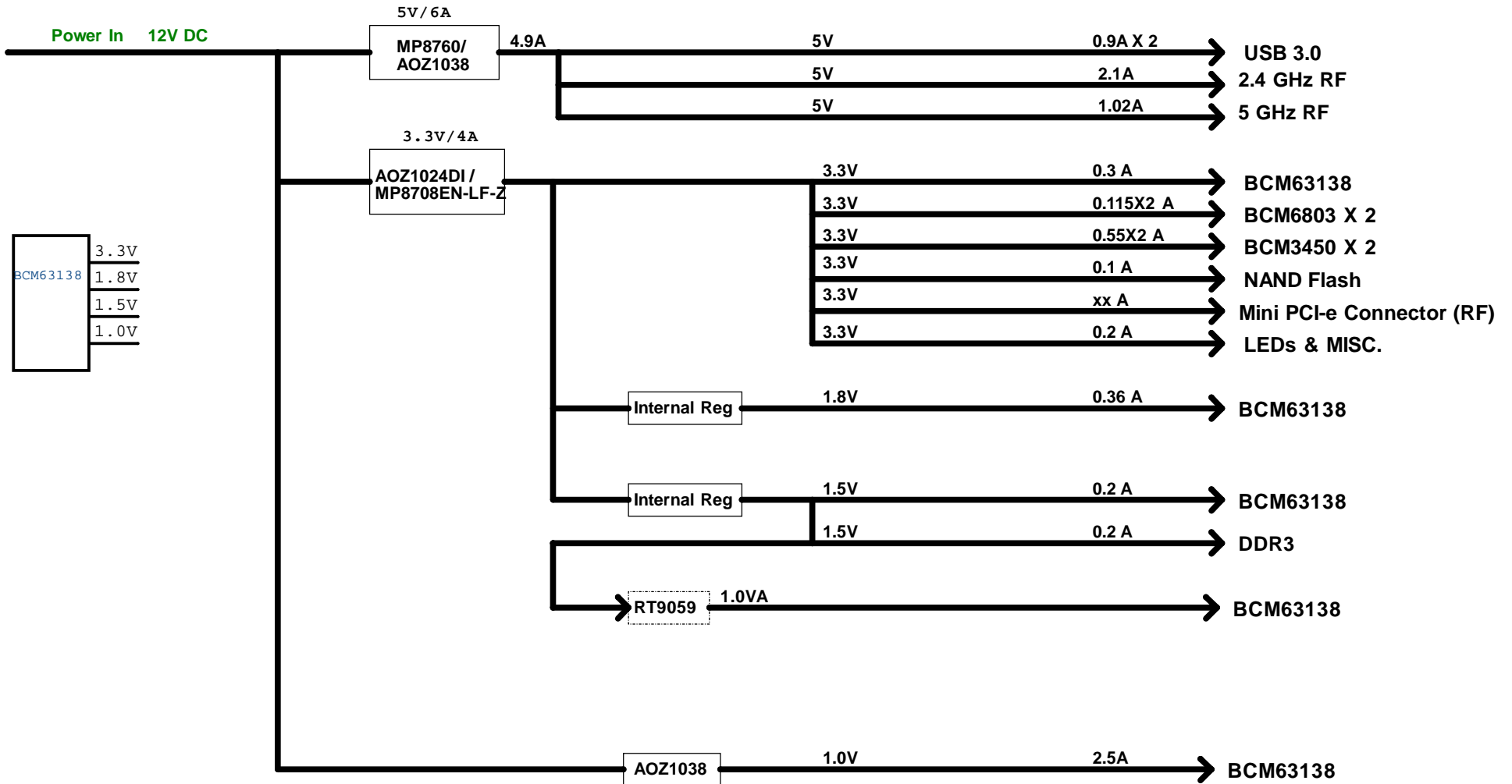
Rev1A3 Revision


- 1) move C1013 out of shield (layout)
- 2) swap D132 and D143 (layout)
- 3) add R25 for R3000 (schemaitc and layout)
- 4) change C51 to through hole

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	Size B	CAGE Code <Cage Code>	DWG NO R3000
0.2 REVISION	Modified: Saturday, September 13, 2014		Rev 1B3
Scale		Sheet	2 of 17

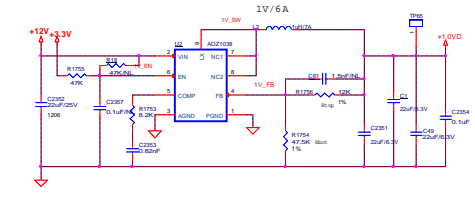
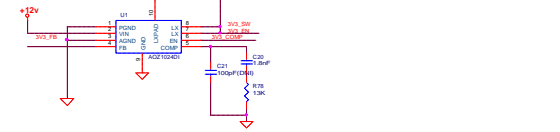
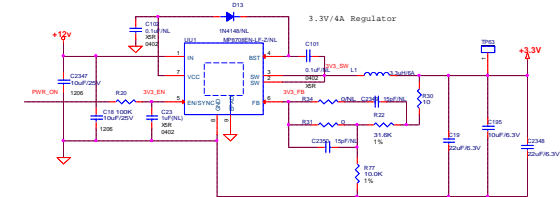
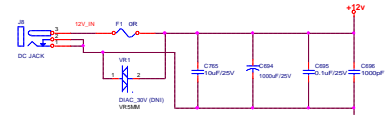


		ACTIONTEC ELECTRONICS, INC 760 N. MARY AVE. SUNNYVALE, CA94086 http://www.actiontec.com	
		0.3 TOP	Size B CAGE Code <Cage Code>
Modified: Saturday, September 13, 2014		Scale	Sheet 3 of 17

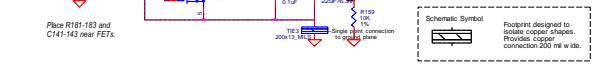
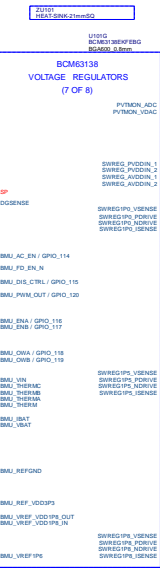
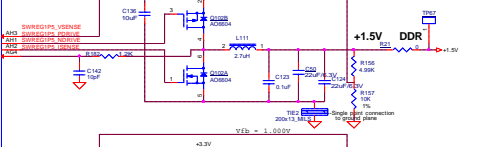
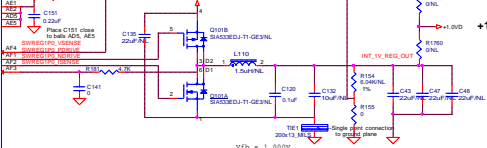
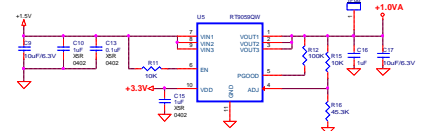
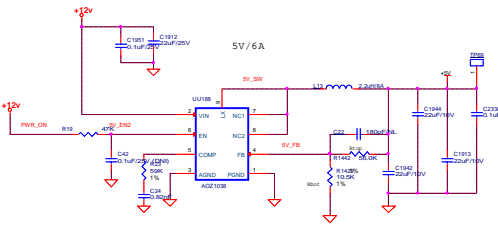
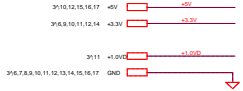


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	0.4 POWER SCHEME	Size B CAGE Code <Cage Code>	DWG NO R3000	Rev 1B3
Modified: Saturday, September 13, 2014	Scale	Sheet 4 of 17		

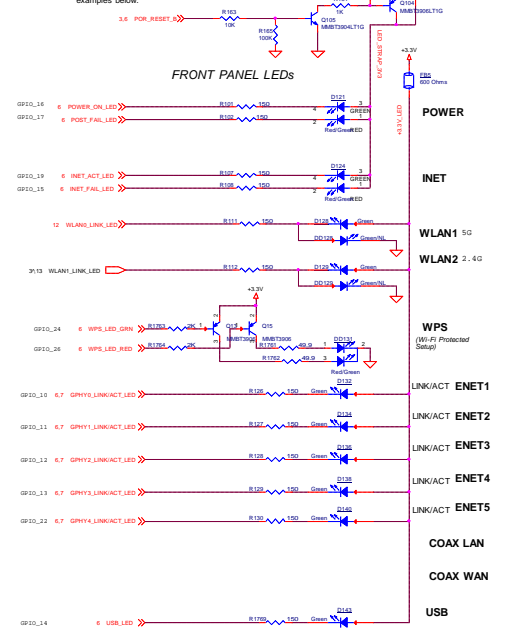
+12VDC Regulated Input



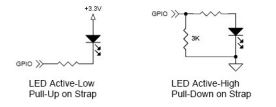
$AOZ1020AI\ V_{out} = 0.8 \cdot \left[\frac{R_{top} + R_{bot}}{R_{bot}} \right]$



This transistor circuit prevents the LEDs from asserting a high on the strap settings of gpio(30,20,16,15). This circuit is used for the evaluation board. To allow the DIP switch to set the strap. A production board should connect the LEDs to match the desired strap settings of the gpio. See examples below.



If an LED is connected to a gpio with strap function, the orientation of the LED must be configured so the desired strap value is set. If the strap should be set high, configure the LED as active-low. If the strap should be set low, configure the LED as active-high.



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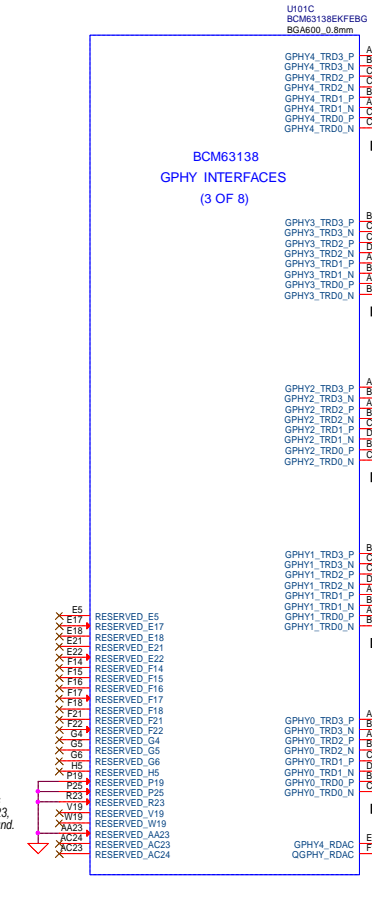
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1.1 POWER AND LEDs	Rev 01	EDGE Code	DWG NO R3000	Rev 001
Manufact	Date	Drawn	Sheet	5 of 17

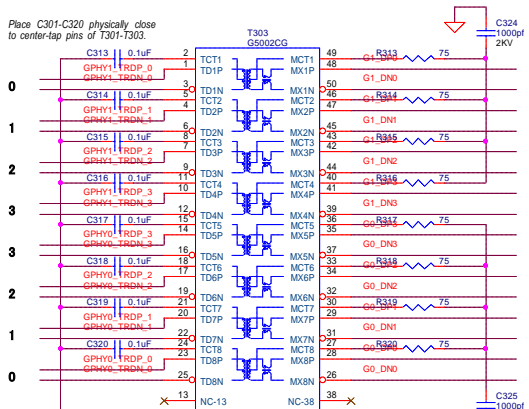
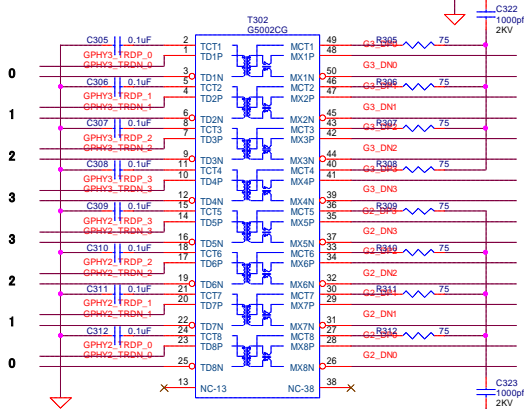
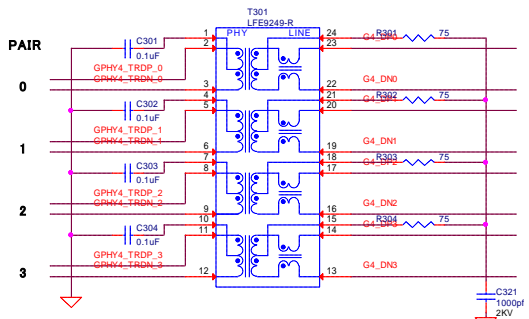
GPHY - Layout Guidelines & Notes

1. Route RDN, RDP and TDN, TDP pairs differentially, with 100ohm differential impedance, adjacent to the ground plane.
2. Keep differential pairs within a port separated by 3H distance and pairs between ports separated by 5H where H is the height of traces above the ground plane. I.e. H = the dielectric thickness.
3. Match differential pair trace length within the pair (P and N) to 10mils. No need to match trace length between differential pairs (RD and TD).

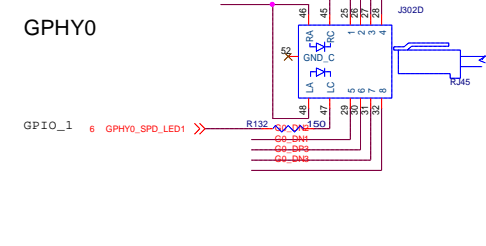
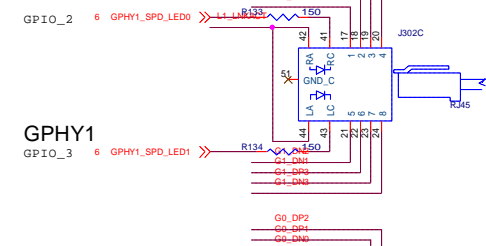
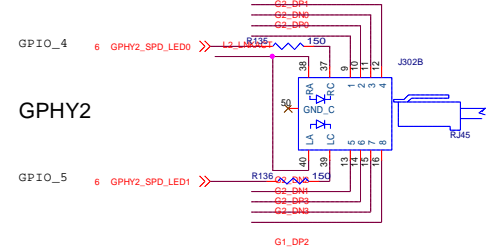
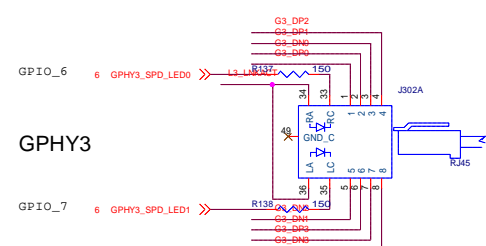
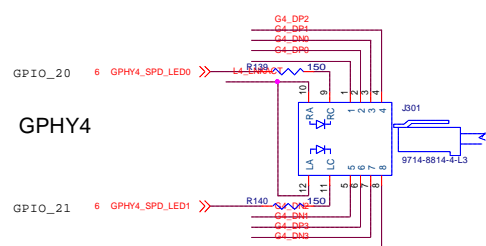
Note pair ordering for best layout.



PHY4 can be WAN



Place C301-C320 physically close to center-tap pins of T301-T303.

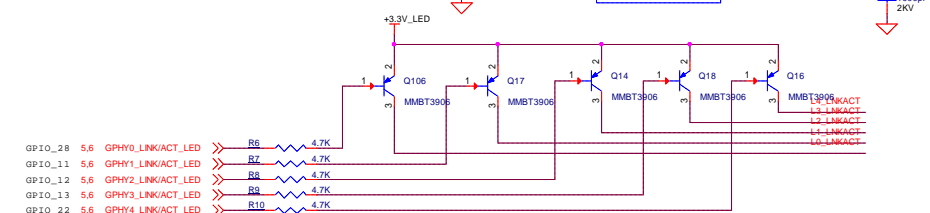


Connected balls P19, P25, R23, AA23 to ground.

Integrated GPHY addresses

The address of the integrated GPHY4 is configurable with the setting of bits [12:08] in the SWITCH_REG_SPHY_CNTRL register. Default phy address = 0x5.

The addresses of the integrated Quad GPHY are = base + offset, where offset = 0,1,2,3 and base is configurable with the setting of bits [16:12] in the SWITCH_REG_GPHY_CNTRL register. Default base value = 0x1.

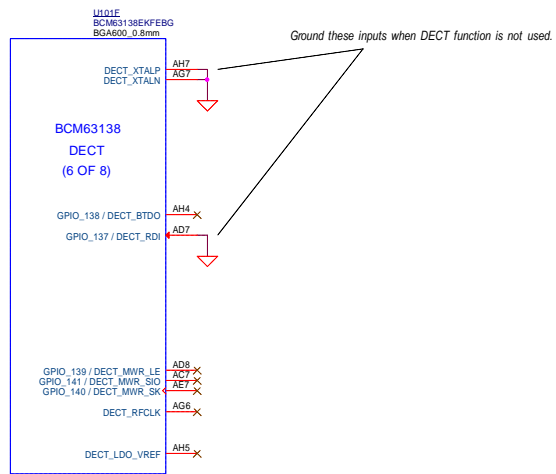
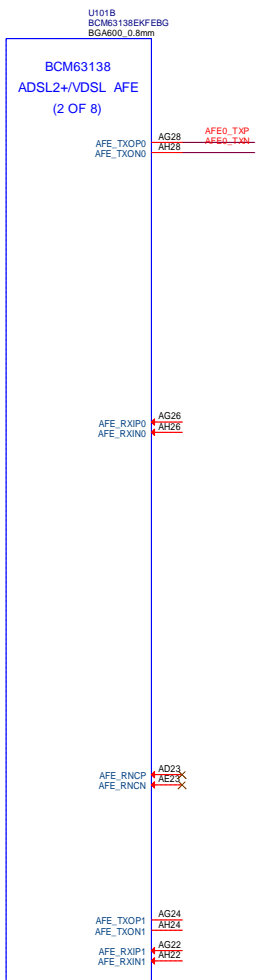



1.3 GPHY0-4

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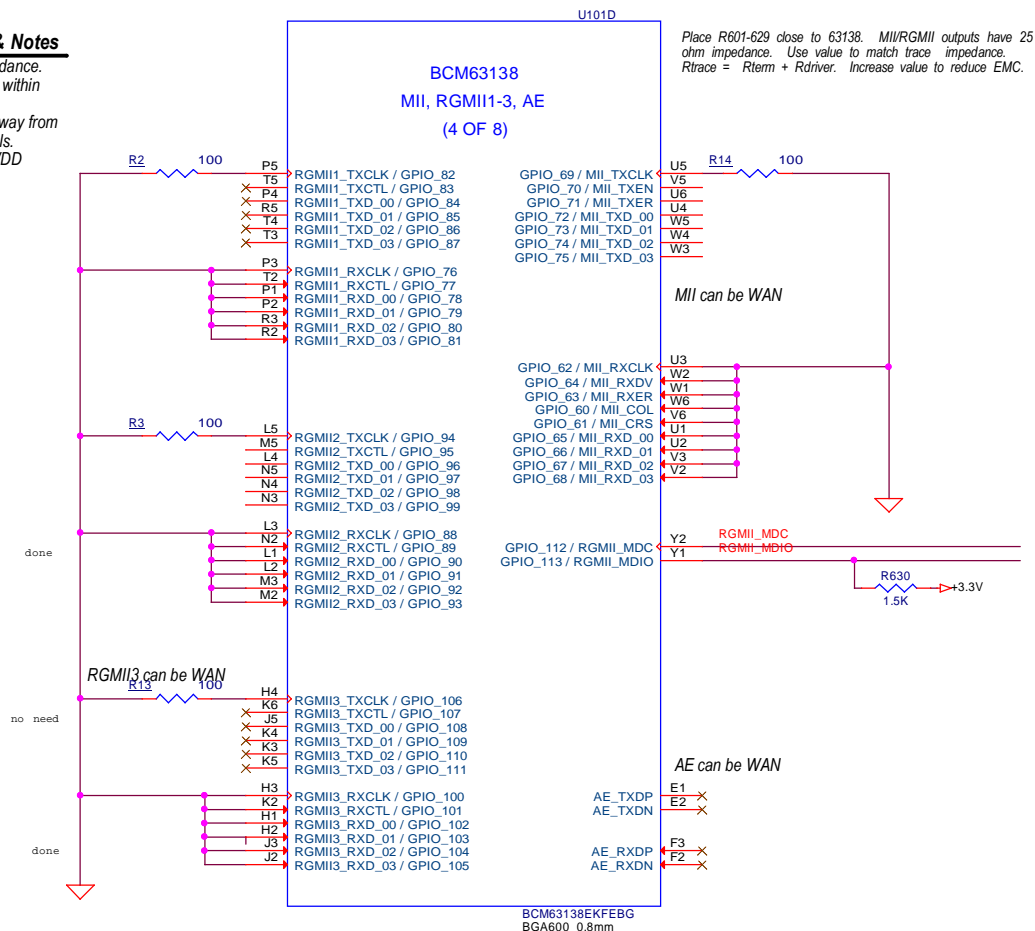
Size C	CAGE Code	DWG NO	Rev
Scale	<Cage Code>	R3000	183
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		ACTIONTEC ELECTRONICS, INC 760 N. MARY AVE. SUNNYVALE, CA94086 http://www.actiontec.com			
		Size	CAGE Code	DWG NO	Rev
1.4 VDSL AFE AND DECT		C	<Cage Code>	R3000	1B3
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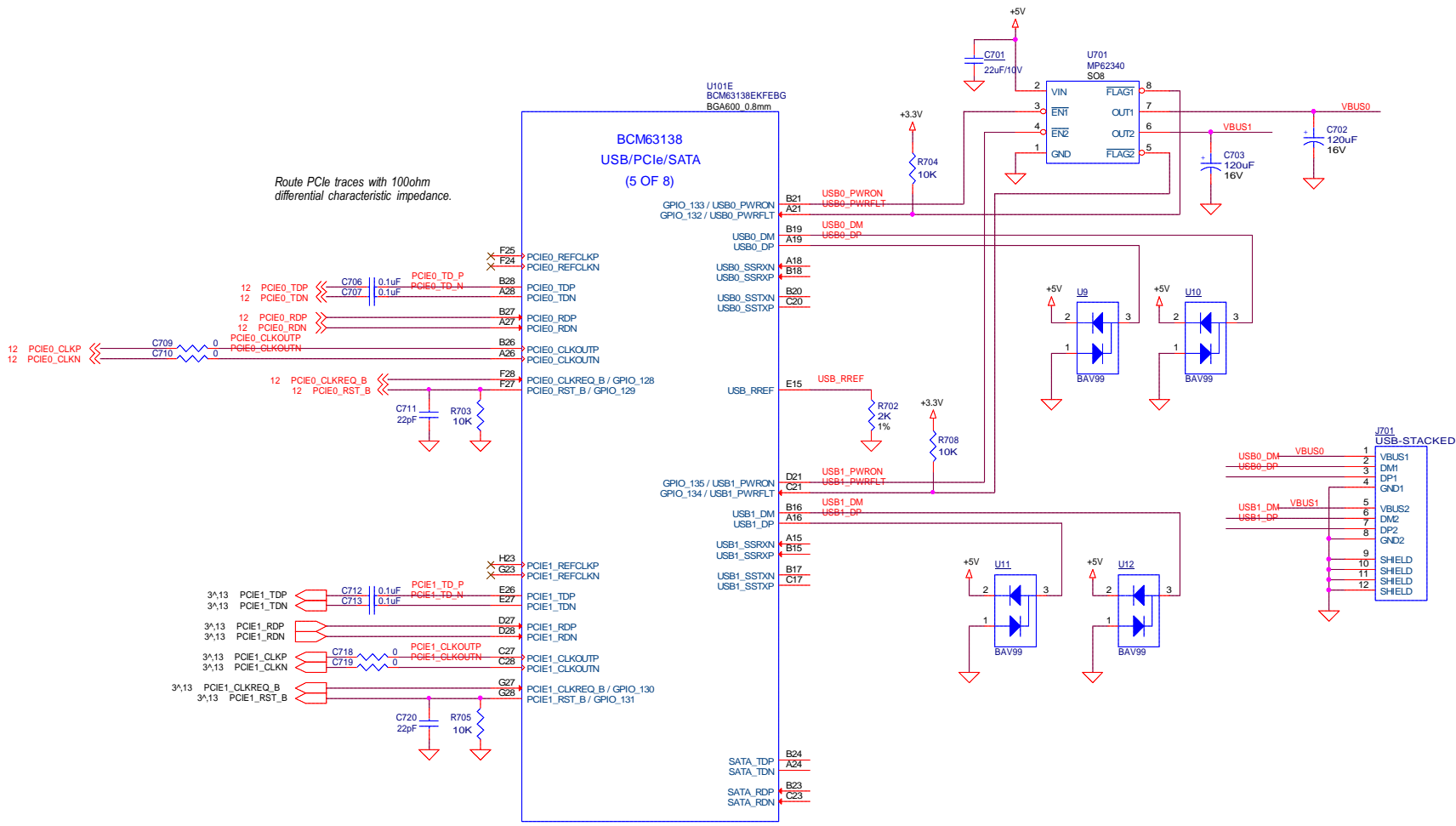
MII/GMII/RGMII - Layout Guidelines & Notes

1. Route traces with 50ohm characteristic impedance.
2. Match trace lengths to a tolerance of 385 mil within TX and RX separately.
3. Keep the receive and transmit signals kept away from each other and other analog and clock signals.
4. Place capacitors and ferrite beads close to VDD traces and routes short.



Place R601-629 close to 63138. MII/RGMII outputs have 25 ohm impedance. Use value to match trace impedance. $R_{trace} = R_{term} + R_{driver}$. Increase value to reduce EMC.

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		Size B	CAGE Code <Cage Code>
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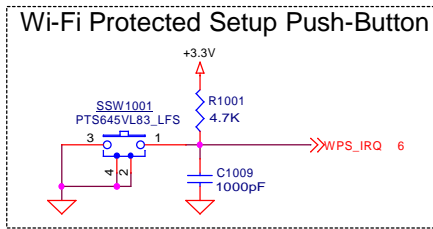
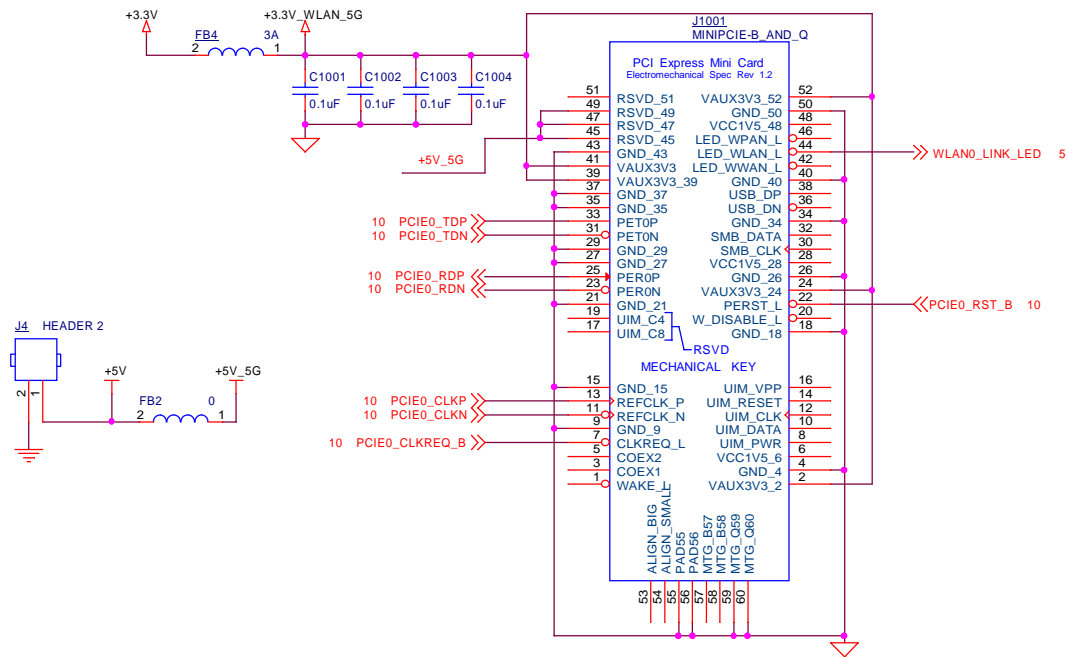



Route PCIe traces with 100ohm differential characteristic impedance.

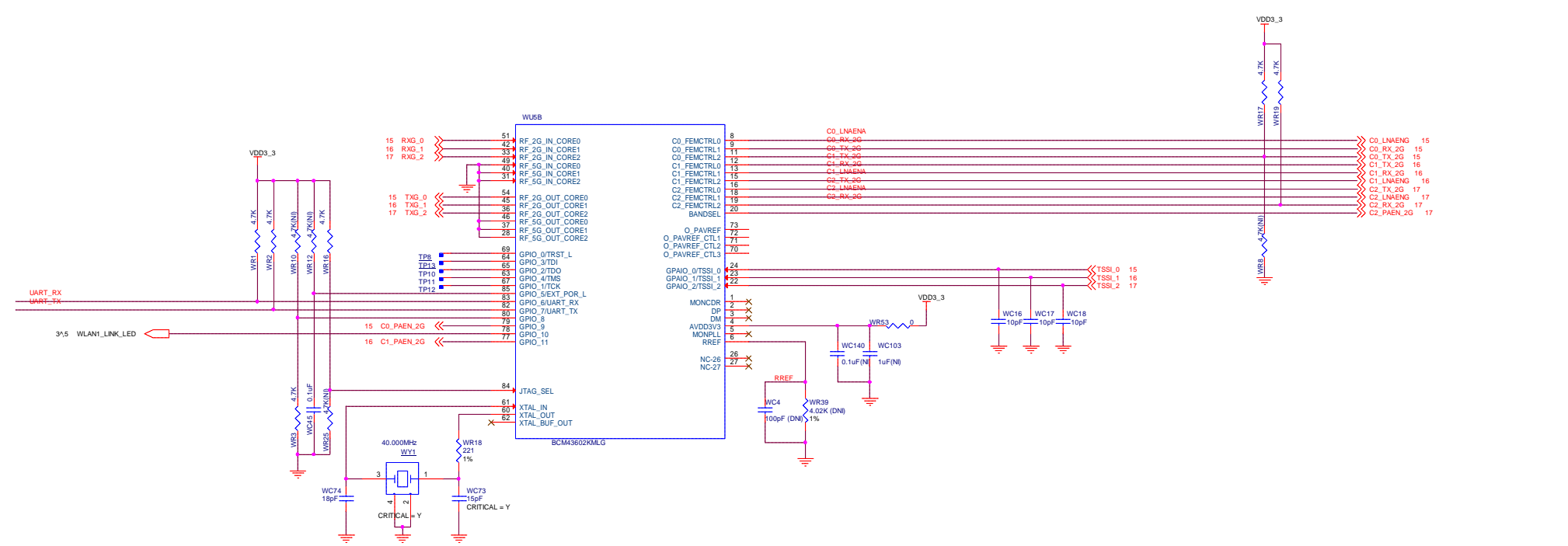
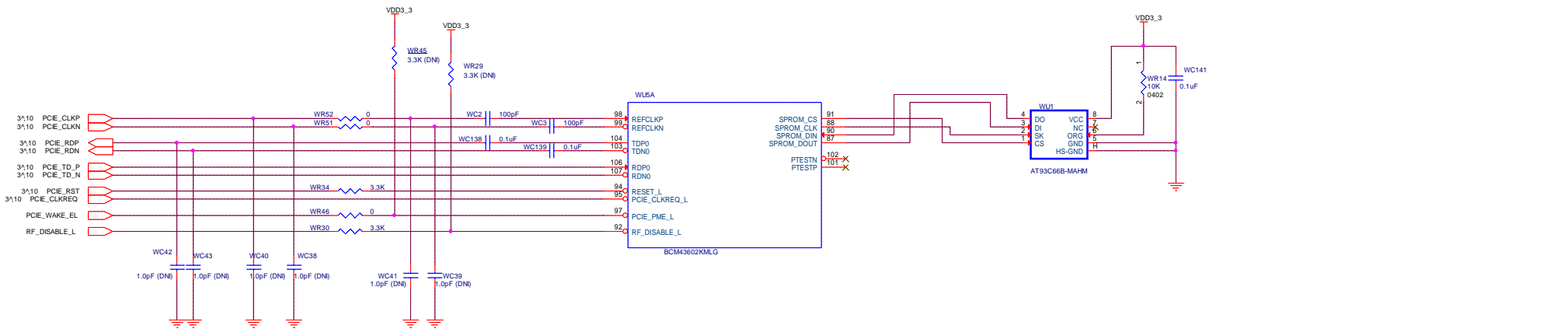
USB3.0 - Layout Guidelines & Notes

1. Route DM/DP pair with 90 ohms differential impedance.
2. Route Super Speed SSRX and SSTX pairs with 100 ohms differential impedance.
3. The P and N traces are length matched, with max differential skew, within 20mils
4. Differential trace length must be less than 5 inches
5. No more than 2 vias per trace, prefer zero.
6. Never split the ground plane under differential pair routing
7. Route differential pairs above the GND plane.
8. Adjacent differential pairs should be separated by at least 3 times the trace width. (e.g. 7.5 mil trace, leave >22.5mils between adjacent diff pairs)

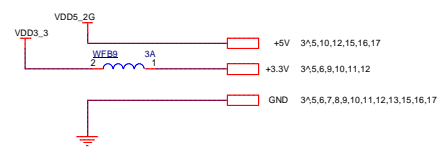
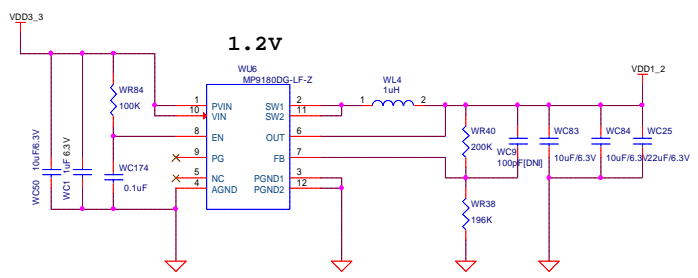
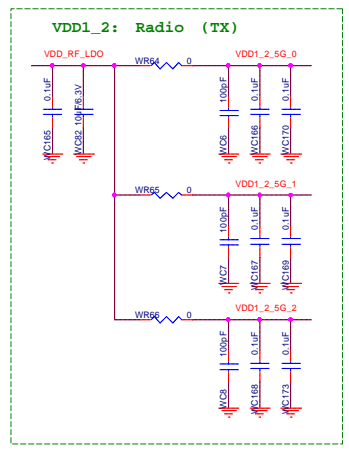
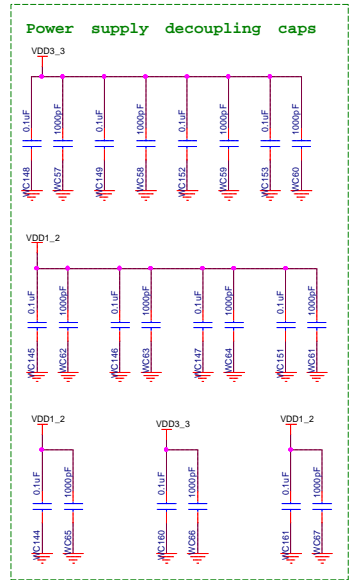
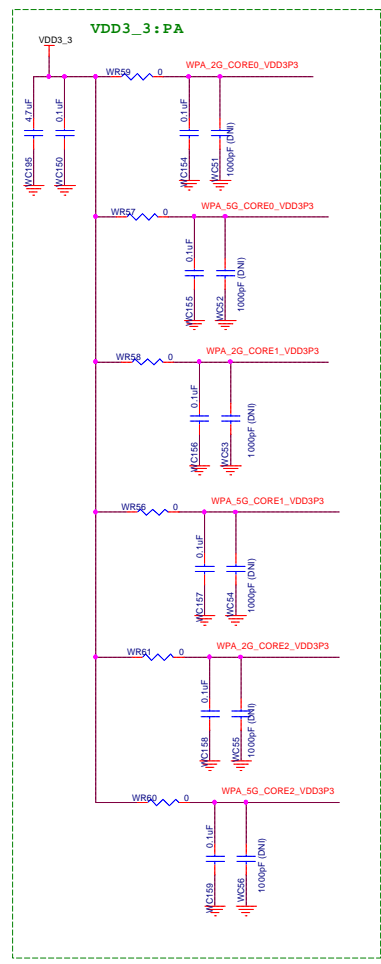
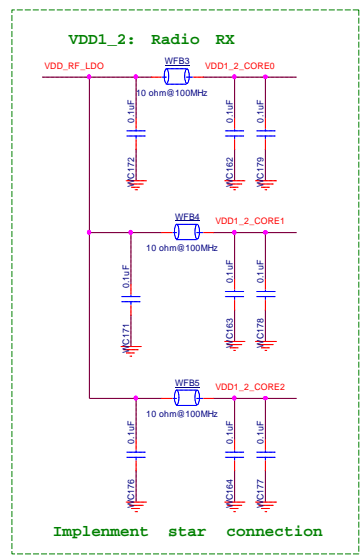
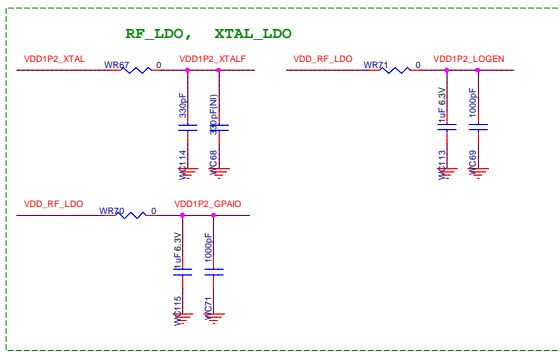
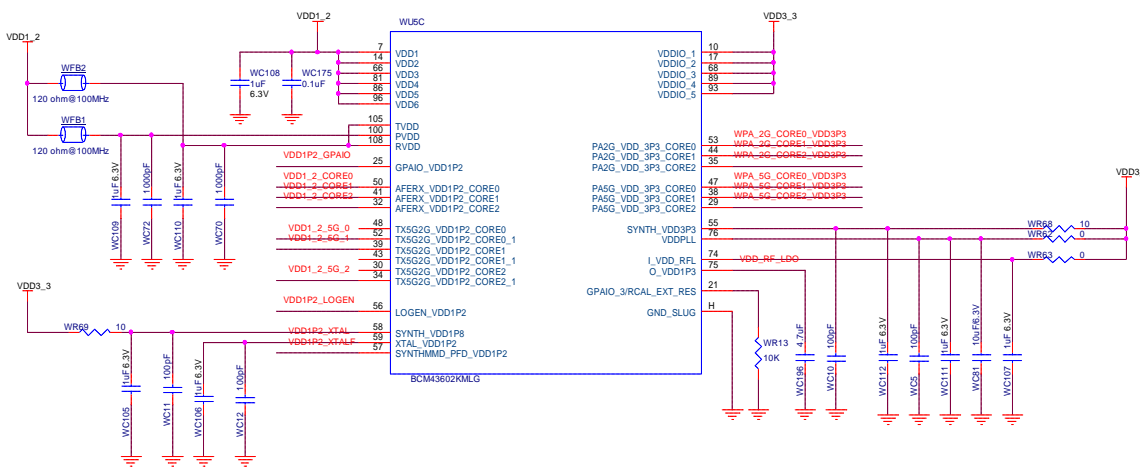
		ACTIONTEC ELECTRONICS, INC 760 N. MARY AVE. SUNNYVALE, CA94086 http://www.actiontec.com	
		1.6 PCIe, SATA, USB	Size: Custom CAGE Code: <Cage Code>
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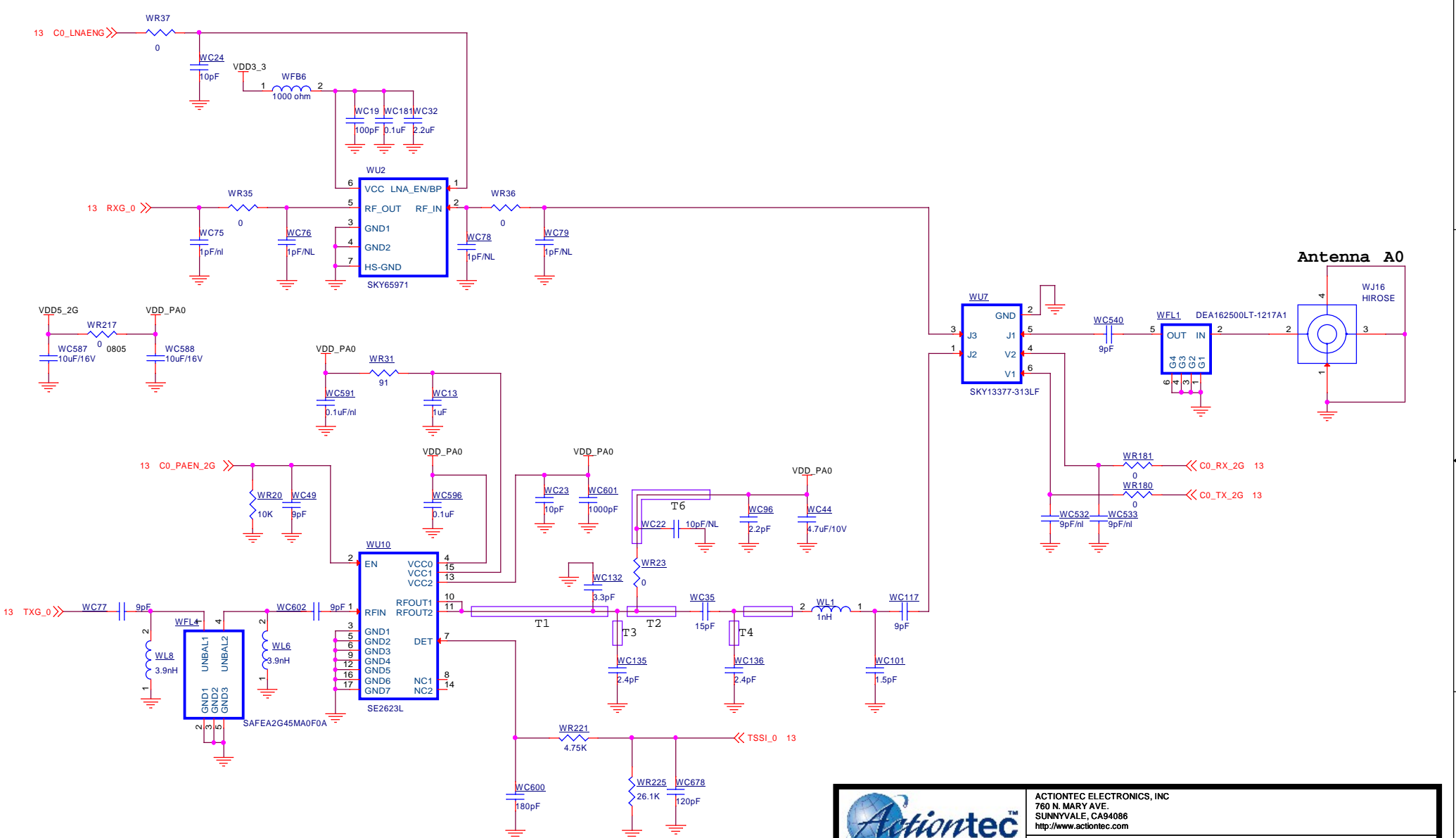
		ACTIONTEC ELECTRONICS, INC 760 N. MARY AVE. SUNNYVALE, CA94086 http://www.actiontec.com	
		1.8 PCI E SOCKETS	Size B CAGE Code <Cage Code>
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	ACTIONTEC ELECTRONICS, INC 760 N. MARY AVE. SUNNYVALE, CA 94086 http://www.actiontec.com			
	5.1 43602 PCIe/CONTROL LINES	Size C CAGE Code <Cage Code>	DWG NO R3000	Rev 1B3
Modified: Saturday, September 13, 2014	Scale	Sheet	13 of 17	

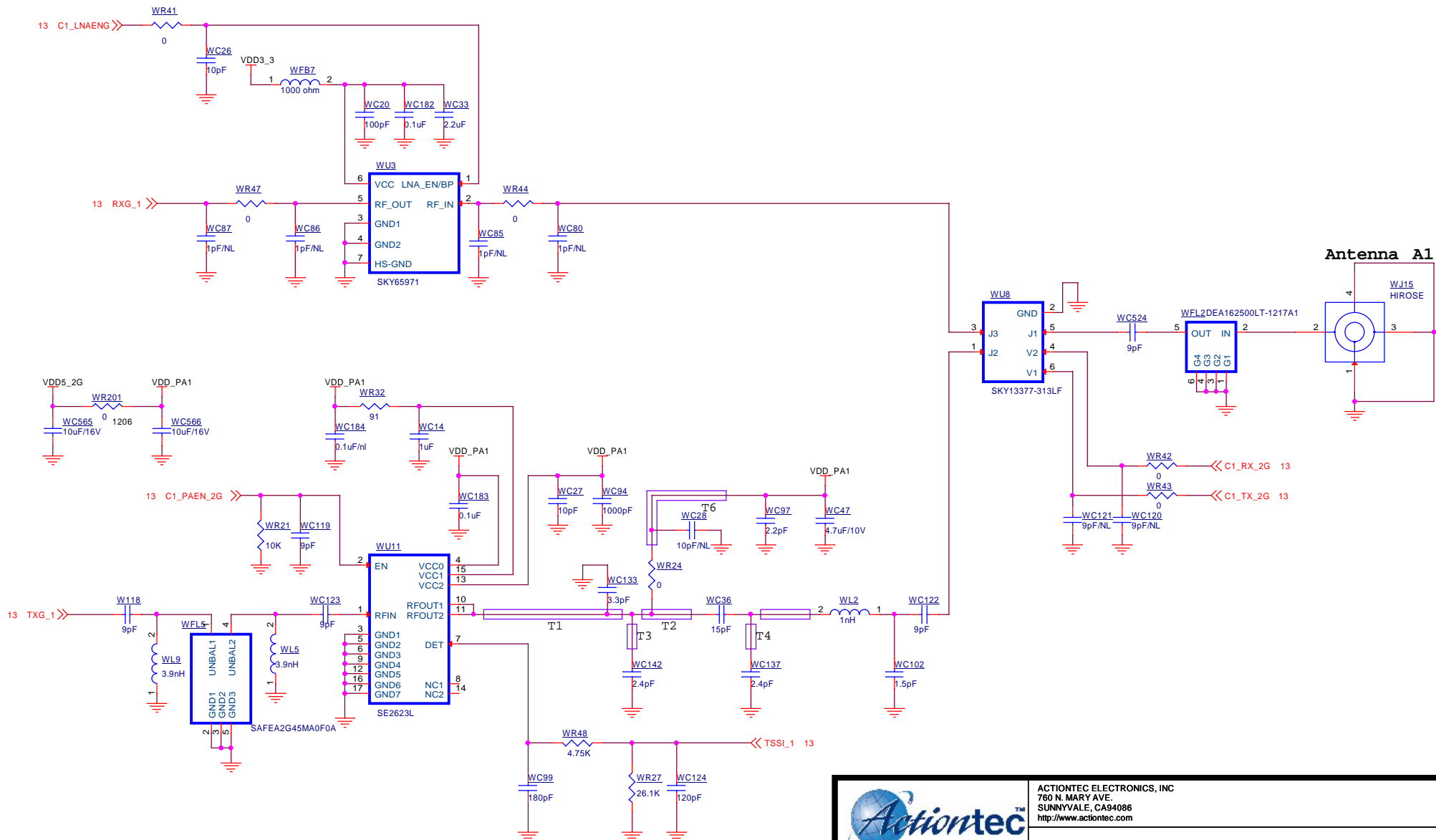



		ACTIONTEC ELECTRONICS, INC. 760 N. MARY AVE. SUNNYVALE, CA 94086 http://www.actiontec.com			
5.2 43602 POWER		Size C	CAGE Code <Cage Code>	DWG NO R3000	Rev 1B3
Modified: Saturday, September 13, 2014		Scale	Sheet	14 of 17	

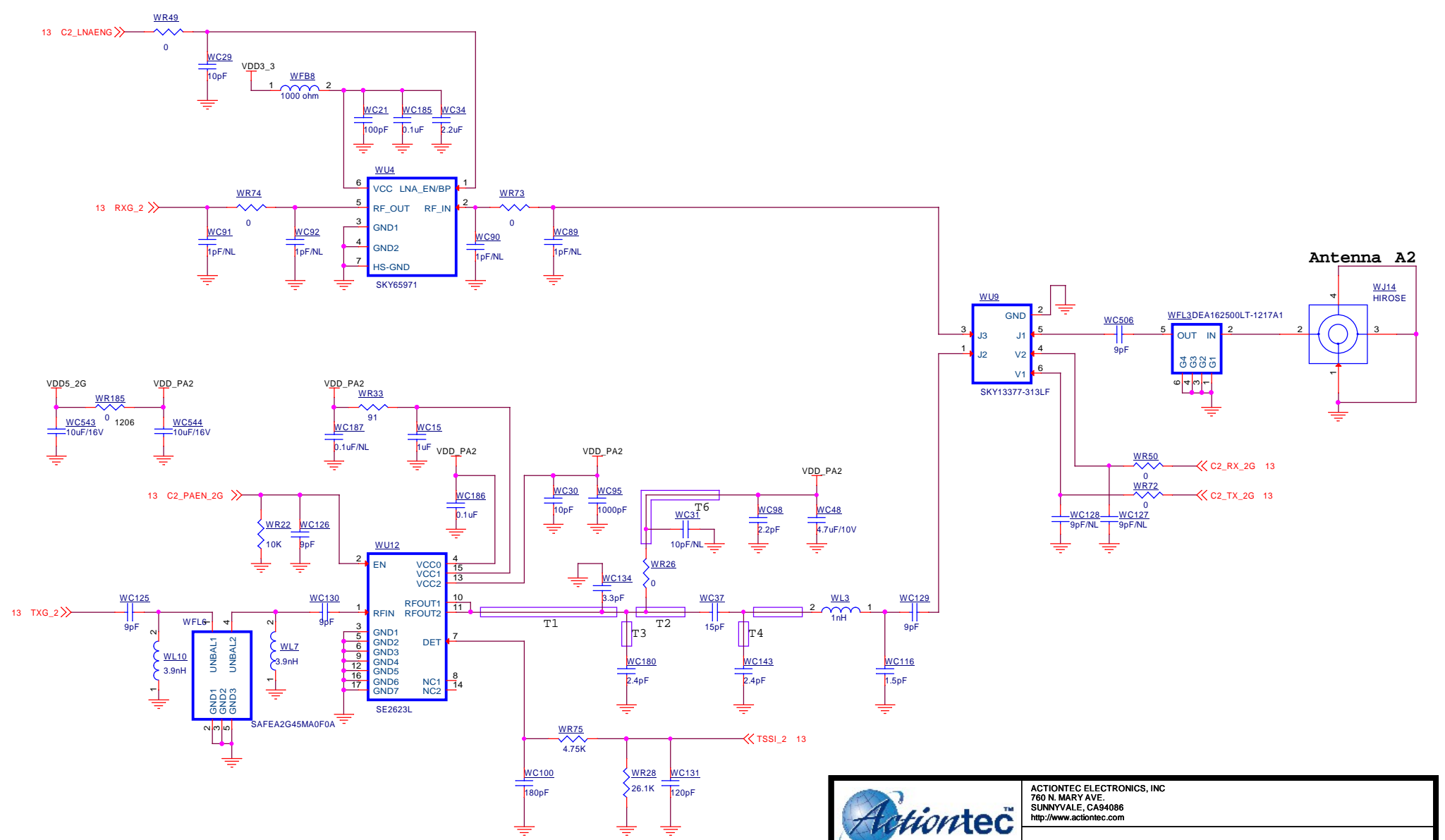



Antenna A0

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	5.4 RF FRONT END - CH1		
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				Size	CAGE Code	DWG NO	Rev
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5.5 RF FRONT END - CH2

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Size	CAGE Code	DWG NO	Rev
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