Basic Operation Theory of Actiontec Bluetooth BTM200B

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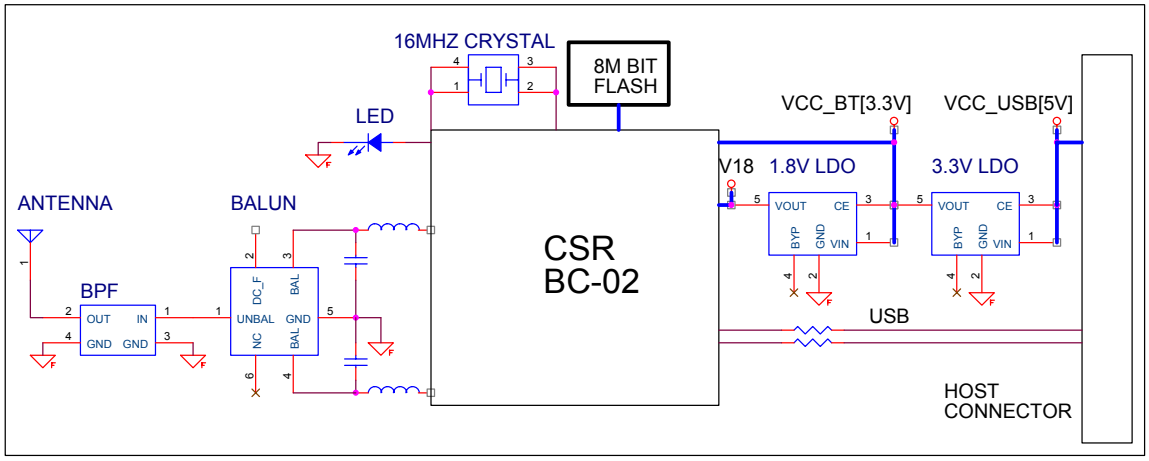

System Block Diagram

Actiontec BTM200B is using BlueCore 2 (CSR BC-02) of Cambridge Silicon Radio as its main chip set. It is actually a combination of 2.4GHz ISM Band Tranceiver, Baseband & Logic plus Microcontroller. The module is fully compliant with Bluetooth Standard v.1.1. Basically it is FHSS (Frequency Hopping Spread Spectrum), which is 1600 hops/s, and the modulation of RF carriers is GFSK (Gaussian Frequency Shift Keying).

Transmitter Path

Refer to the Device Diagram and System Block Diagram. The transmitter output power is Bluetooth Class 2, or 4dBm maximum. The module interface format is USB (Universal Serial Bus). So the BTM200B module acts as a USB peripheral, responding to requests from a master host controller such as a PC.

The having processed data coming from Baseband & Logic is fed to a D/A converter, then to a digital baseband transmit filter which provides the required spectral shaping. A multiplier plays a role of direct I/Q modulator to fulfill GFSK modulation with a controlled modulation index. The chip built-in PA has a maximum output power of +4dBm allowing transmitter to meet Bluetooth Class 2 without using external PA. The RF Synthesizer has been integrated into the chip set so that there is no need to add external components such as VCO (Voltage Controlled Oscillator), tuning diode but a simple RC loop filter. Frequency Hopping function is done through RF Synthesizer too.

The PA output from the chip set is differential to reduce common mode noise. An external Balun transformer converts the differential to single ended signal which then passes through a BPF (Band Pass Filter) blocking all unwanted out of band emissions.

Receiver Path

The receiver path is basically a reverse process to transmitter. The off air signal passes through BPF and Balun to a chip built-in LNA (Low Noise Amplifier). A receive multiplier down converts the channel signal to a near-zero IF (Intermediate Frequency) which is then filtered out and fed to a FSK discriminator. The data stream coming out from the discriminator goes to the Baseband & Logic for further processing. This architecture allows the filters to be integrated into the chip set. Sufficient out of band blocking specification at LNA input allows the radio to be used in close proximity to GSM Mobile Communications and WCDMA cellular phone transmitters without being interfered. The excellent performance in the noise presence of Actiontec BTM200B allows the system to exceed the Bluetooth requirements for co-channel and adjacent channel rejection.

A RSSI (Received Signal Strength Indication) line is internally hooked up to an A/D converter. This constructs a part of AGC loop for the receiver. The rest of the circuitry is within the Baseband & Logic and comes back to the gain control of the LNA.

Microcontroller, Baseband & Logic

The microcontroller, interrupt controller and event timer run the Bluetooth software stack, which is loaded in a 8Mbit flash, and control the radio and host interfaces. Two terminals of the Programmable I/O ports are currently used for LED indication.

The Memory Management Unit (MMU) provides a number of dynamically allocated ring buffers that hold the data which is in transit between the host and the air or vice versa. The dynamic allocation of memory ensures efficient use of the available RAM and is performed by a hardware MMU to minimize the overheads on the processor during data transfer.

The Physical Layer Hardware Engine DSP is dedicated to perform: Forward error correction, Header error control, Cyclic redundancy check, Encryption, Data whitening, Access code correlation and Audio transcoding.

During radio transmission, Burst Mode Controller (BMC) constructs a packet from header information previously loaded into memory-mapped registers by the software and payload data/voice taken from the appropriate ring buffer in RAM. During radio reception, the BMC stores the packet header in memory-mapped registers and the payload data in the appropriate ring buffer in RAM. This architecture minimizes the intervention required by the processor during transmission and reception.

Device Diagram