Basic Operation Principle of 802PI25

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Description

The Wireless LAN of 802pi25 is a 2.4GHz ISM Band DSSS Radio. It is designed to operate using IEEE 802.11b WLAN Standard for use in wireless networking systems. The Radio consists of 5 major ICs, which are ISL3685, HFA3783, ISL3984, ISL3874A, ISL3183 and few support ICs. It operates at maximum transmit rate 11Mb/s, back off rates 5.5, 2 and 1 Mb/s. The modulation schemes include CCK (Complementary Code Keying), DQPSK and DBPSK depending on what transmit bit rate it operates at. The radio card interfaces to PC through a MiniPCI bus.

Main Chips

ISL3874A:	Intersil, Wireless LAN integrated Medium Access Controller with Baseband Processor
HFA3783:	Intersil, I/Q Modulator/Demodulator and Synthesizer
ISL3183:	Intersil, 748MHz Voltage Controlled Oscillator
ISL3685:	Intersil, 2.4GHz RF/IF Converter and Synthesizer
ISL3984:	Intersil, 2.4GHz Power Amp and Detector

Host Interface

The host interface on the 802pi25 is designed specifically for Mini PCI applications. It consists of 32 bits of address and data, as well as all the required Mini PCI control signals. The chip supports the 3.3V signaling environment, with clock speeds up to 33 MHz. Most of the host interface signals are bi-directional. The output slew rates of the signals on 802pi25 have been designed to comply with the Mini PCI Specification, revision 1.0, October 25th 1999.
Refer to the standard for a functional description of the Mini PCI signals.

Flash

A 128K * 8 bits flash chip from SST on the 802pi25. It is used to store the program for the onboard processor. Right after power on, the program will download from flash to SRAM, then the processor execute the program from the SRAM.

SRAM

A 128K * 16 bits SRAM on the 802pi25. It is used for program downloaded from Flash chip as well as storage buffer for the receiving and transmitting data packet.

External LED

There is 3 LED status. Once power apply to 802pi25, LED3 will be on. LED1 is used to indicate LINK status; LED2 is used to indicate ACTIVITY status, such as receiving and transmitting.

The LED signal go through Mini PCI connector to the host.

44MHz Oscillator

The 44MHz oscillator provides almost all the clock for 802pi25. The 44MHz clock is fed into ISL3874 (MAC/BBP), ISL3685 (RF/IF Converter) and HFA3783 (IQ Modem/Synthesizer).

For ISL3874, the 44MHz clock is required for the processor to run the program and other circuitry.

In ISL3685, the 44MHz clock is used for the internal phase lock loop to keep track the RF frequency from the RF VCO.

In HFA3783, the 44MHz clock is used for the internal phase lock loop to keep track the RF frequency from the IF VCO.

44MHz

32KHz Crystal

There is a 32KHz crystal connected to ISL3874 chip. The 32KHz clock will only be used in power saving mode.

During power saving mode, the 44MHz oscillator will be turned off, and 32KHz will provide clock for the processor in ISL3874. Therefore, minimum of current would be used.

RF Connector

There are two RF antenna connectors (J1 & J2) onboard to connect to the antenna in the notebook. J1 is to connect to Main antenna; J2 is to connect to Aux. antenna.

Main antenna is used for transmitting and receiving while Aux. antenna is for receiving only.

Transmitter Path

The Ethernet data comes through the MiniPCI interface, the Host I/O interface to the MAC section of ISL3874. The signal then flows into the data router where it is converted from Ethernet to 802.11b protocol. After the signal is converted, a radio preamble and header is added to it and passed to the I/O of BBP (Base Band Processor) section of ISL3874 via PHY I/O, RADIO I/O. There is also support circuitry, such as outboard SRAM and flash ROM, which contains the firmware controlling the radio.

In TX modulator of BBP section, differential phase shift keying modulation schemes DBPSK, DQPSK and CCK, with data scrambling capability, are fulfilled to provide a variety of data rates--DBPSK for 1 Mb/s, DQPSK for 2 Mb/s and CCK for 5.5 and 11Mb/s. The signal, which now is two separate quadrature components I and Q, then flows to the quad IF chip HFA3783 through D/A converters.

At TX side of BBP, there is also TX ALC (Automatic Level Control) circuitry, which is part of the TX ALC loop. The loop keeps TX output power to be consistent so that prevent the power spectrum from regrowth.

HFA3783 is now the dual up conversion mixers (dual down conversion mixers for RX). The signal upconverts to an IF frequency of 374 MHz and passes into a variable gain amplifier, which is also a part of the ALC loop. Next, it passes through the switched TX/RX shared SAW filter into ISL3685 and then upconverts again to a RF frequency from 2.412~2.484 GHz, depending on the channel selection. The signal flows through a pre-amplifier, two band pass filters, which block all the unwanted emissions such as image components, harmonics and spurious stuff, into ISL3984 power amplifier. The output of the power amplifier is then fed through another band pass filter that is about 85 MHz bandwidth to one of the antennas.

Receiver Path

The receive signal traveling through the air is received by the dual diversity antennas. The circuits will switch to the antenna which provides better RSSI (Received Signal Strength Indication). The RF signal then feeds into an 85 MHz band pass filter, which blocks all the unwanted components such as image frequency. The signal again is amplified using the LNA within ISL3685 and mixed down to the IF frequency of 374 MHz. The PLL and synthesizer select the channel frequency using Low Side Injection. The mixer outputs are then fed through the IF SAW filter that provides image rejection into HFA3783, which is now a quad down converter. HFA3783 also provides RSSI to BBP of ISL3874. There is a two stage analog AGC (Automatic Gain Control) circuit which adjusts the gain to compensate the signal strength differences. The output of the twin AGC's provides a constant level signal to the I and Q down converters, which convert the IF to both I and Q signals to BBP. A second frequency synthesizer, which uses ISL3183 as its VCO, feeds the I and Q mixers with a same frequency signal that is phase shifted by 90° .

The I and Q signals that are fed into BBP of ISL3874 are converted into digital signals via a dual A/D converters then flow through the digital AGC control circuit followed by the digital demodulator. The correlation codes that BBP generates properly detect the transmitted complimentary codes. In here the automatic antenna selection is also done by taking RSSI as the reference. The output of the digital demodulator is sent into an I/O interface of MAC section. The digital codes then flow into the PHY I/O interface and into the MAC protocol engine. The MAC of ISL3874 converts the signal protocol from 802.11b to Ethernet and finally passes that data through the HOST I/O interface to the PC.

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