Hope Technology Inc.

HPC3129 Preliminary Datasheet

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Application Information

This document is designed for datasheet of HPC3129 chipset, approved to be released to and used by customers.

To obtain the most updated Application Notes and other useful information for your design, contact your local Hope sales office. Please also visit the Hope web site at www.hopemicro.com

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1 Overview

The HPC3129 is an integrated system-on-chip application processor, which is designed to provide a low power and high performance multimedia solution for wireless monitor and CE market, such as Baby Monitor and hand-held devices. The HPC3129 is based on H-CORE, including a 32bit RISC processor with the addition of dedicated SIMD accelerator.

The HPC3129 provides the high quality on-chip audio codec features, including 24bit stereo DAC and 24bit stereo ADC.

The HPC3129 integrates many widely used multimedia processing functions for a simple and quick system integration, which include AMR codec, MP3 codec, WMA decoder, AAC codec, AAC+ decoder, OGG decoder, JPEG codec, MPEG4 and H.263 codec, H.264 codec etc.

The HPC3129 also integrates a wireless communication baseband controller, named as HMAC, which could transmit or receive serial data to or from RF module. HMAC can easily interface with many popular RF transceivers, such as A7121(AMICCOM®). HECC, a wireless communication error correction controller, is also included, which consists of CRC generator, RS encoder and RS decoder. So the HPC3129 is preferred for wireless multimedia applications.

A large variety of peripherals and interfaces such as CAMERA, LCD, I^2C, I2S, SDRAM, NAND Flash, ATA, SD/MMC/T-Flash, UART, SPI, Keypad, etc. provide the maximum flexibility and efficiency for building application systems.

Main features of the HPC3129 are as follows:

- Architecture: based on H-CORE, including a 32bit RISC processor with the addition of dedicated 128-bit SIMD accelerator
- 193-Pin BGA package
- Input image resolution up to (4096x4096) pixels
- Support asynchronous MPU interface(80 type) LCD, support synchronous RGB LCD, and support variable display window size and OSD up to 1024x1024
- Microphone input(single end)
- High performance headphone driver
- Stereo line input
- H-CORE based software supports main stream audio formats, such as MP3, AAC, AAC+, AMR NB, AMR WB, WMA, SBC, OGG, APE
- SIMD based video decoder software supports main stream video formats, such as MPEG2, MPEG4/H.263, VC1, REAL VIDEO with performance up to D1@30fps
- SIMD based JPEG codec supports encoder size up to 128M and decoder size up to 128M pixels
- SIMD based video encoder software supports MPEG4 format with performance up to D1@30fps
- Hardware H.264 codec supports H.264 format with performance up to D1@30fps
- Support 16 bit or 32 bit data bus SDRAM or SRAM
- Support up to two NAND devices, support up to 20 bit ECC by hardware BCH ECC accelerator

- Support ATA-PIO mode 4 and UDMA-4
- Support SD memory card physical layer specification 2.0
- HMAC controller easy to interface with many popular RF transceivers
- Including hardware HECC controller for wireless front error correction to improve RF performance
- Related Video DAC integrated on chip, support for TV OUT up to D1 resolution
- 2-channel single-ended 10-bit Successive Approximation Register (SAR) analog-to-digital converter(ADC)
- Support up to an 4x4 external key pad matrix
- With RTC function
- Providing programmable clock out
- With a large variety of interfaces such as I2C, I2S, SPI, UART, PWM, GPIO etc.

2 Applications

- Baby Monitor
- Home Security
- PMP
- PDA
- GPS Navigator
- Wireless Video Doorbell
- Wireless Surveillance System
- Photo Frame
- DVR
- DSC/DV

3 Function block diagram

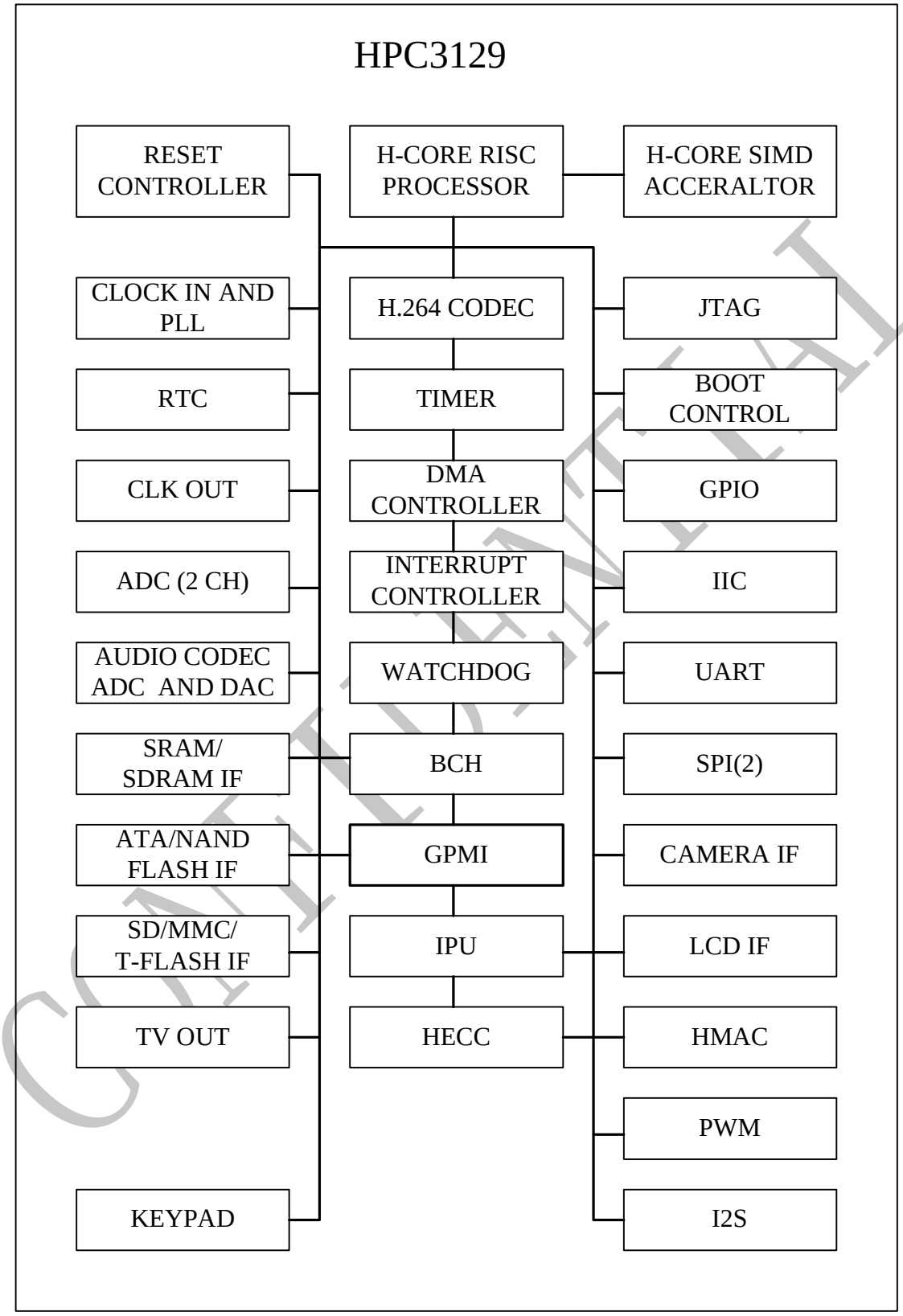

FIGURE 3-1 HPC3129 function block diagram

4 Feature sets

4.1 General features

- Architecture: based on H-CORE, including a 32bit RISC processor with the addition of dedicated SIMD accelerator
- Embedded 32-bit RISC MCU with 32Kbyte instruction cache and 32Kbyte data cache to reach high performance and lower bus-loading occupation
- 128-bit SIMD accelerator
- On-chip crystal oscillator with frequency of 24MHz
- On-chip crystal oscillator with frequency of 32.768KHz
- Providing power on reset for chip and system
- Providing programmable clock out
- 193-Pin BGA package

4.2 IPU unit

4.2.1 Image sensor interface

- Input image resolution up to (4096x4096) pixels
- Support CCIR656/CCIR601 compliant 8-bit input interface with YUV422
- Programmable AC timing parameter to support different sensors
- Image data from sensor can be trimmed and scaled for preview or capture
- Support preview image frame rate up to 30fps under (4096x4096)pixels

4.2.2 Display interface

- Support asynchronous MPU interface(80 type) LCD
- Support synchronous RGB LCD
- Support 12/16/18/24 bit color STN/UFB/TFT and OLED panels
- Configurable AC timing for support variable LCD
- Support variable display window size and OSD up to 1024x1024
- Support CCIR656 interface for TV encoder, support for both NTSC and PAL

4.3 Video codec and JPEG codec

- SIMD based video decoder software supports main stream video formats, such as MPEG2, MPEG4/H.263, VC1, REAL VIDEO with performance up to D1@30fps
- SIMD based JPEG codec supports encoder size up to 128M and decoder size up to 128M pixels
- SIMD based video encoder software supports MPEG4 format with performance up to D1@30fps
- Hardware H.264 codec supports H.264 format with performance up to D1@30fps

4.4 Audio codec

- 24 bit multi-bit sigma delta ADC and DAC
- ADC SNR 90dB(A weighted); DAC SNR 100dB(A weighted)
- Microphone input(single end)

- High performance headphone driver
- Stereo line input
- H-CORE based software support main stream audio formats, such as MP3, AAC, AAC+, AMR NB, AMR WB, WMA, SBC, OGG, APE

4.5 Game engine

- Support GBA game
- Support FC emulator

4.6 Memory interface

- GPMI interface(only work in NAND flash or ATA mode by software select)
  - NAND flash interface
    - Support SLC and MLC NAND Flash
    - Support 8 bit data bus
    - Support up to two NAND devices
    - Support up to 20 bit ECC by hardware BCH ECC accelerator
  - ATA interface
    - Support ATA-PIO mode 4 and UDMA-4
    - Support all basic ATA operations
    - Support Compact-Flash devices configured for True IDE mode
- SDRAM/SRAM controller
  - Support 16 bit or 32 bit data bus
  - Support memory size from 8MB to 256MB SDRAM
- SD card interface
  - Support SD memory card physical layer specification 2.0
  - Support SD/MMC/T-FLASH
  - Support SDHC
  - Support SDIO device
  - Compliant with SD memory card physical layer specification 1.10
  - Support Multimedia card specification 2.11

4.7 RTC

- Real time counter to support YEAR/MONTH/DAY/HOUR/MINUTE/SECOND

4.8 HMAC interface

- Responsible for transmitting or receiving data to or from RF module
- Half-duplex transmitter and receiver
- Data bit rate: 1Mbps, 3 Mbps and 6 Mbps
- A7121 digital interface support
- A7121 direct mode and FIFO mode compatible
- Easy to interface with many popular RF transceivers
- Including hardware HECC controller for wireless front error correction to improve RF performance

4.9 TV encoder (Embedded Video DAC)

- Related Video DAC integrated on chip
- Support for TV OUT up to D1 resolution
- Support CCIR656 interface for TV encoder, support for both NTSC and PAL

4.10 I2S interface

- Support I2S bus specification(Philips Semiconductor 1996)
- Support master and slave mode with DMA channel
- Connecting with internal audio codec as I2S slave
- Full duplex communication due to the independence of transmitter and receiver
- Audio data resolutions of 12, 16, 20, 24, and 32 bits
- Standard I2S stereo frame format

4.11 ADC

- 2-channel single-ended 10-bit Successive Approximation Register (SAR) analog-to-digital converter

4.12 I2C interface

- Philips I2C standard compliant
- Support stand mode(100Kbps), fast mode(400Kbps) and high-speed mode(3.4Mbps)
- 7- or 10-bit addressing
- Master or slave I2C operation

4.13 SPI interface

- 2 sets of 4-wire SPI interface
- Support master and slave mode with DMA channel

4.14 UART

- 1 set of 2-wire serial port
- Support standard baud rate from 9.6Kbps to 460.8Kbps, extendable up to 920Kbps for Bluetooth application
- Support data transfer with DMA channel

4.15 KEYPAD

- Support up to an 4x4 external key pad matrix
- Port pins can be used as general purpose I/O
- Multiple-key detection
- Long key-press detection
- Hardware de-bounce function
- Support interrupt to CPU

4.16 GPIO

- Up to 101 GPIO, all of them shared with other functions, except 3 independent GPIO
- Support interrupt to CPU

- Hardware de-bounce function
- 1 GPIO with PWM function for LCD backlight or motor control

4.17 PWM

- PWM function for LCD backlight or motor control

7 Interface description and timing

7.1 IPU unit

IPU unit performs the following functions: capturing image data from a camera sensor or from a TV decoder; preprocessing of data from the sensor or from the external system memory; postprocessing of data from the external system memory; post-filtering of data from the system memory with support of the MPEG-4 (both deblocking and deringing) and H.264 postfiltering algorithms; displaying video and graphics on a synchronous (dump or memory-less) display; displaying video and graphics on an asynchronous (smart) display; displaying video and graphics on a TV (through a TV encoder).

IPU unit includes image sensor interface and display interface, and supports CCIR656 interface for TV encoder (both NTSC and PAL).

7.1.1 Image sensor interface

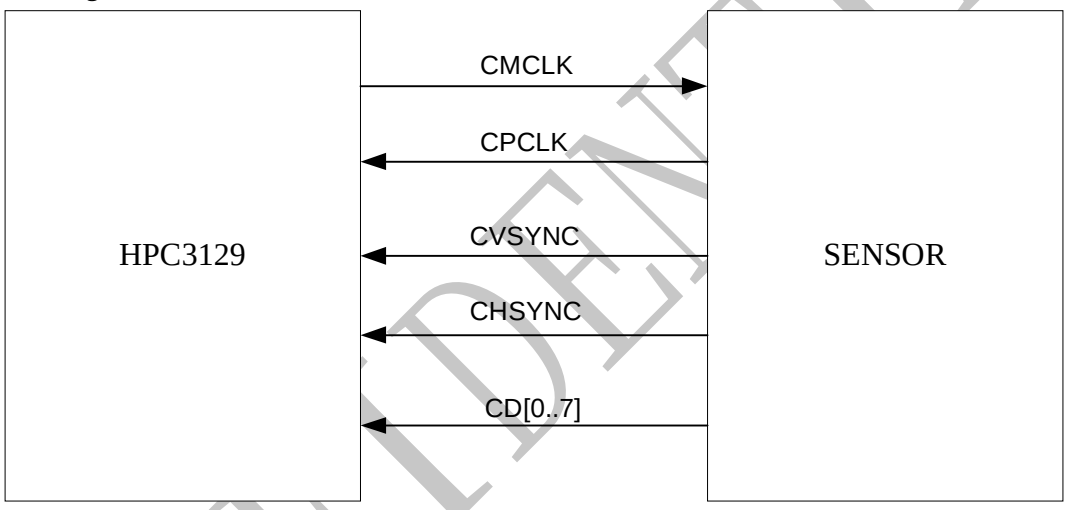

Figure 7-1 Image sensor interface diagram

There are three timing modes supported by image sensor interface.

7.1.1.1 Pseudo BT.656 video mode

This operation mode follows the recommendations of ITU BT.656 specifications.

7.1.1.2 Gated clock mode

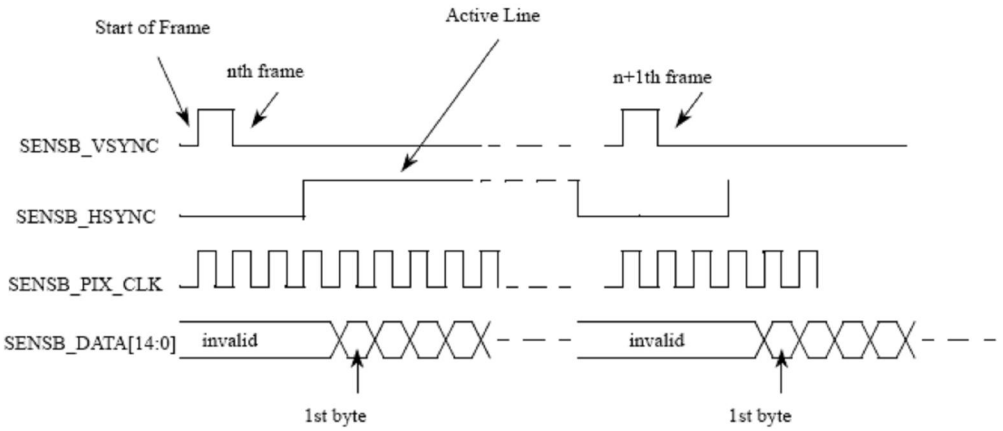

Figure 7-2 Gated clock mode timing diagram

7.1.1.3 Non-gated clock mode

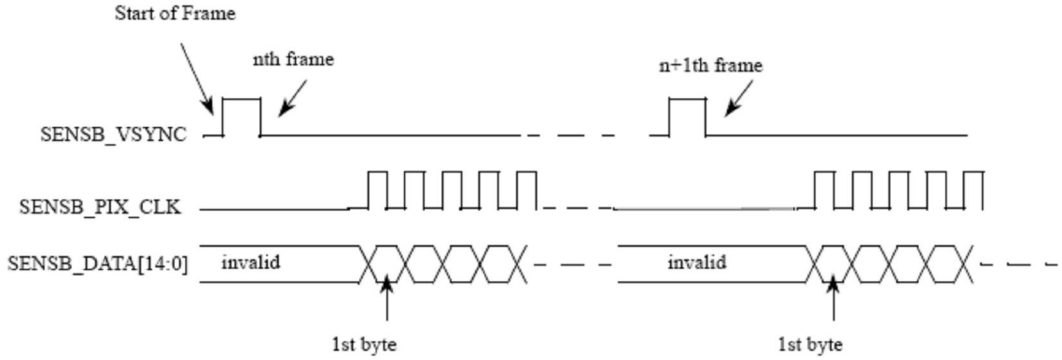

Figure 7-3 Non-gated clock mode timing diagram

7.1.1.4 Timing

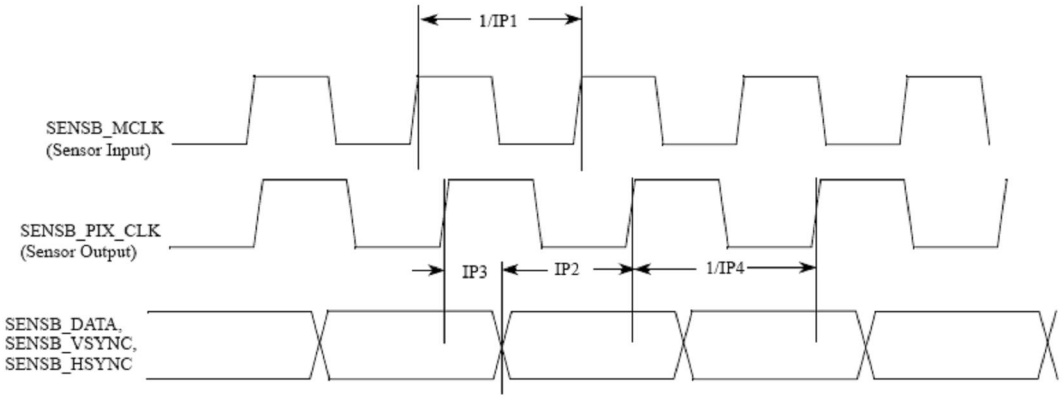

Figure 7-4 Sensor interface timing diagram

Table 7-1 Sensor interface timing characteristics

ID	Parameter	Symbol	Min.	Max.	Units
IP1	Sensor input clock frequency	Fmck	0.01	73	MHz
IP2	Data and control setup time	Tsu	5		ns
IP3	Data and control holdup time	Thd	3		ns
IP4	Sensor output (pixel) clock frequency	Fpck	0.01	73	MHz

7.1.2 Display interface

Display interface can support asynchronous MPU interface(80 type) LCD and synchronous RGB LCD.

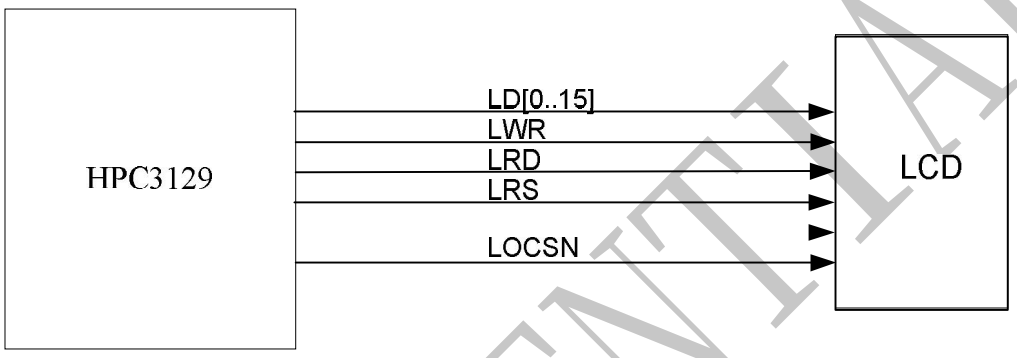

Figure 7-5 MPU type(80 type) LCD interface diagram

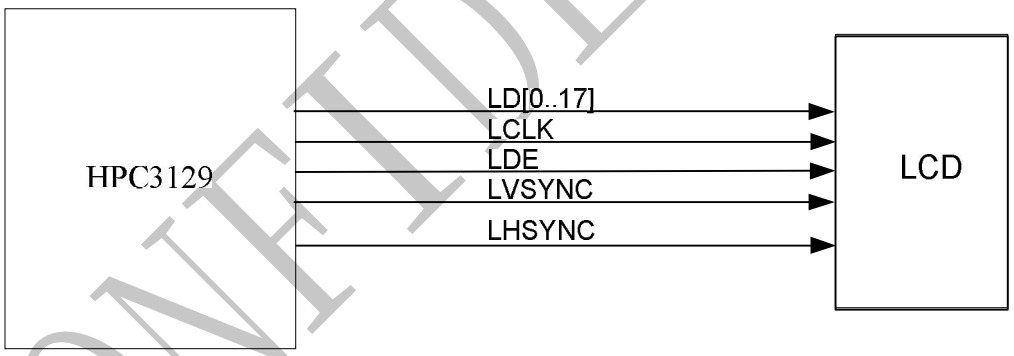

Figure 7-6 Synchronous RGB LCD interface diagram

MPU type LCD timing:

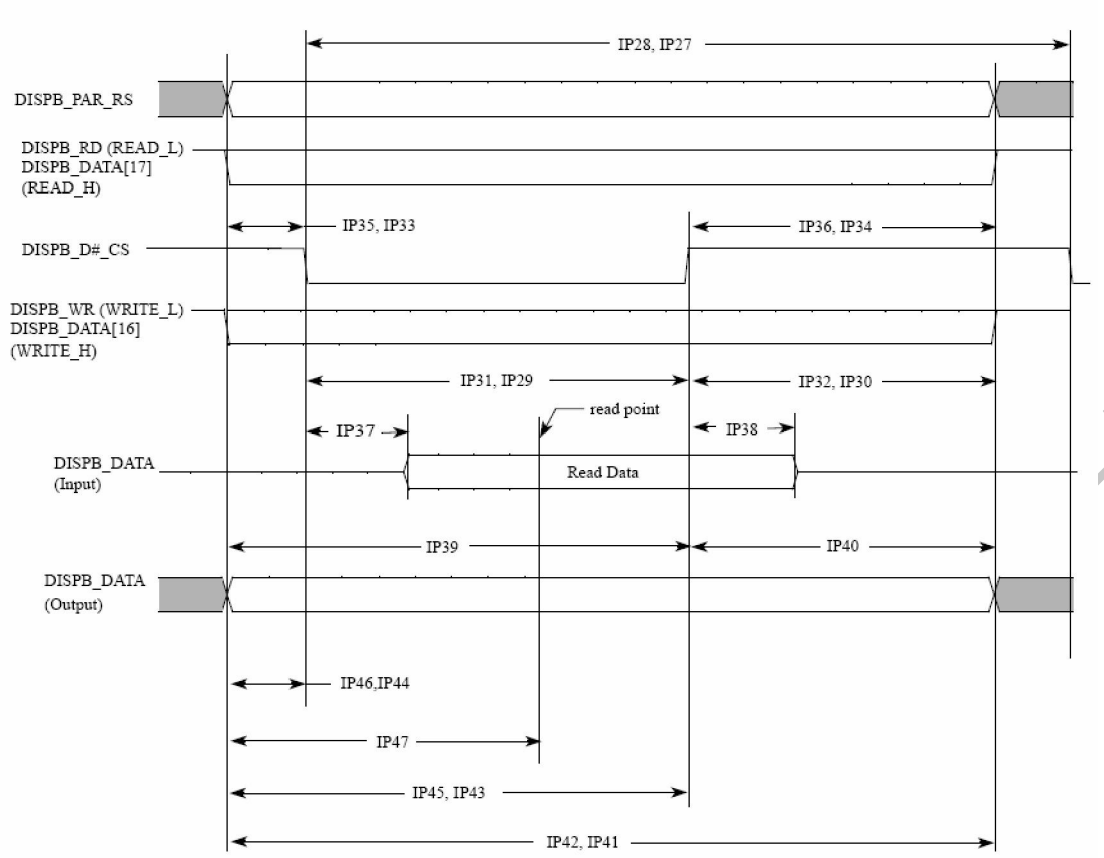

Figure 7-7 Asynchronous parallel system 80 interface (type 1) timing diagram

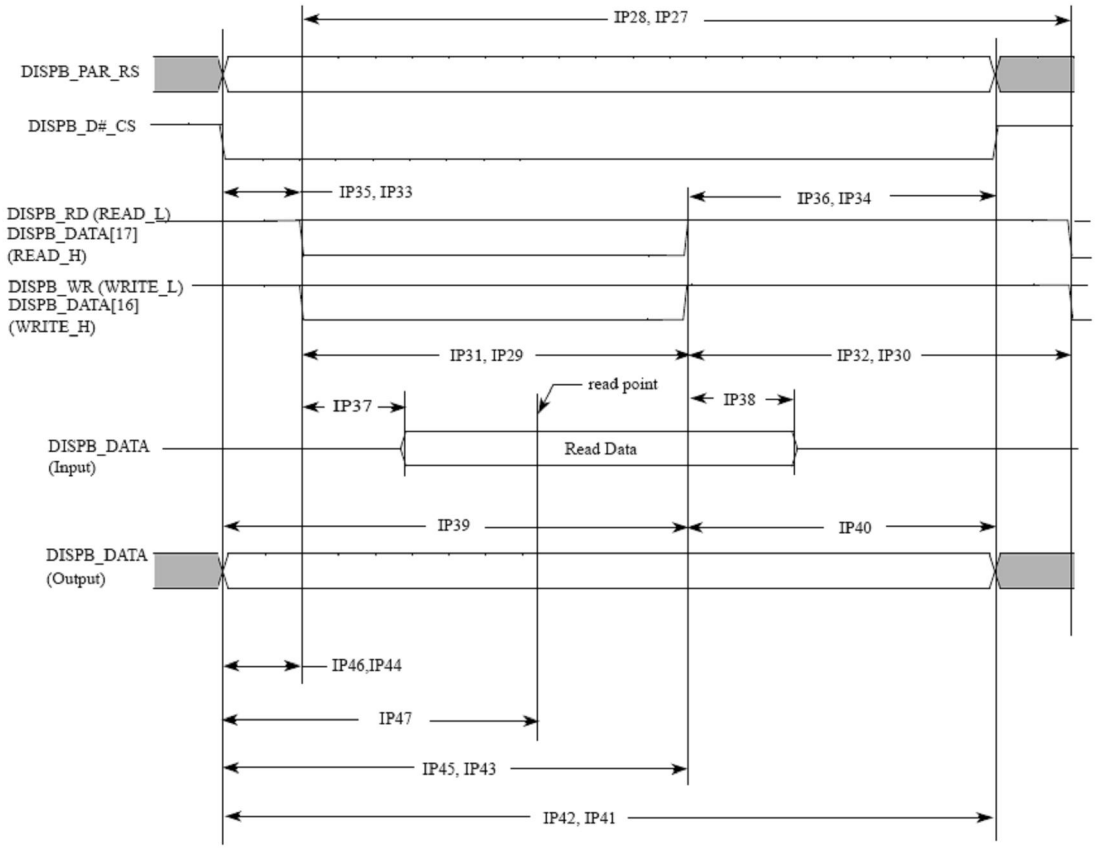

Figure 7-8. Asynchronous parallel system 80 interface (type 2) timing diagram

Table 7-2 Asynchronous parallel interface timing characteristics

ID	Parameter	Symbol	Min.	Typ.[1]	Max.	Units
IP27	Read system cycle time	Tcycr	Tdicpr-1.5	Tdicpr[2]	Tdicpr+1.5	ns
IP28	Write system cycle time	Tcycw	Tdicpw-1.5	Tdicpw[3]	Tdicpw+1.5	ns
IP29	Read low pulse width	Trl	Tdicdr-Tdicur-1.5	Tdicdr[4]-Tdicur[5]	Tdicdr-Tdicur+1.5	ns
IP30	Read high pulse width	Trh	Tdicpr-Tdicdr+Tdicur-1.5	Tdicpr-Tdicdr+ Tdicur	Tdicpr-Tdicdr+Tdicur+1.5	ns
IP31	Write low pulse width	Twl	Tdicdw-Tdicuw-1.5	Tdicdw[6]-Tdicuw[7]	Tdicdw-Tdicuw+1.5	ns
IP32	Write high pulse width	Twh	Tdicpw-Tdicdw+ Tdicuw-1.5	Tdicpw-Tdicdw+ Tdicuw	Tdicpw-Tdicdw+ Tdicuw+1.5	ns
IP33	Controls setup time for read	Tdcsr	Tdicur-1.5	Tdicur		ns

ID	Parameter	Symbol	Min.	Typ.[1]	Max.	Units
IP34	Controls hold time for read	Tdchr	Tdicpr-Tdicdr-1.5	Tdicpr-Tdicdr		ns
IP35	Controls setup time for write	Tdcsw	Tdicuw-1.5	Tdicuw		ns
IP36	Controls hold time for write	Tdchw	Tdicpw-Tdicdw-1.5	Tdicpw-Tdicdw		ns
IP37	Slave device data delay[8]	Tracc	0		Tdrp[9]-Tlbd[10]-Tdicur-1.5	ns
IP38	Slave device data hold time[8]	Troh	Tdrp-Tlbd-Tdicdr+1.5		Tdicpr-Tdicdr-1.5	ns
IP39	Write data setup time	Tds	Tdicdw-1.5	Tdicdw		ns
IP40	Write data hold time	Tdh	Tdicpw-Tdicdw-1.5	Tdicpw-Tdicdw		ns
IP41	Read period[2]	Tdicpr	Tdicpr-1.5	Tdicpr	Tdicpr+1.5	ns
IP42	Write period[3]	Tdicpw	Tdicpw-1.5	Tdicpw	Tdicpw+1.5	ns
IP43	Read down time[4]	Tdicdr	Tdicdr-1.5	Tdicdr	Tdicdr+1.5	ns
IP44	Read up time[5]	Tdicur	Tdicur-1.5	Tdicur	Tdicur+1.5	ns
IP45	Write down time[6]	Tdicdw	Tdicdw-1.5	Tdicdw	Tdicdw+1.5	ns
IP46	Write up time[7]	Tdicuw	Tdicuw-1.5	Tdicuw	Tdicuw+1.5	ns
IP47	Read time point[9]	Tdrp	Tdrp-1.5	Tdrp	Tdrp+1.5	ns

Note:

1 The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be chip specific.

2 Display interface clock period value for read.

3 Display interface clock period value for write.

4 Display interface clock down time for read.

5 Display interface clock up time for read.

6 Display interface clock down time for write.

7 Display interface clock up time for write.

8 This parameter is a requirement to the display connected to the IPU.

9 Data read point.

10 Loopback delay.

Synchronous RGB LCD interface timing:

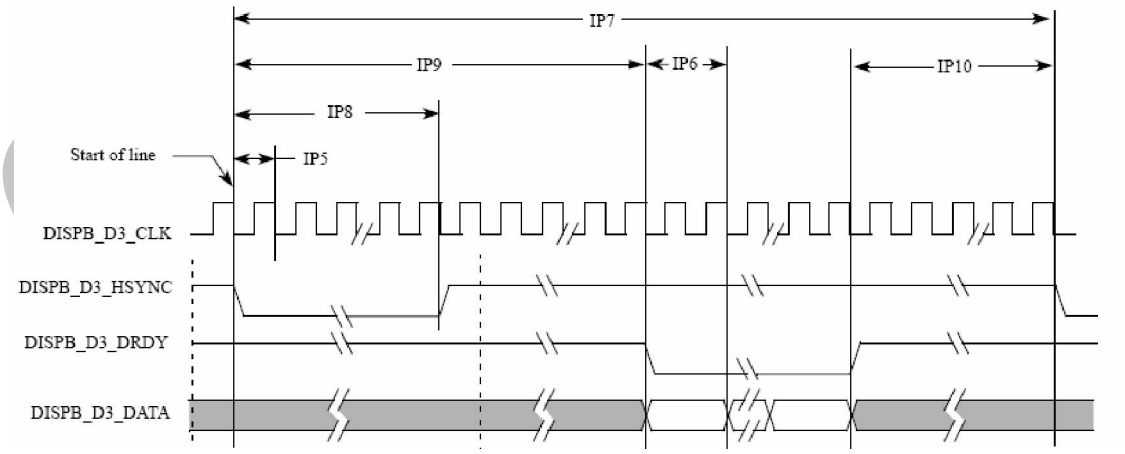

Figure 7-9. TFT Panels Timing Diagram—Horizontal Sync Pulse

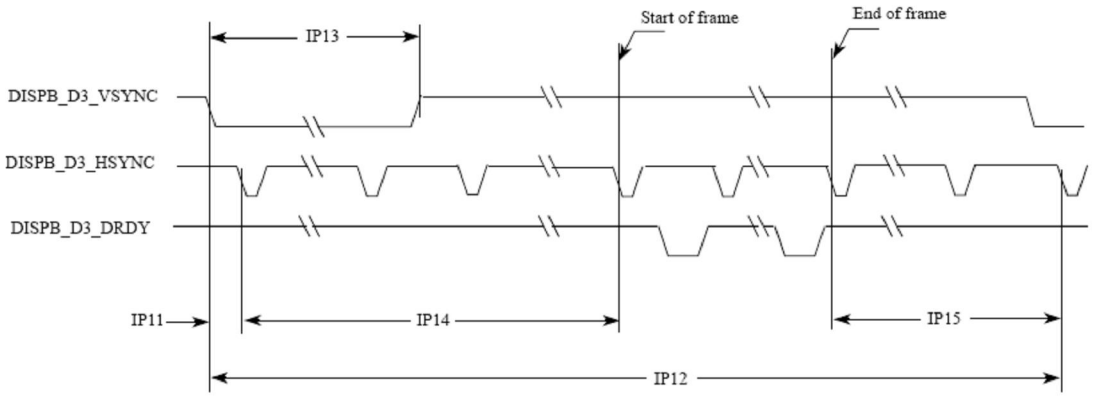

Figure 7-10 TFT Panels Timing Diagram—Vertical Sync Pulse

Table 7-3 Synchronous Display Interface Timing Characteristics (Pixel Level)

ID	Parameter	Symbol	Value	Units
IP5	Display interface clock period	Tdicp	(1)	ns
IP6	Display pixel clock period	Tdpcp	(DISP3_IF_CLK_CNT_D+1) * Tdicp	ns
IP7	Screen width	Tsw	(SCREEN_WIDTH+1) * Tdpcp	ns

ID	Parameter	Symbol	Value	Units
IP8	HSYNC width	Thsw	(H_SYNC_WIDTH+1) * Tdpcp	ns
IP9	Horizontal blank interval 1	Thbi1	BGXP * Tdpcp	ns
IP10	Horizontal blank interval 2	Thbi2	(SCREEN_WIDTH - BGXP - FW) * Tdpcp	ns
IP11	HSYNC delay	Thsd	H_SYNC_DELAY * Tdpcp	ns
IP12	Screen height	Tsh	(SCREEN_HEIGHT+1) * Tsw	ns
IP13	VSYNC width	Tvsw	if V_SYNC_WIDTH_L = 0 than (V_SYNC_WIDTH+1) * Tdpcp else (V_SYNC_WIDTH+1) * Tsw	ns
IP14	Vertical blank interval 1	Tvbi1	BGYP * Tsw	ns
IP15	Vertical blank interval 2	Tvbi2	(SCREEN_HEIGHT - BGYP - FH) * Tsw	ns

1 Display interface clock period immediate value.

7.2 Memory interface

7.2.1 GPMI interface

The general-purpose media interface (GPMI) controller is a flexible interface to an ATA device or up to two NAND flash.

7.2.1.1 NAND flash interface

NAND flash interface supports up to 20 bit ECC by hardware BCH ECC accelerator

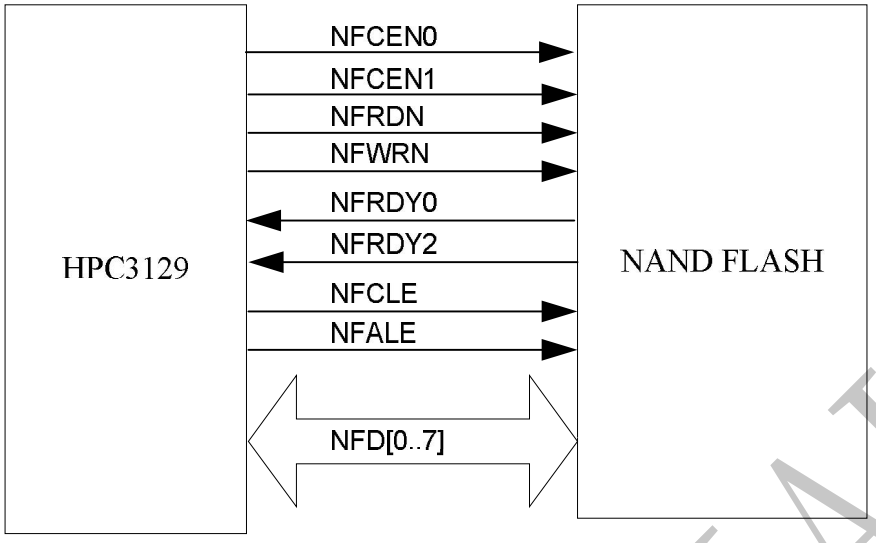

Figure 7-11 NAND flash interface diagram

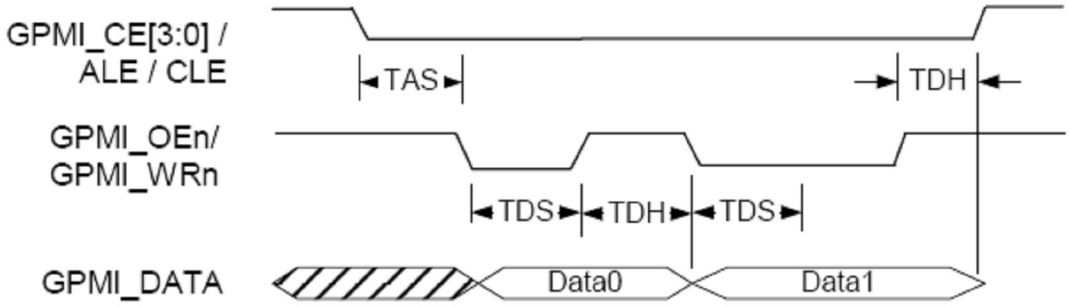

Figure 7-12 NAND flash basic timing diagram

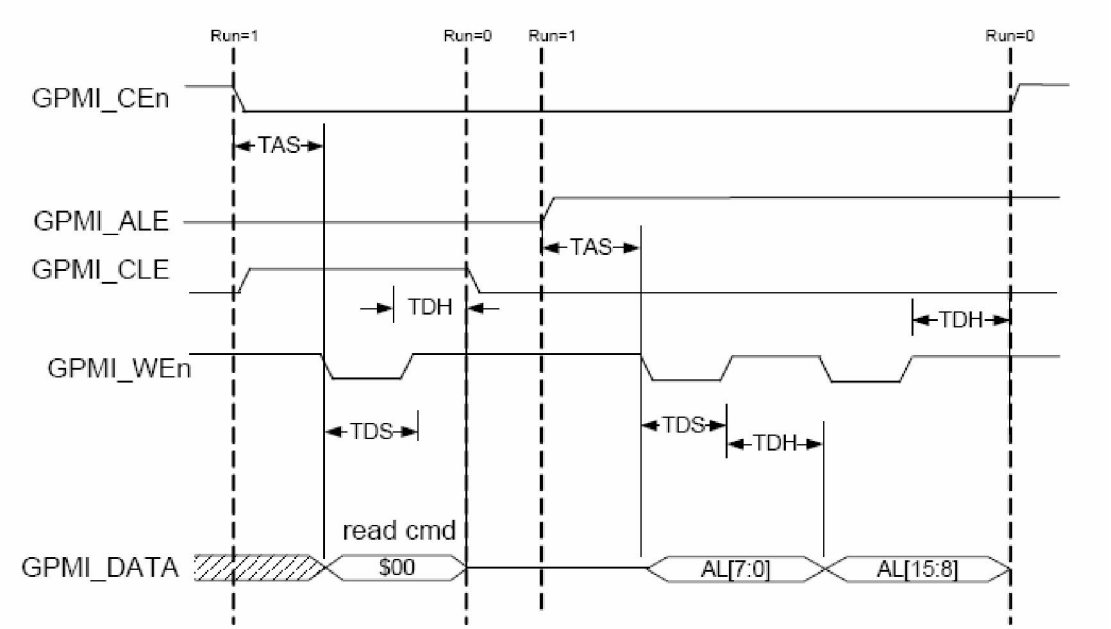

Figure 7-13 NAND flash command and address timing diagram

7.2.1.2 ATA interface

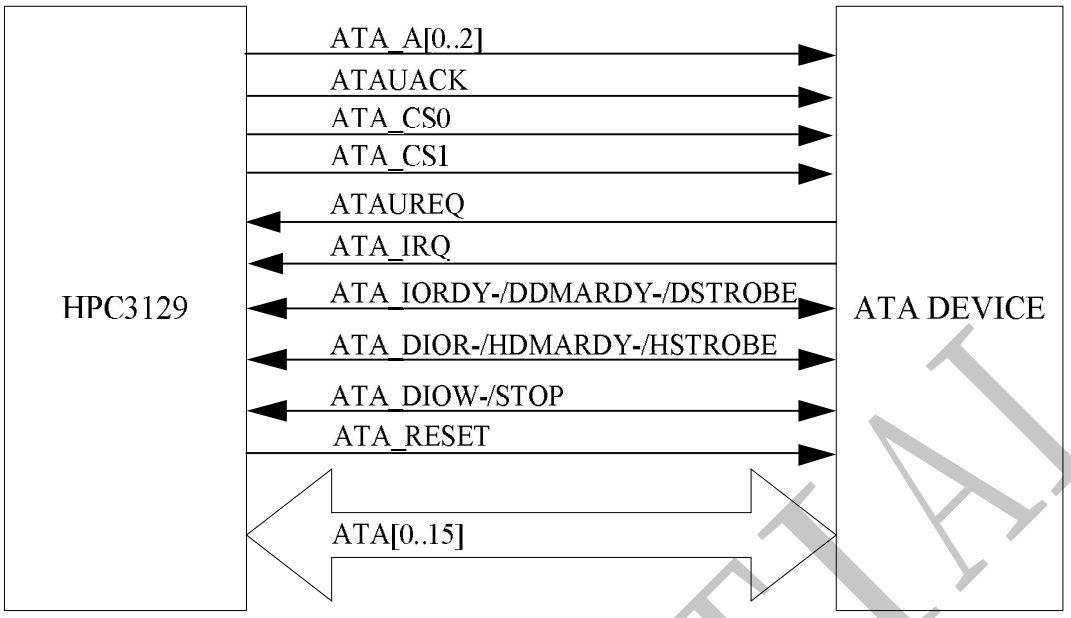

Figure 7-14 ATA interface diagram

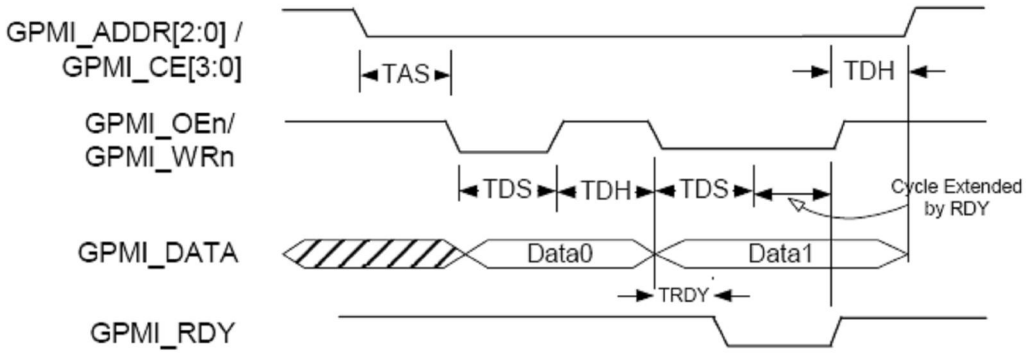

Figure 7-15 ATA PIO mode timing diagram

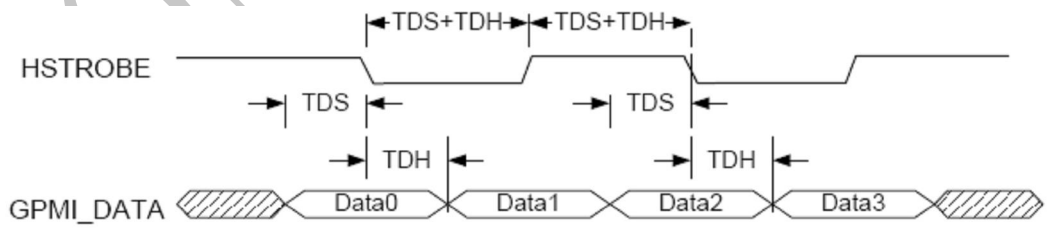

Figure 7-16 ATA UDMA data write mode timing diagram

Please refer to ATA specification for detailed timings.

7.2.2 SDRAM/SRAM interface

SDRAM/SRAM controller supports 16 bit or 32 bit SDRAM and mobile SDRAM or

SRAM.

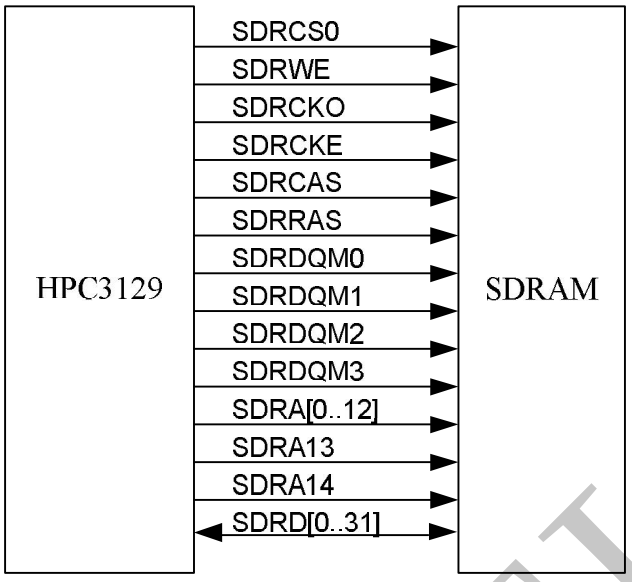

Figure 7-17 SDRAM interface diagram

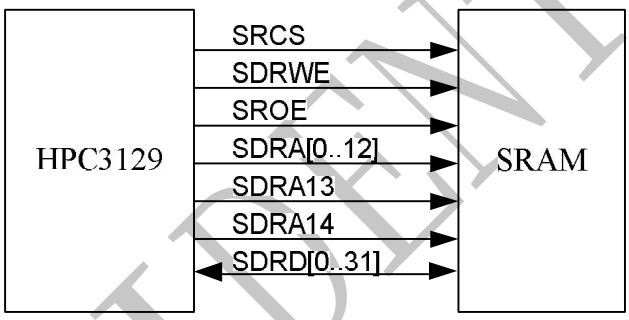

Figure 7-18 SRAM interface diagram

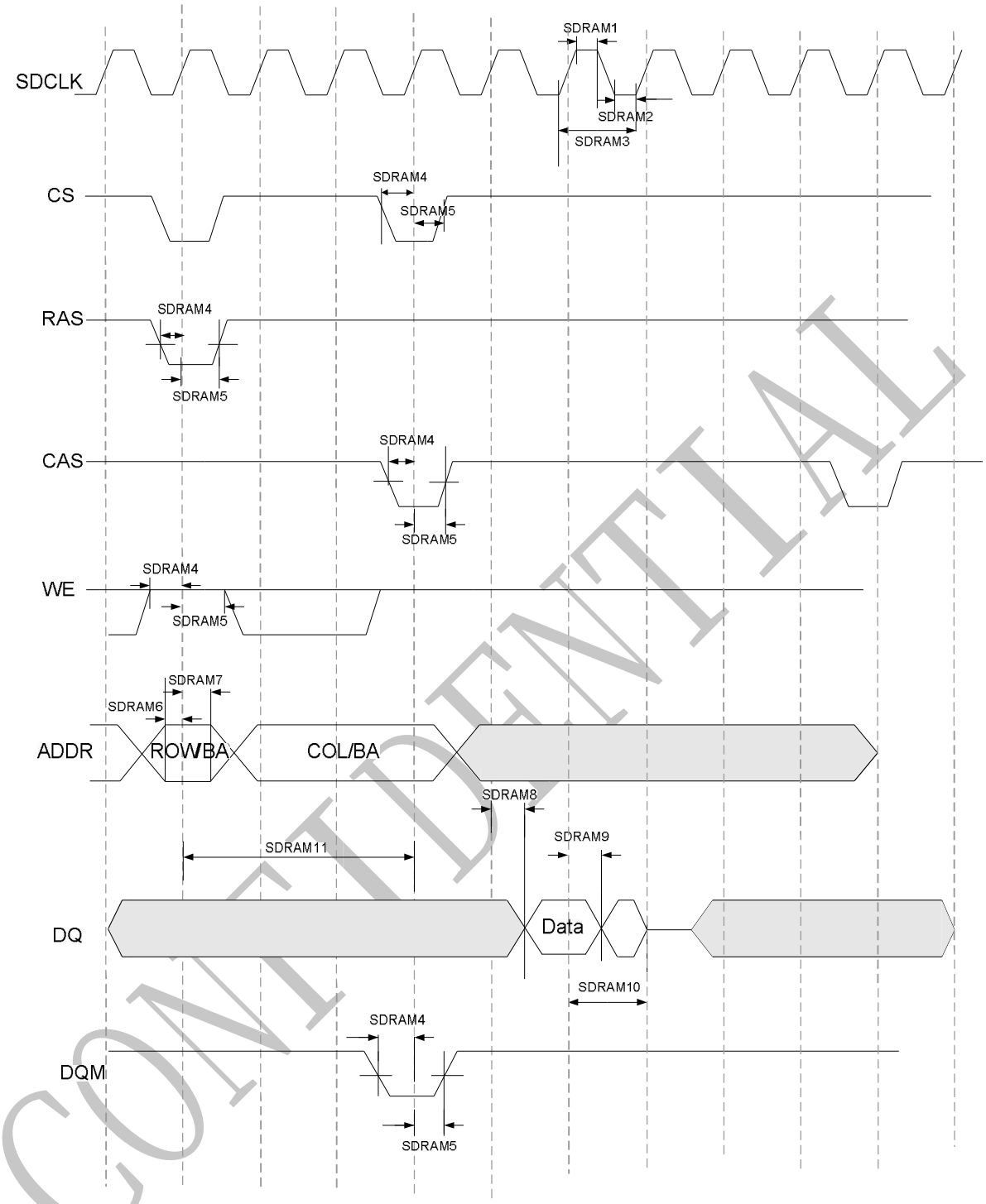

Figure 7-19 SDRAM interface read timing diagram

Table 7-4 AC timing parameter of read cycle

ID	Parameter	Symbol	Min	Max	Unit
SDRAM1	SDRAM clock high	tCH	TBD	-	ns
SDRAM2	SDRAM clock low	tCL	TBD	-	ns
SDRAM3	SDRAM clock cycle	tCLK	TBD	-	ns
SDRAM4	CS,RAS,CAS,WE,DQM	tSU	TBD	-	ns

	setup time				
SDRAM5	CS,RAS,CAS,WE,DQM hold time	tH	TBD	-	ns
SDRAM6	Address setup time	tASU	TBD	-	ns
SDRAM7	Address hold time	tAH	TBD	-	ns
SDRAM8	SDRAM access time (CL=3)	tACC	-	TBD	
SDRAM8	SDRAM access time (CL=2)	tACC	-	TBD	
SDRAM8	SDRAM access time (CL=1)	tACC	-	-	
SDRAM9	Data out hold time	tDOH	TBD	tHZ[1]	
SDRAM10	Data out high-impedance time (CL=3)	tDOF	-	tHZ[1]	
SDRAM10	Data out high-impedance time (CL=2)	tDOF	-	-	
SDRAM10	Data out high-impedance time (CL=1)	tDOF	-	-	
SDRAM11	Active to read/write command (RC=1)	tARW	tRCD[2]	-	

Note: [1] t_{HZ}=SDRAM data out high-impedance time, external SDRAM memory device dependent parameter.

[2] t_{RCD}=SDRAM clock cycle time

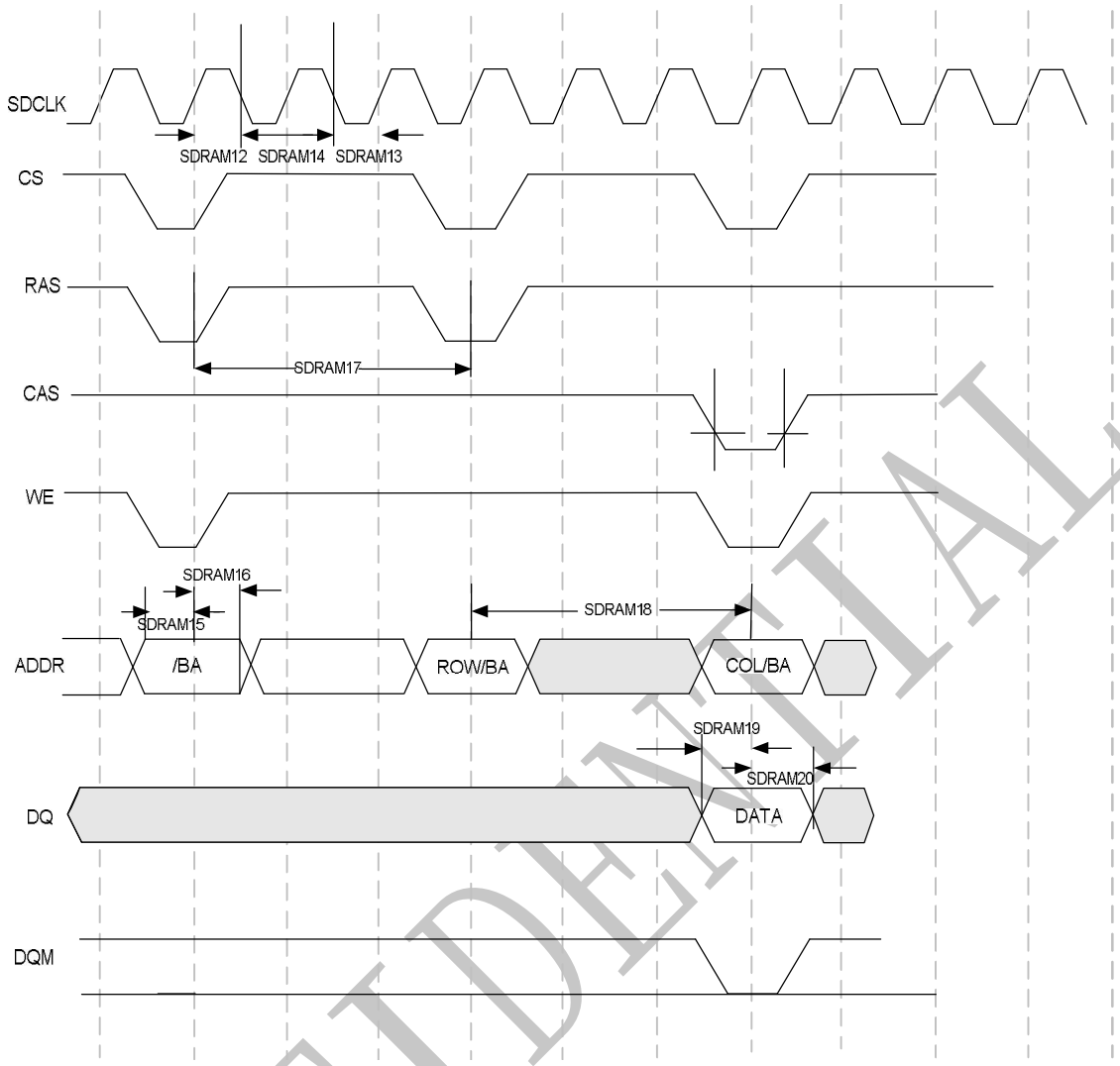

Figure 7-20 SDRAM interface write timing diagram

Table 7-5 AC timing parameter of write cycle

ID	Parameter	Symbol	Min	Max	Unit
SDRAM12	SDRAM clock high	tCH	TBD	TBD	ns
SDRAM13	SDRAM clock low	tCL	TBD	TBD	ns
SDRAM14	SDRAM clock cycle	tCLK	TBD	TBD	ns
SDRAM15	Address setup time	tASU	TBD	TBD	ns
SDRAM16	Address hold time	tAH	TBD	TBD	ns
SDRAM17	Precharge cycle period[1]	tPRE	TBD	TBD	
SDRAM18	Active to read/write command delay	tARW	TBD	TBD	
SDRAM19	Data setup time	tDSU	TBD	TBD	
SDRAM20	Data hold time	tDH	TBD	TBD	

Note: Precharge cycle timing is included in the write timing diagram

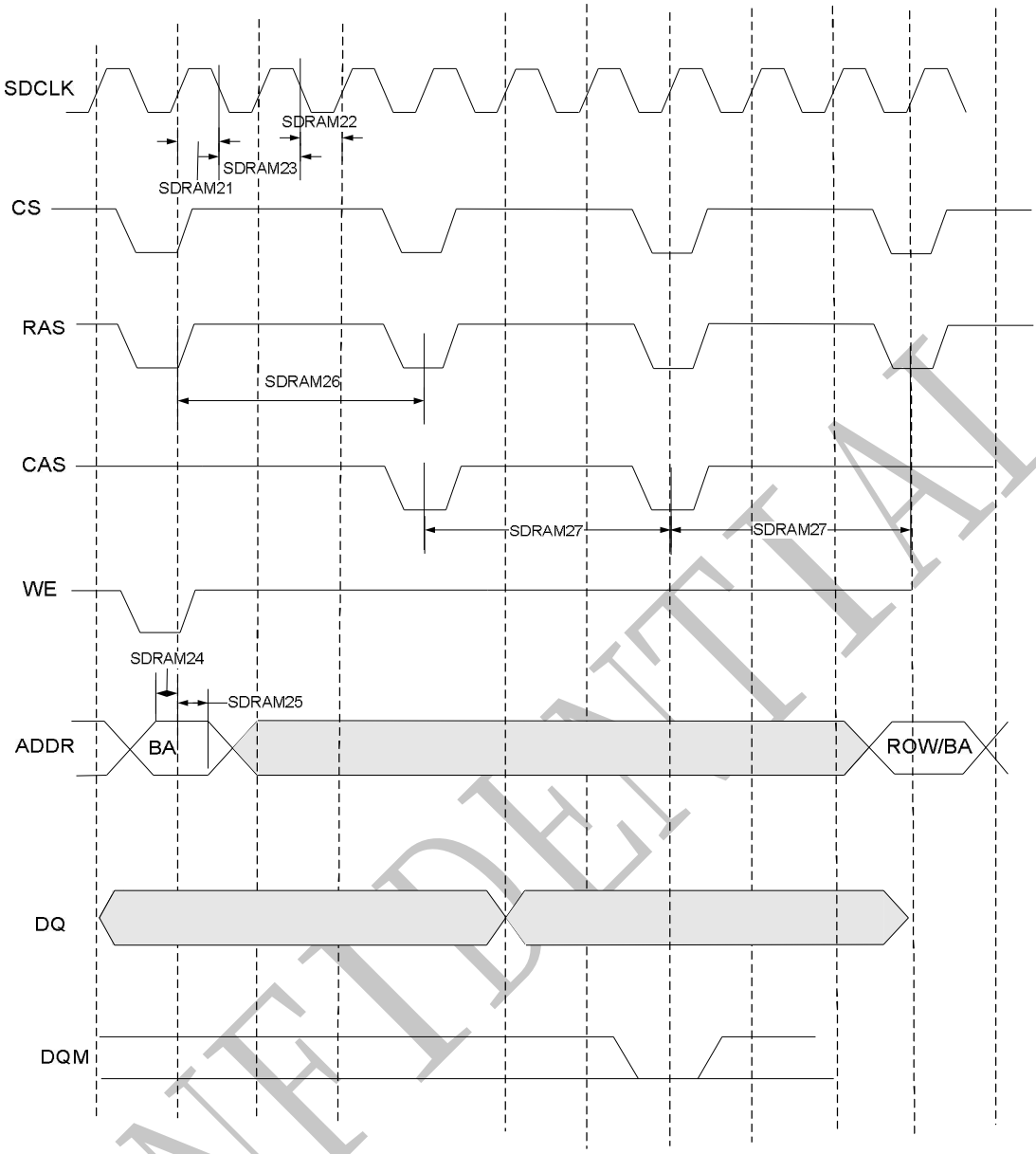

Figure 7-21 SDRAM interface refresh cycle timing diagram

Table 7-6 AC timing parameter of refresh cycle

ID	Parameter	Symbol	Min	Max	Unit
SDRAM21	SDRAM clock high	tCH	TBD	TBD	ns
SDRAM22	SDRAM clock low	tCL	TBD	TBD	ns
SDRAM23	SDRAM clock cycle	tCLK	TBD	TBD	ns
SDRAM24	Address setup time	tASU	TBD	TBD	ns
SDRAM25	Address hold time	tAH	TBD	TBD	ns

SDRAM26	Precharge command period[1]	tPRE	TBD	TBD	tCLK
SDRAM27	Auto refresh command period	tAPRE	TBD	TBD	tCLK

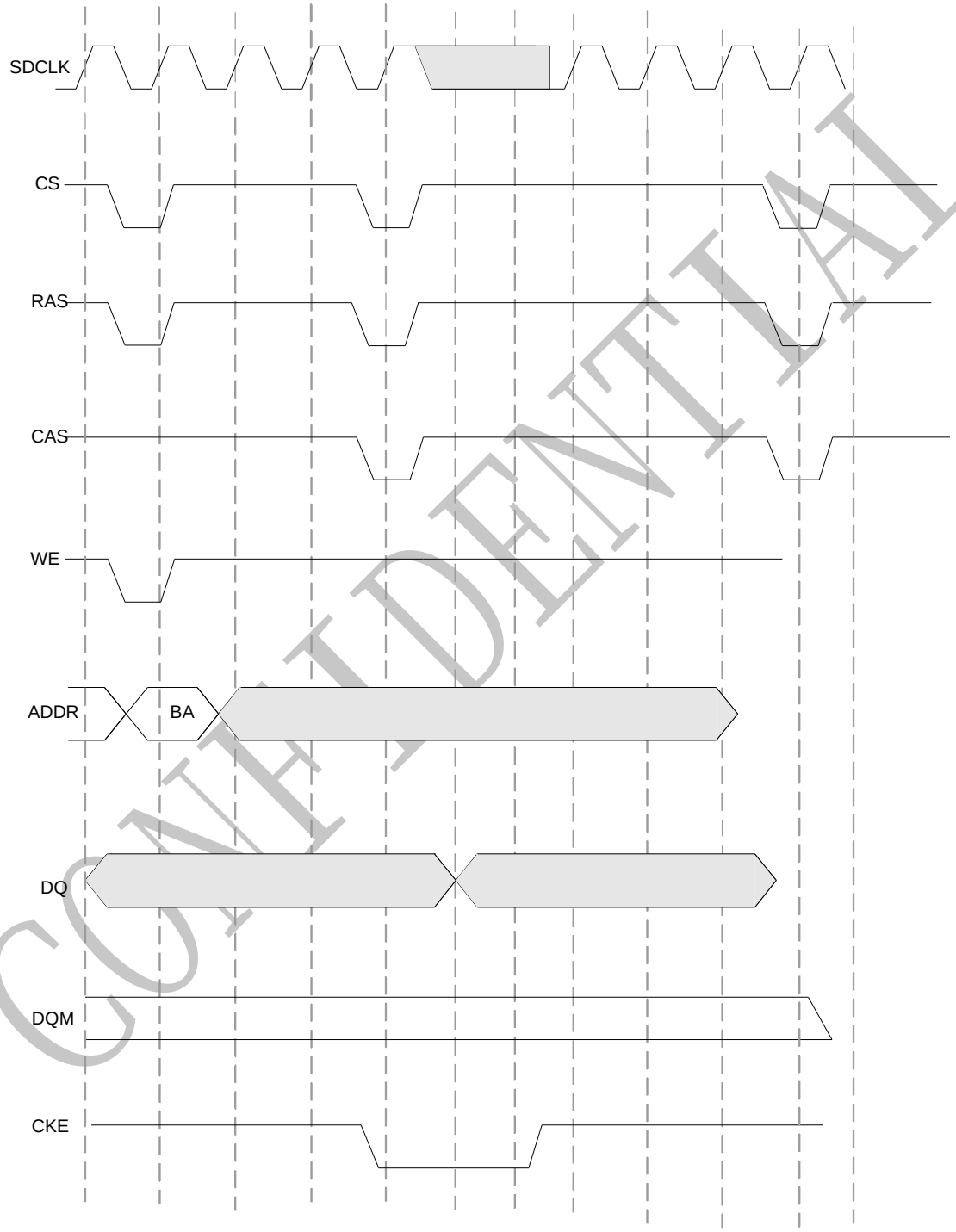

Figure 7-22 SDRAM interface self-refresh cycle timing diagram

7.2.3 SD card interface

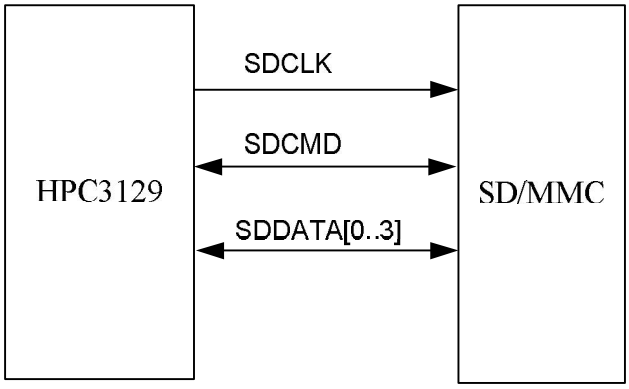

Figure 7-23 SD card interface diagram

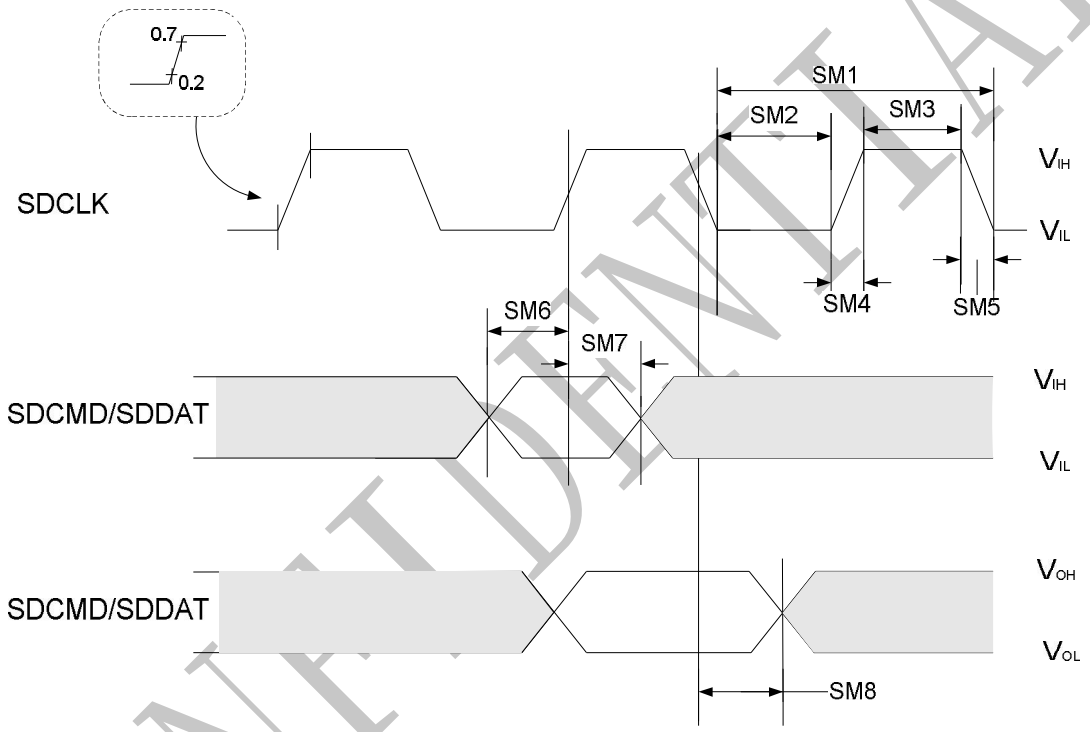

Figure 7-24 SD card interface timing diagram

Please refer to SD card physical layer specification for detailed timings.

7.3 HMAC interface

HMAC interface is responsible for transmitting or receiving data from RF module and the data rate is up to 6Mbps. HMAC can easily interface with many popular RF transceivers, such as A7121(AMICCOM®). HECC, a wireless communication error correction controller, is also included, which consists of CRC generator, RS encoder and RS decoder. So the HPC3129 is preferred for wireless multimedia applications.

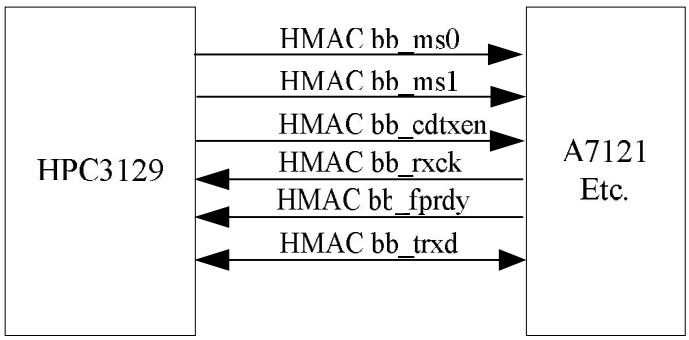

Figure 7-25 HMAC interface diagram

Please refer to corresponding transceiver datasheet for detailed timings.

7.4 TV encoder (Embedded Video DAC)

TV encoder is integrated on chip and supports for TV OUT up to D1 resolution (both NTSC and PAL).

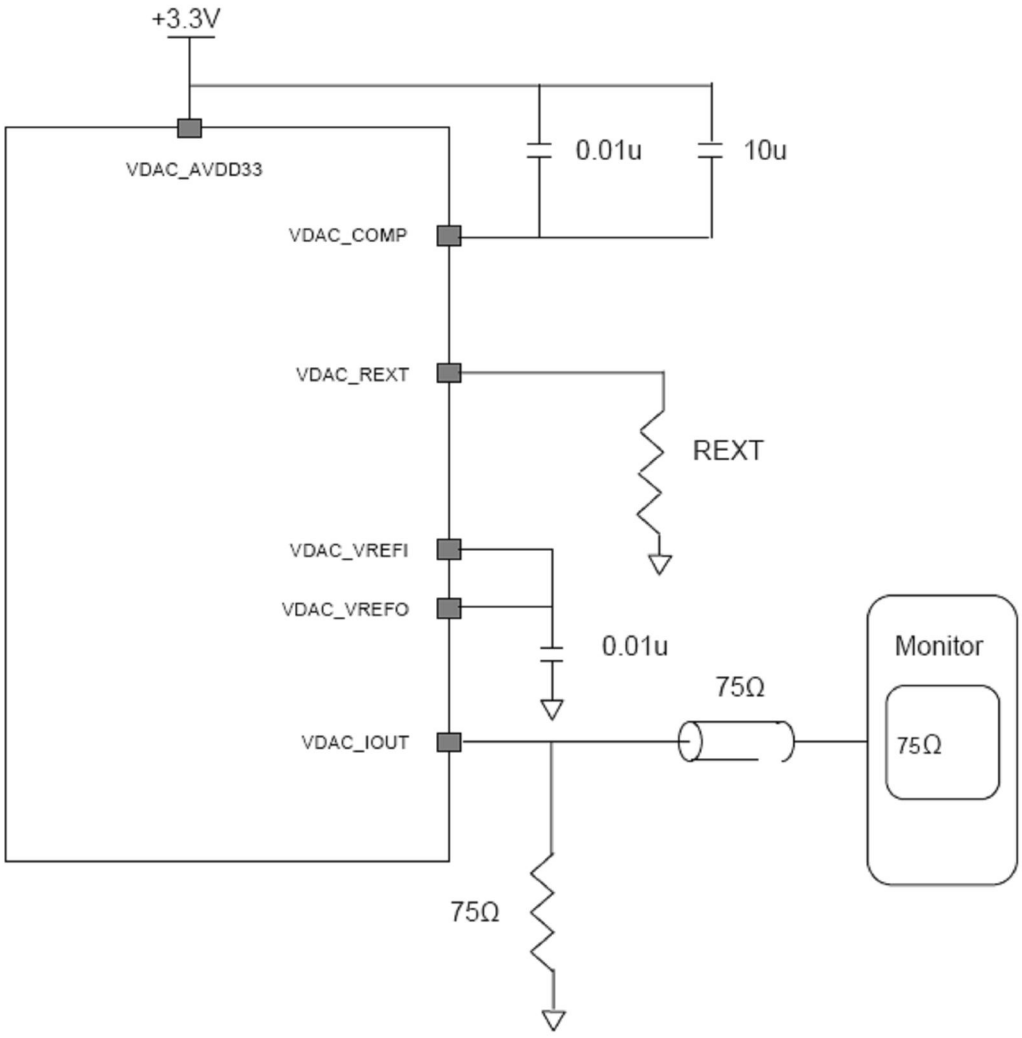

Figure 7-26 TV encoder interface diagram

7.5 I2S interface

I2S interface supports I2S bus specification(Philips Semiconductor 1996), and master and slave mode with DMA channel.

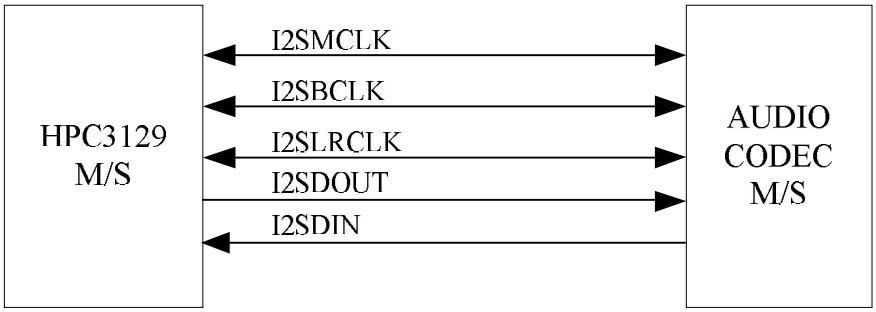

Figure 7-27 I2S interface diagram

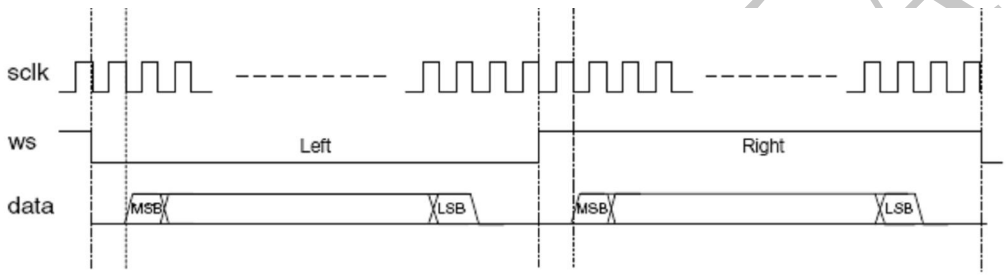

Figure 7-28 Standard I2S stereo frame format timing diagram

Note: sclk stands for I2SBCLK;
ws stands for I2SLRCLK;
data stands for I2SDIN or I2S DOUT.
Please refer to I2S standard for detailed timings.

7.6 ADC

ADC interface includes a 2-channel single-ended 10-bit Successive Approximation Register (SAR) analog-to-digital converter. It can be used to measure voltage of battery and other analog signals.

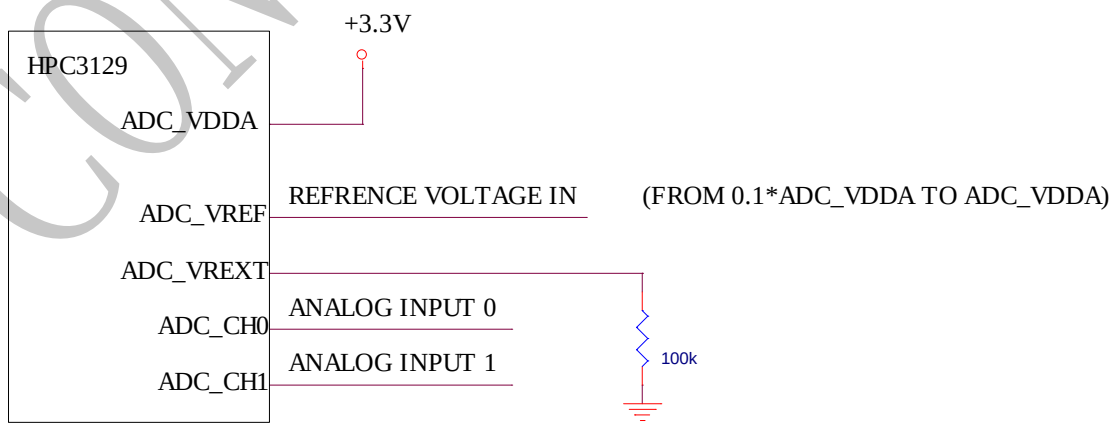

Figure 7-29 ADC interface diagram

7.7 I2C interface

I2C interface is compliant with Philips I2C standard and supports stand mode(100Kbps), fast mode(400Kbps) and high-speed mode(3.4Mbps). It also works in master or slave mode

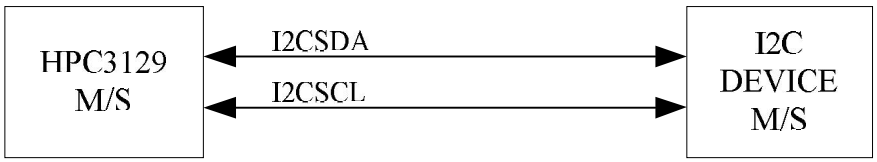

Figure 7-30 I2C interface diagram

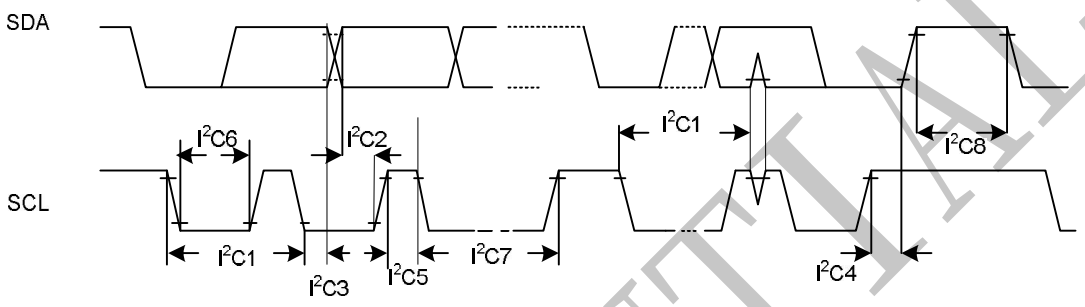

Figure 7-31 I2C interface timing diagram

Please refer to I2C standard for detailed timings.

7.8 SPI interface

The HPC3129 has 2 sets of 4-wire SPI buses, which of all both support master and slave mode with DMA channel

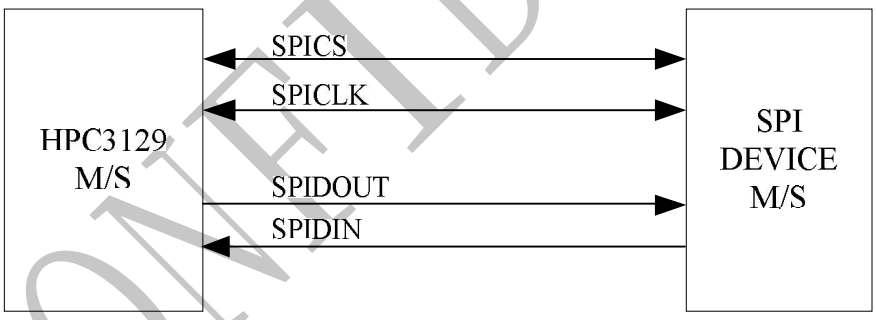

Figure 7-32 SPI interface diagram

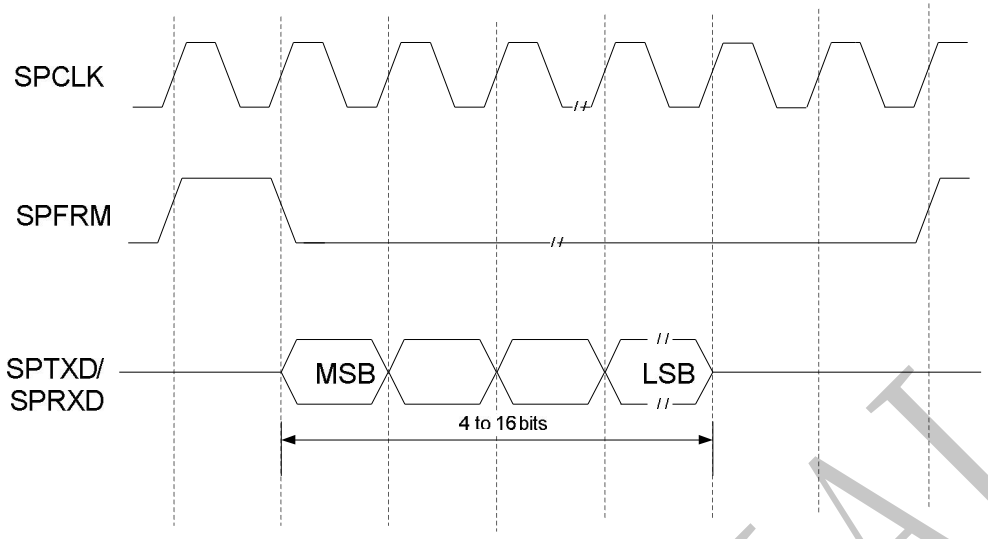

Figure 7-33 Texas Instruments' synchronous serial port interface timing diagram

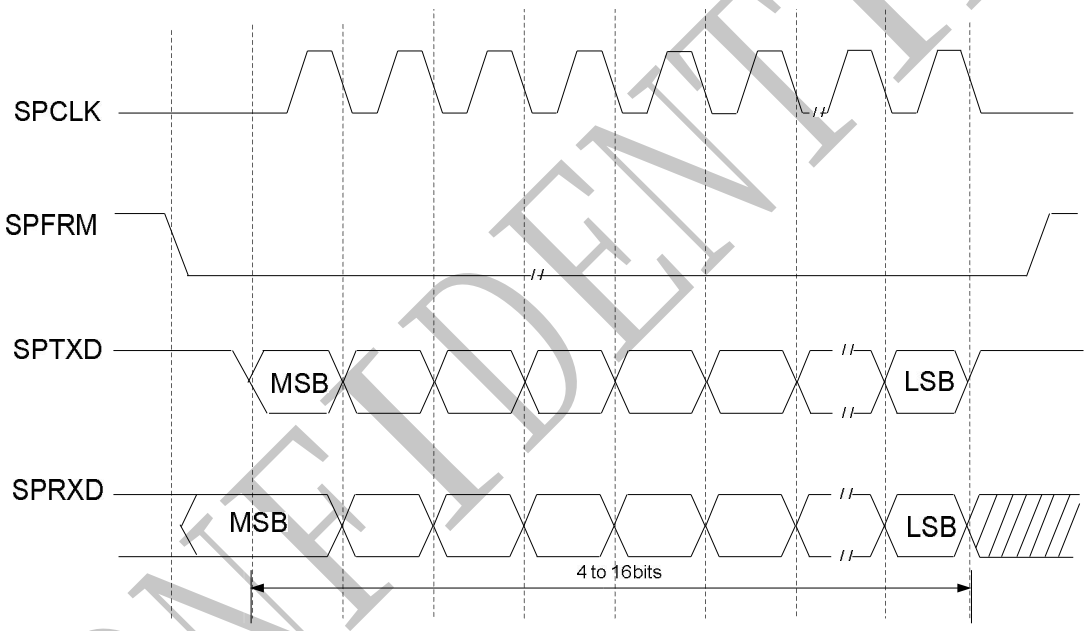

Figure 7-34 Motorola SPI interface timing diagram

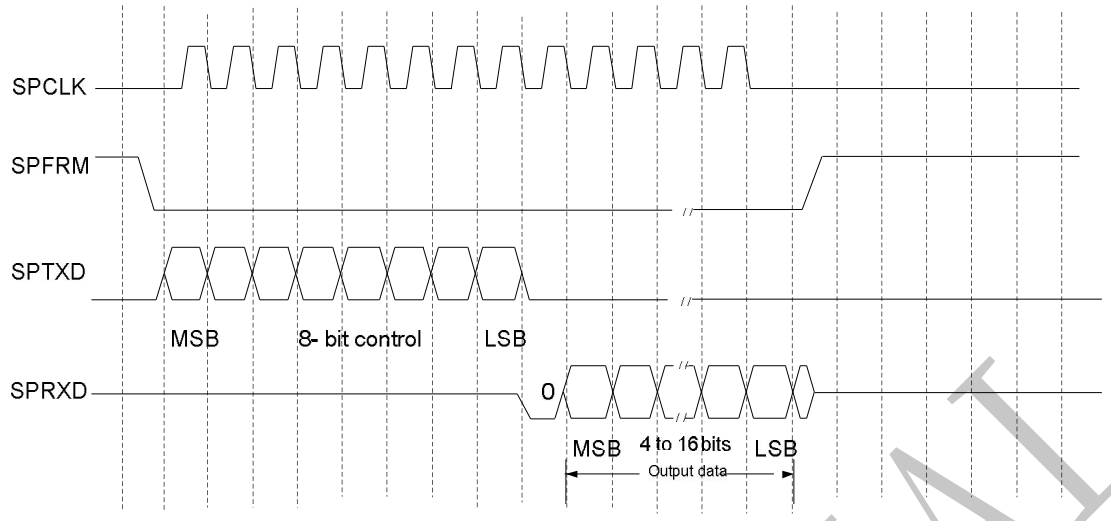

Figure 7-35 National Semiconductor microwire interface timing diagram

7.9 UART

UART interface has 1 set of 2-wire serial port and supports data transfer with DMA channel.

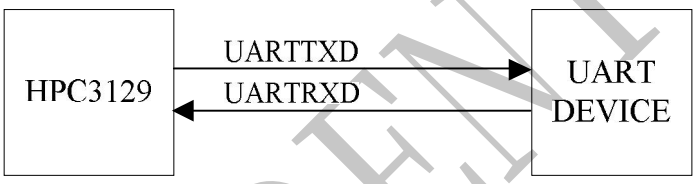

Figure 7-36 UART interface diagram

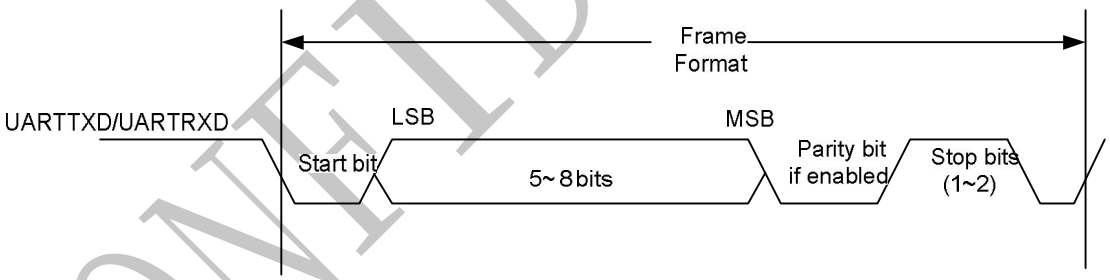

Figure 7-37 UART interface frame format diagram

7.10 KEYPAD

KEYPAD interface supports up to a 4x4 external key pad matrix and can generate interrupt to CPU.

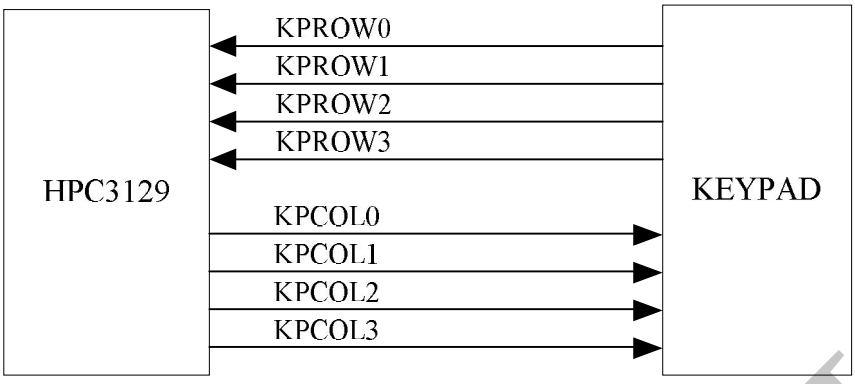

Figure 7-38 KEYPAD interface diagram

7.11 GPIO

GPIO interface has a total of 101 GPIO and all of them have been shared with other functions, except 3 independent GPIO. ALL GPIO can support interrupt to CPU.

7.12 PWM

The HPC3129 has a pin with PWM function for LCD backlight or motor control.

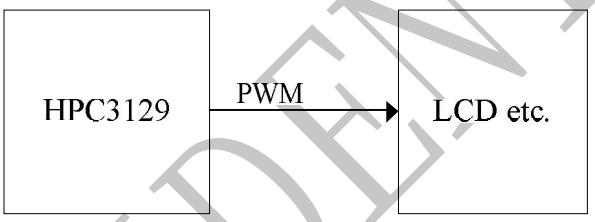

Figure 7-39 PWM interface diagram

7.13 Boot mode select

Two pins, BOOT0 and BOOT1, are used to select boot mode during chip reset. The HPC3129 can boot from NAND flash. SPI flash and UART. SPI flash for boot must be mounted on SPI bus 0.

Table 7-7 Boot mode select

BOOT1 LEVEL	BOOT0 LEVEL	Boot source
LOW	LOW	NAND flash
LOW	HIGH	SPI flash
HIGH	LOW	Reserved
HIGH	HIGH	UART

Note: HIGH stands for 1(high level);

LOW stands for 0(low level).

7.14 JTAG interface

JTAG interface is used to debug the HPC3129 and program.

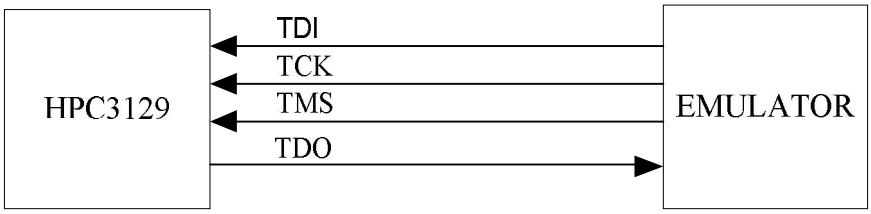

Figure 7-40 JTAG interface diagram