

CIRCUIT DESCRIPTION

Model: FRS200

a. Receiver Section

Radio Frequency signal received by the antenna (ANT1), passing through the Low Pass Filter (L2-L3, C8-C46). The RF signal is then amplified by Low Noise Amplifier Q10 and passes through a Band Pass Filter FL1 (465MHz). The filtered signal within the range of 462 MHz – 467 MHz is then mixed with the first local oscillator signal from the Voltage Controlled Oscillator (VCO) circuit (Q17-Q19, D9, L18) a portion of VCO signal is then feedback to the PLL IC (IC6) for phase comparison generating a stable RX Frequency, the output signal is filtered by FL2 (21.7 MHz) which is the first Intermediate Frequency (IF) and is then amplified by Q13. The IF signal is fed to the discriminator IC (IC1) pin 16 which is then mixed with the second local oscillator supplied by crystal X2 (21.25 MHz) to produce a reduced second IF signal which is then filtered by FL4 (450M). Demodulated signal is recovered through correct adjustment of IF tank coil (L13) and the internal discriminator circuit of IC2. The recovered audio signal is outputted at pin 9 of IC2 and then processed through filtering done by U1B circuit, the fully recovered audio signal is then further amplified by Power Amplifier U1A. An audible sound is therefore produced by the speaker SPK100, which can be varied from minimum to maximum through the key function (up/down) and process by the CPU IC3.

b. Transmitter Section

PTT switch when pushed triggers the Transmitter Circuit "ON", the voice signal generated by the surrounding noise passes through the Microphone MIC1 where mechanical to electrical transformation occurs, the electrical transformed signal is then filtered by a Band Pass Filter. The output signal is modulated by a modulator circuit with a varactor diode D7 and L18. The external components from Q17-Q19 form a VCO Circuit which generates the required oscillating frequency for transmission, a portion of this signal is feedback to the PLL IC6 pin 14 for phase comparison in order to produce a stabilized TX frequency. The modulated signal is then amplified by a Cascaded Amplifier Circuit Q15 and Q16 and again amplified by Q11 and Q14 to produce a sufficient Radio Frequency signal emitted by the Antenna (ANT1).

c. Call Transmission

By pushing the **CALL** key, a signal is detected by the CPU (IC3), a **CALL data** is then produced by the CPU. This data passes through the Band Pass Filter and modulated by the varactor diode D7 and L18. The signal follows its conventional transmission section path through the antenna.

d. Battery Low Detection

Battery Low Detection is controlled by the CPU IC3 as detected on the FRSLCD (IC5), however a voltage divider circuit R50 and R51 serve as the stabilize reference voltage for the CPU IC3 to process its detection.

e. Squelch Detection

Supported by the linear IC circuit (IC2), a variable resistor VR1 sets the level of detection and Diode D11 acts as a comparator circuit interface with the CPU IC3.

f. Power Supply

Supply voltage of 6 Volts dc is needed to power "ON" the whole circuitry, by four (4) batteries "AAA" size.

FREQUENCY CHART

CHANNEL	FREQUENCY (MHz)
1	462.5625
2	462.5875
3	462.6125
4	462.6375
5	462.6625
6	462.6875
7	462.7125
8	467.5625
9	467.5875
10	467.6125
11	467.6375
12	467.6625
13	467.6875
14	467.7125