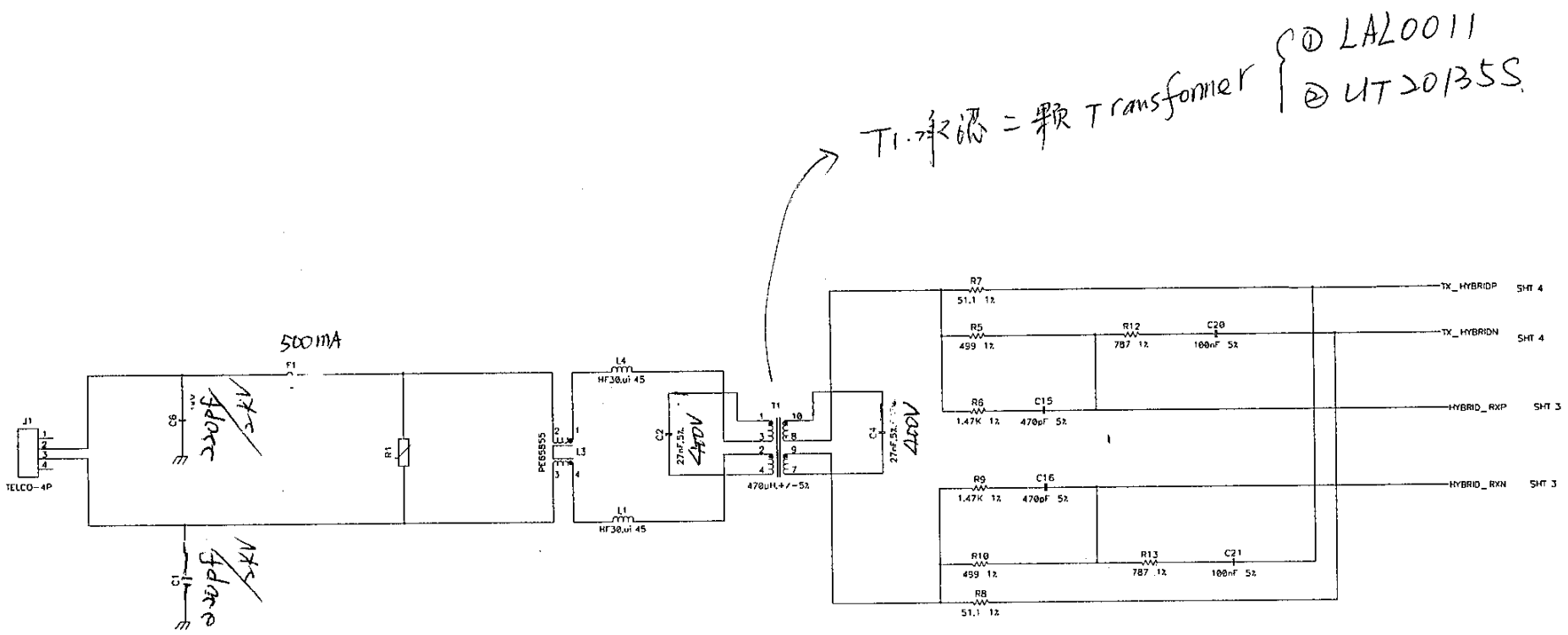
EXHIBIT D

Circuit Diagram

LINE PROTECTION + HPF + HYBRID

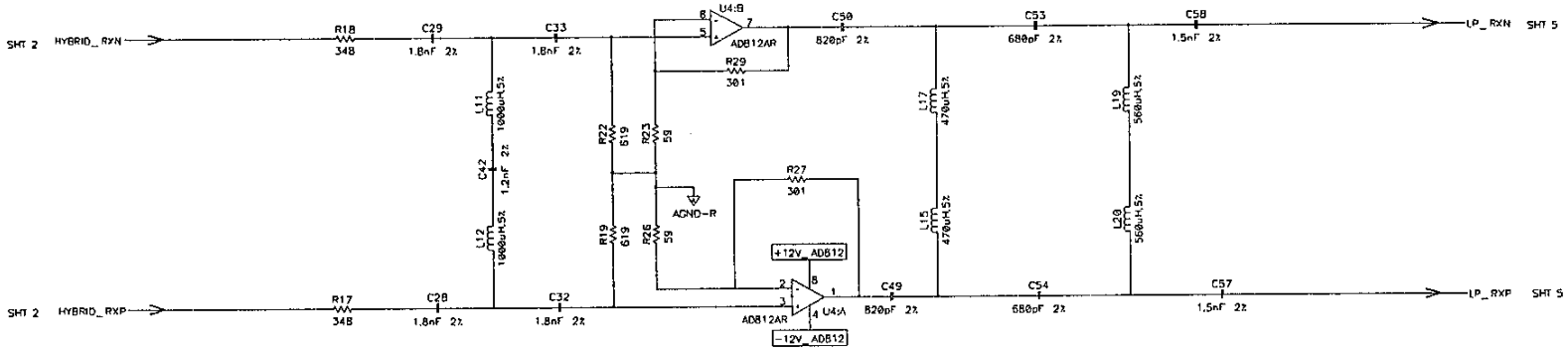


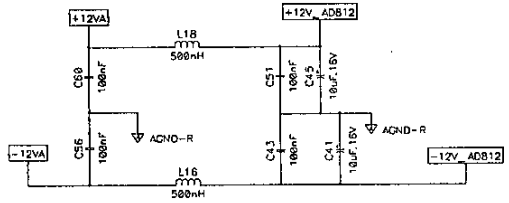
SAM_18K BOARD

SIZE	DWG NO.	REV
B	21-070010-00A	
SCALE: NONE	FILE NO	SHEET 2 OF 6

FORM D-1998-1 REV A

RECEIVE PATH

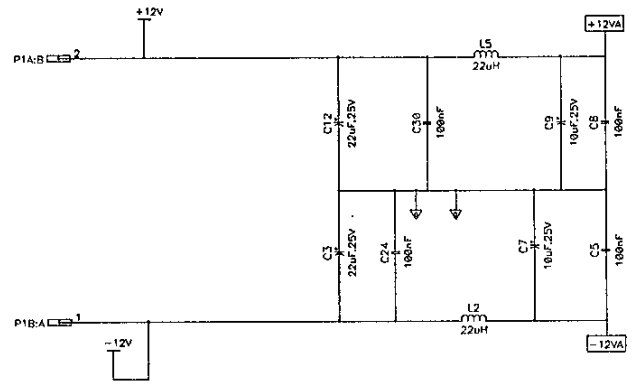


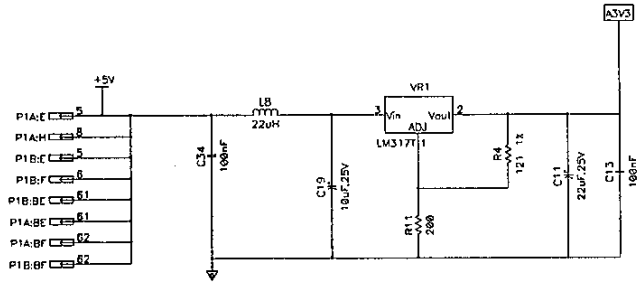


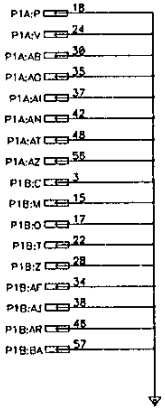
SAM_18K BOARD

SIZE	DWG NO.	REV
B	21-070010-00A	
SCALE: NONE	FILE NO.	SHEET 3 OF 5

FORM: D-1998-2 REV A







2. ALL CAPACITANCE ARE IN UF,+/-20%, 50V

1. ALL RESISTANCE ARE IN OHM, 1%

NOTES: UNLESS OTHERWISE SPECIFIED

REV	DESCRIPTION	DATE	APPROVED
A			

PARTS LIST

REV NO	QTY REQD	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

22-050010-004	APOLLO 701
NEXT ASY	USED ON

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES:
DECIMALS (.XX) ± .01 FRACTIONS ±
DECIMALS (.XXX) ± .005 ANGLES ±1
MATERIAL
FINISH
DO NOT SCALE DRAWING

APPROVALS	DATE
DRAWN SW	10-29-99
CHECKED	
ENGINEER	
ENG MFG	
RELEASED	

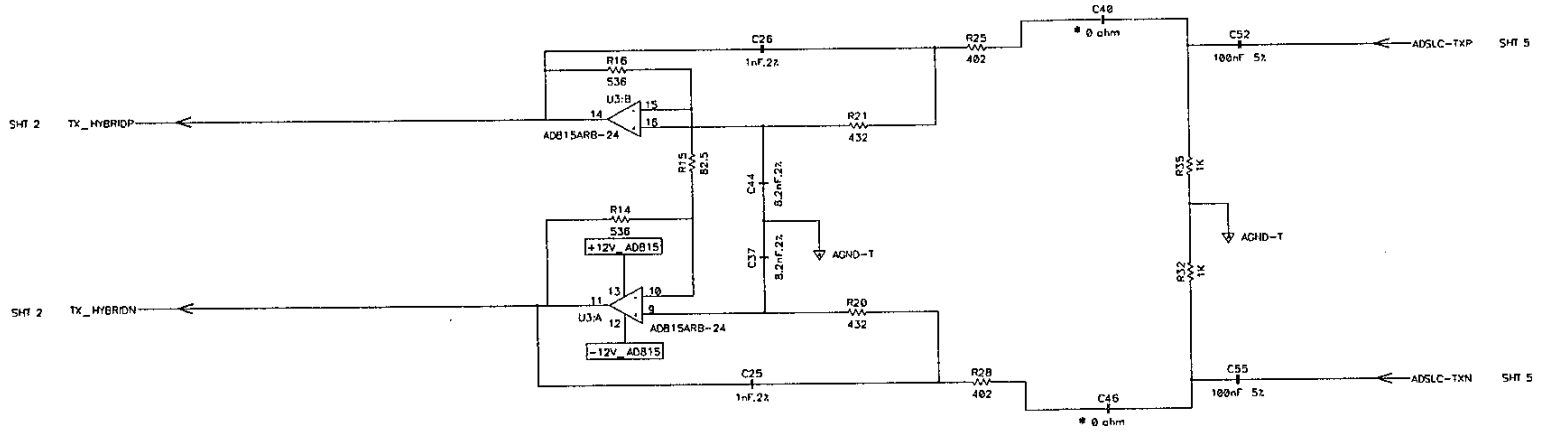
ITeX
2710 WALSH AVENU
SANTA CLARA, CA 95051

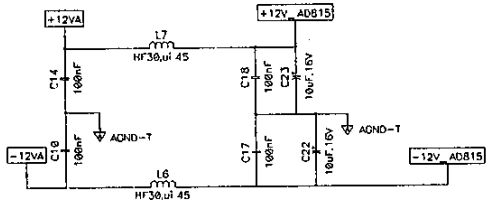
SCHEMATIC DIAGRAM
SAM_18K BOARD

SIZE B | DWG NO. 21-070010-00A
SCALE NONE | FILE NO | SHEET 1 OF 6

FORM: D-1998-1 REV A

TRANSMIT PATH





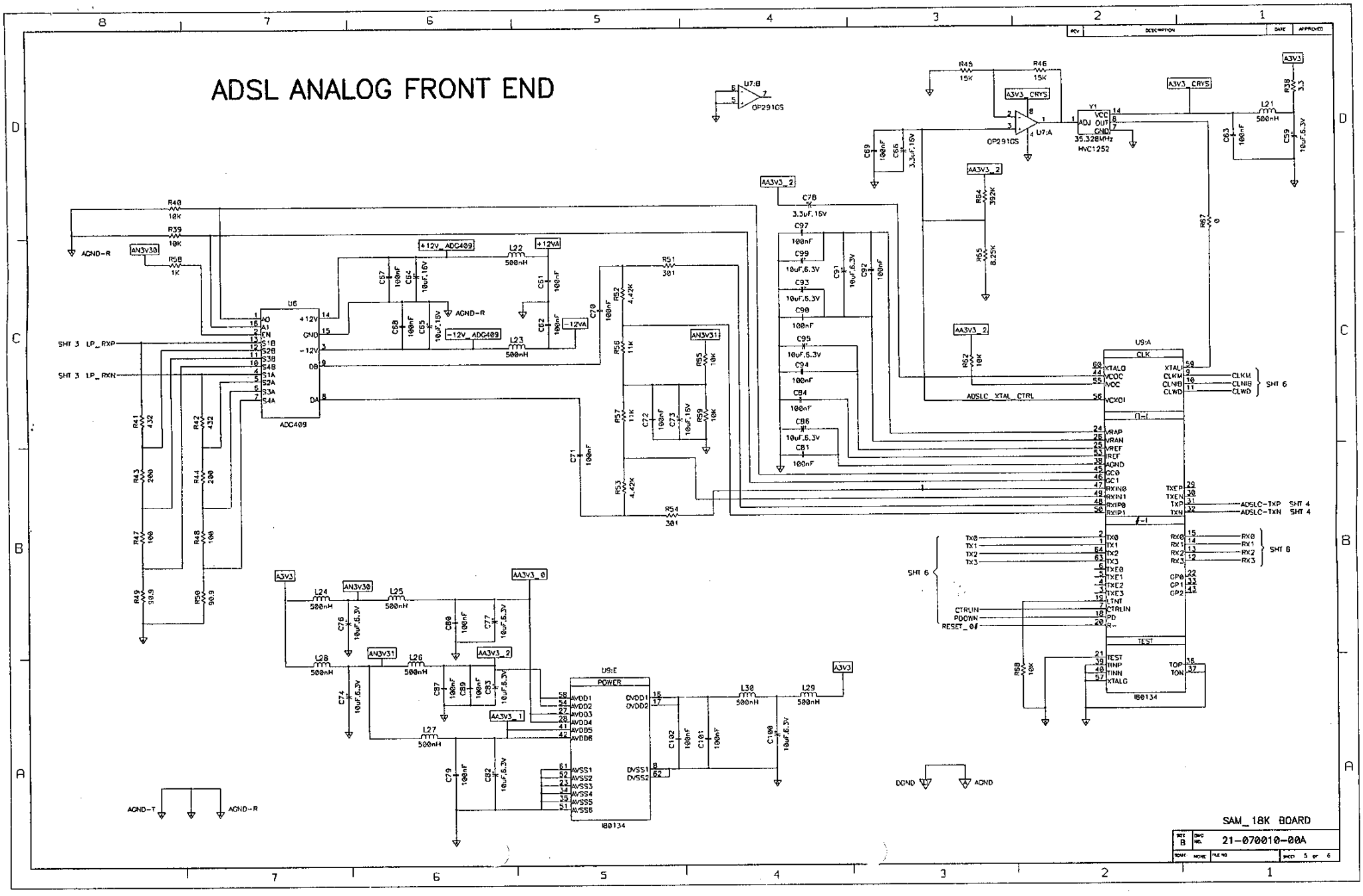
NOTE:

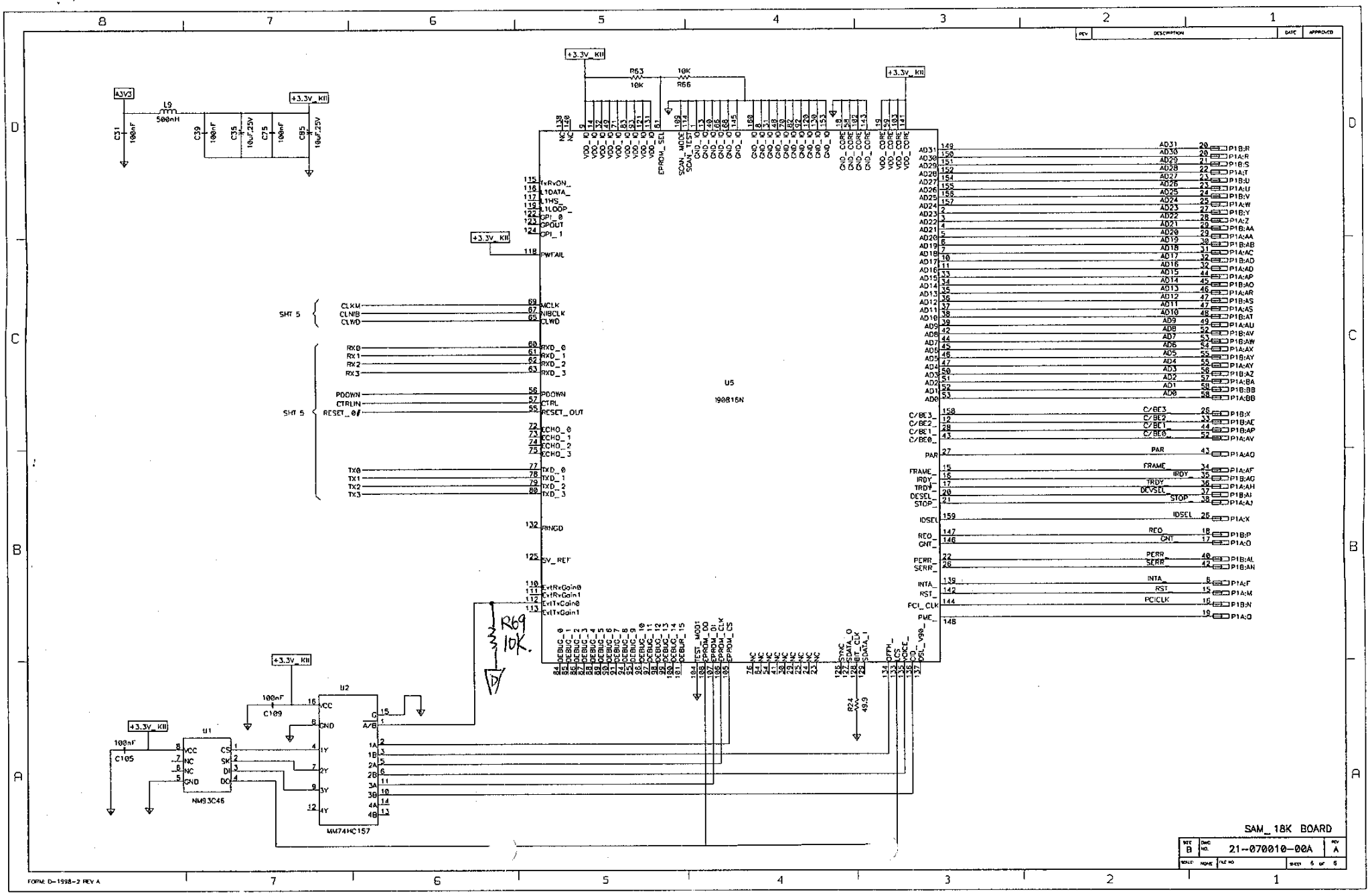
1. FOR U3 (AD815), PIN 5,6,7,8,17,18,19,20 MUST BE TIED TO +12V ACCORDING TO THE SPECIFICATION.
2. + FOR LOOP PURPOSE IN THIS CIRCUIT.

SAM_18K BOARD

SIZE	DWG NO.	21-070010-00A
B		
SCALE: NONE	FILE NO.	SHEET 4 OF 5

FORM: D-1998-2 REV A


ADSL ANALOG FRONT END
SAM_18K BOARD
21-070010-00A
SHT 3 LP_RXP
SHT 3 LP_RXN
ADC409
U6
U9:A
U9:E
U7:A
U7:B
OP291GS
35.328MHz
HVC1252
ADSLC_XTAL_CTRL
ADSLC-TXP SHT 4
ADSLC-TXN SHT 4
SHT 6
AGND-R
AGND-T
DGND
AGND
POWER
IB0134


SAM_18K BOARD
21-070010-00A
U5
190B15N
MM74HC157
NM93C46
R69
10K.
R63
10K
R66
10K
R24
49.9
+3.3V_KII
A3V3
L9
500nH
C31
100nF
C39
100nF
C35
10uF,25V
C75
100nF
C85
10uF,25V
C109
100nF
C105
100nF
SHT 5
CLKM
CLNIB
CLWD
RXD_0
RXD_1
RXD_2
RXD_3
PDOWN
CTRL
RESET_OUT
ECHO_0
ECHO_1
ECHO_2
ECHO_3
TXD_0
TXD_1
TXD_2
TXD_3
RNGD
SV_REF
ExtRxGain0
ExtRxGain1
ExtTxGain0
ExtTxGain1
PWFAIL
TxRxON_
L1DATA_
L1HS_
L1LOOP_
GPI_0
GPOUT
GPI_1
MCLK
NIBCLK
CLWD
AD31
AD30
AD29
AD28
AD27
AD26
AD25
AD24
AD23
AD22
AD21
AD20
AD19
AD18
AD17
AD16
AD15
AD14
AD13
AD12
AD11
AD10
AD9
AD8
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
C/BE3_
C/BE2_
C/BE1_
C/BE0_
PAR
FRAME_
IRDY_
TRDY_
DEVSEL_
STOP_
IDSEL
REQ_
GNT_
PERR_
SERR_
INTA_
RST_
PCI_CLK
PME_
P1B:R
P1A:R
P1B:S
P1A:T
P1B:U
P1A:U
P1B:V
P1A:W
P1B:Y
P1A:Z
P1B:AA
P1A:AA
P1B:AB
P1A:AC
P1B:AD
P1A:AD
P1A:AP
P1B:AO
P1A:AR
P1B:AS
P1A:AS
P1B:AT
P1A:AU
P1B:AV
P1B:AW
P1A:AX
P1B:AY
P1A:AY
P1B:AZ
P1A:BA
P1B:BB
P1A:BB
P1B:X
P1B:AC
P1B:AP
P1A:AV
P1A:AO
P1A:AF
P1B:AG
P1A:AH
P1B:AI
P1A:AJ
P1A:X
P1B:P
P1A:O
P1B:AL
P1B:AN
P1A:F
P1A:M
P1B:N
P1A:Q
DEBUG_0
DEBUG_1
DEBUG_2
DEBUG_3
DEBUG_4
DEBUG_5
DEBUG_6
DEBUG_7
DEBUG_8
DEBUG_9
DEBUG_10
DEBUG_11
DEBUG_12
DEBUG_13
DEBUG_14
DEBUG_15
TEST_MODE
EPROM_DO
EPROM_CLK
EPROM_CS
SYNC
SDATA_O
BIT_CLK
SDATA_I
OFFH_
CS
VOICE_
CD
PSL_V90_
EPROM_SEL
SCAN_MODE
SCAN_TEST
SAM_18K BOARD
21-070010-00A
FORM: D-1998-2 REV A