Test Name: Process Gain **Test# 3.1**

Test Summary:

- Verifies that the radio generates at least 10 dB of process gain while receiving a signal.
- Test performed using signal simulator combined with CW jamming signal, both at same operating frequency
- Test performed at room temperature, one operational frequency only.

Applies to Specification: 3.3.8

Definition:

Channel Frequency: 923.58 MHz

Pass / Fail Criteria:

A pass is defined when the mean of measured one's power relative to the mean of a zero's value exceeds 10 dB. One's value relates to the desired signal properly correlated. Zero's value relates to the CW signal spread by the receive correlator. Both values measured at the detector output.

Required Test Equipment:

Boonton 4220A Power meter with 51175 sensor (diode sensor).
HP ESG 4423B Signal Generator (qty 2).
HP 8590L Spectrum Analyzer or equivalent.
Axonn Transmitter Simulator (Interositor)
Dual output, variable Power Supply for 0 to 30.0 VDC, Loadstar or equivalent
IBM PC compatible computer with two RS 232 serial interfaces
Axonn WINTAP Receiver Analysis Software Version 0.81
FLUKE 87 True RMS Multi-meter
Transceiver RS232 and Power Interface Box with wall transformer
RS 232 transceiver serial cable (qty 2)
High Isolation 50 Ohm cables (STORM or equivalent)
2:1 50 Ohm Signal Combiner
HP 1662A Logic Analyzer or equivalent

Equipment Setup: *(Refer to diagram labeled **Test Configuration 3.1**)*

Note: Tests assume all devices are in calibration and operating to manufacturers specification.

Initial Setup (Desired Signal Generation)

1 Configure Power Supply to output +/- 12 VDC. Set current limit to 150 mA. Measure output voltage using Fluke DVM or equivalent. Disable (or turn off supply)

2 Connect RS232 cable between computer (PC) and the signal simulator

3 Configure HP ESG 4423B Signal Generator to produce CW signal at 923.58 MHz, -38 dBm output power (as starting point to be modified below for calibration)

4 Connect RF output of HP ESG 4423B Signal Generator to RF IN connector of the signal simulator using SMA cable.

5 Connect RF OUT of signal simulator to step attenuator. Set step attenuator to 0 ohms.

6 Connect output of step attenuator to HP 8590L Spectrum Analyzer. Configure Spectrum Analyzer to monitor signal at 923.58 MHz, 3 MHz span, peak signal to be observed around –54 dBm.

7 Install / Run WINTAP program on PC. Select TX CAL mode using button on top bar of program.

8 Select CAL mode on signal simulator. This should be observed as a CW signal on the Spectrum analyzer at 923.58 MHz with relative signal power at –54 dBm.

9 Adjust output power of the HP ESG 4423B Signal Generator until the peak power observed on the HP8590L spectrum analyzer reads – 54 dBm.

10 Remove signal from spectrum analyzer and connect to Boonton 4220A Power meter. Confirm power measurement at – 54 dBm. Select RUN mode on signal simulator (from CAL mode). Confirm power measurement on Boonton Power Meter does not change from – 54 dBm.

11 Disconnect signal from Boonton Power Meter and connect to conducted (antenna B) input of AXC420 device under test (DUT).

Initial Setup (final test configuration)

12 Connect second com port of PC to RS232 and Power Interface of AXC420.

13 Plug in wall power transformer for the RS232 and Power Interface and connect cannon jack to the interface box. Insure On/Off switch is set to the ON position for test.

14 Connect HP 1662A Logic Analyzer to test interface connector of DUT observing connections in table 3.1-1.

15 Connect “trigger Out” and “clock out“ signals from DUT to spread gating interface.

16 Configure Logic Analyzer as follows (Load config from saved file on disk or set as follows): **System**: set for State Mode, Pod 1 & 2 to State Machine 1. **Format definitions**: DBUS Pod 1, pins 1-8; RD Pod1, pin 9; WR Pod1, pin 10. CLK definitions: enable JCLK and KCLK rising edge. **Trigger definitions**: while storing anything, trigger on DBUS = C0 hex, RD=0, then store anything; enable measure time in data acquisition option.

Data Collection

17 Confirm transmitter and receiver operation. Select RUN mode in WINTAP program. Observe messages being received at receiver.

18 Attenuate signal by 50 dB at step attenuator. This places signal being processed to –104 dBm. Observe messages being received at receiver.

19 Attenuate signal by 60 dB at step attenuator. Confirm signal no longer is being received.

20 Return attenuator to 50 dB setting.

21 Press RUN on Logic Analyzer. Observe data collected on logic analyzer. Data at analyzer should represent captured messages similar to that depicted in table 3.1-2 below. *Note: This confirms test configuration only and the data collected is not used for measurement*.

22 Connect "spread/CW" signal from spread gating interface to signal simulator.

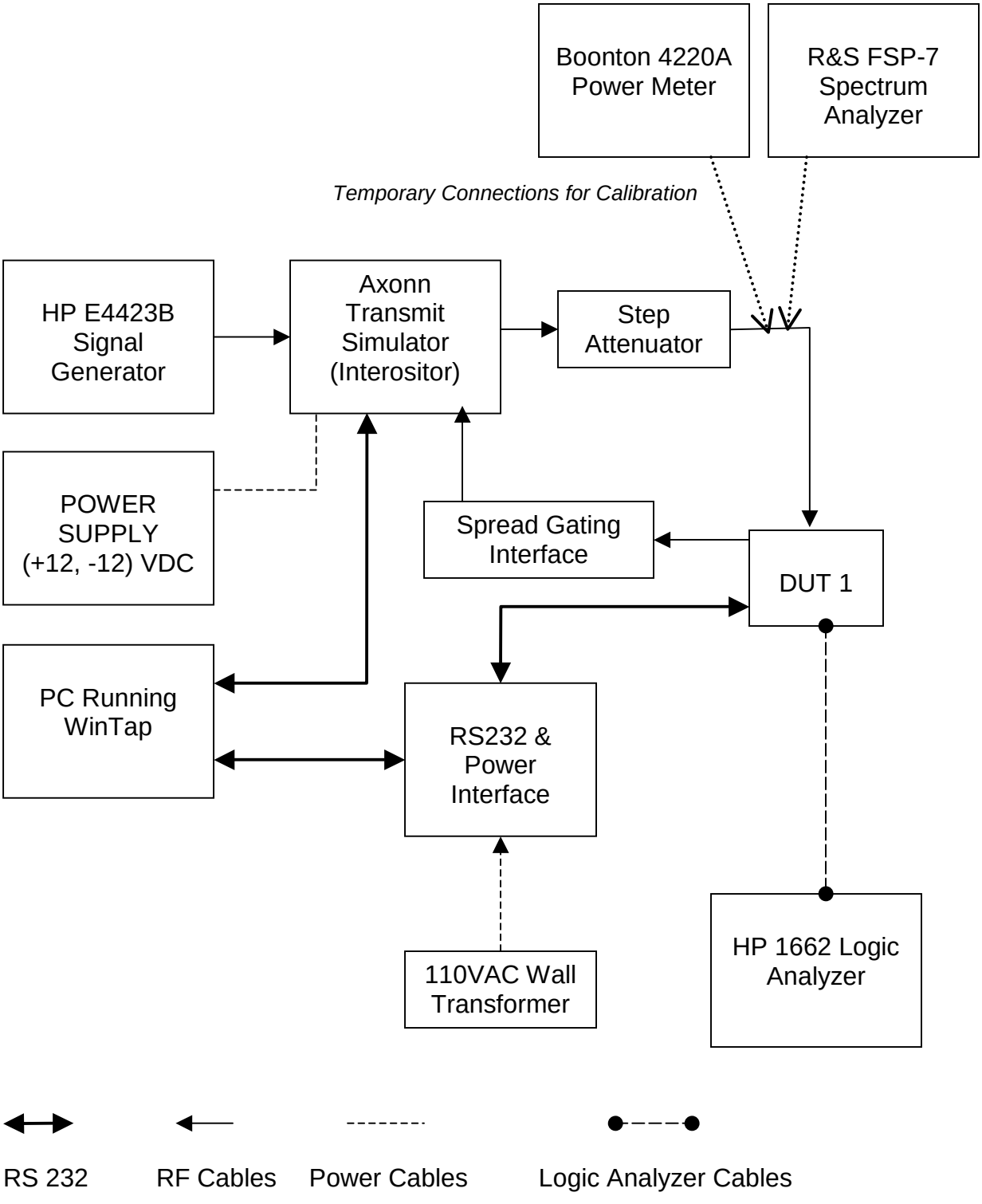
23 Press RUN on Logic Analyzer. Observe data collected on logic analyzer and **save the listing to floppy.** Data collected should represent a captured with the spread signal being modulated on and off during the message. Signal received will appear similar to that depicted in table 3.1-3 below. This is the –104 dBm data used to evaluate process gain.

24 Attenuate signal by 40 dB at step attenuator. (desired signal at –94 dBm)

25 Press RUN on Logic Analyzer. Observe data collected on logic analyzer and **save the listing to floppy**. Data collected should represent a captured with the spread signal being modulated on and off during the message. Signal received will appear similar to that depicted in table 3.1-3 below. This is the –94 dBm data used to evaluate process gain.

Data Processing and Interpretations

26 Process the –104 dBm and –94 dBm data collected while the data demodulator interface was engaged. See notes below tables 3.1-2 and 3.1-3 for data interpretations and methods.



TEST CONFIGURATION 3.1

Test Configuration and Data Collection Description:
Although this test configuration may be complicated, the test methodology above may require further information to provide clarity. This section is provided to add more detail than allowed for in the process method above.

Configuring the hardware for test as noted above will result in displays presented on several of the test equipment. Those displays were captured and presented below as confirmation of proper configuration.

Step 8 in **Equipment Setup** has a display on the spectrum analyzer as depicted in Fig 3.1.1. The CW signal generated by the function generator through the signal simulator serves as the uncorrelated signal source.

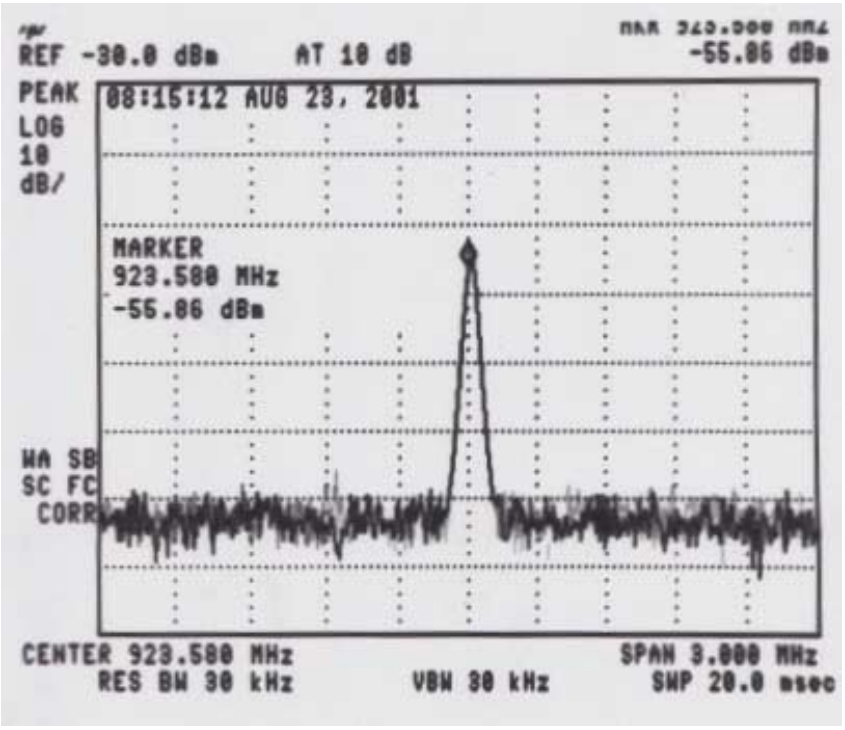


Fig. 3.1.1

Switching the CAL/RUN switch to the RUN position on the transmitter simulator will enable the transmitted signal to be spread. The CW signal is spread by the signal simulator. The resulting signal will be correlated in the receiver to generate process gain. The spread signal will appear on the spectrum analyzer as depicted in Fig 3.1.2 and Fig 3.1.3.

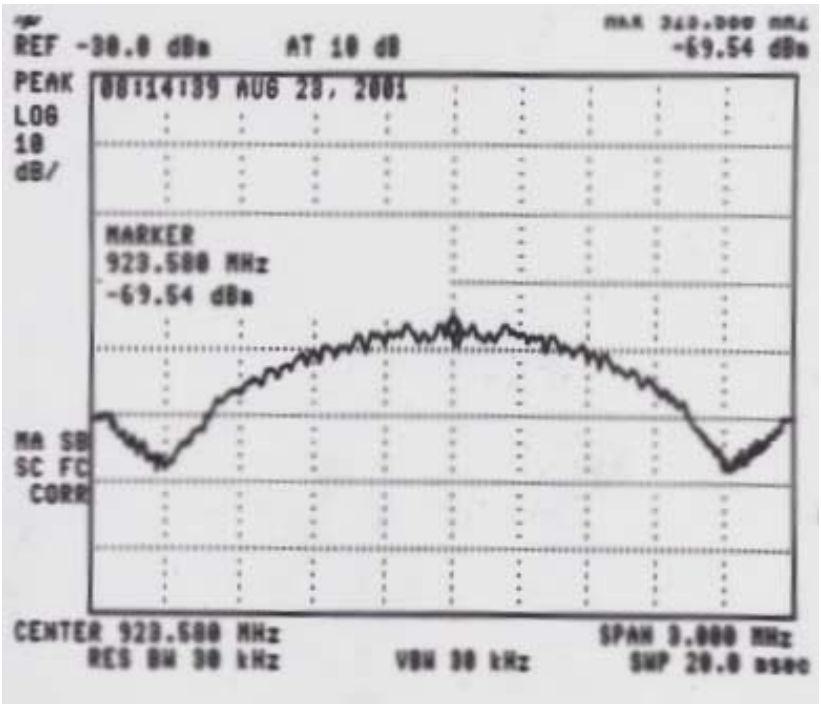


Fig. 3.1.2

Using the peak hold feature of the spectrum analyzer and toggling the switch will show the transmitter process gain that the receiver will recover.

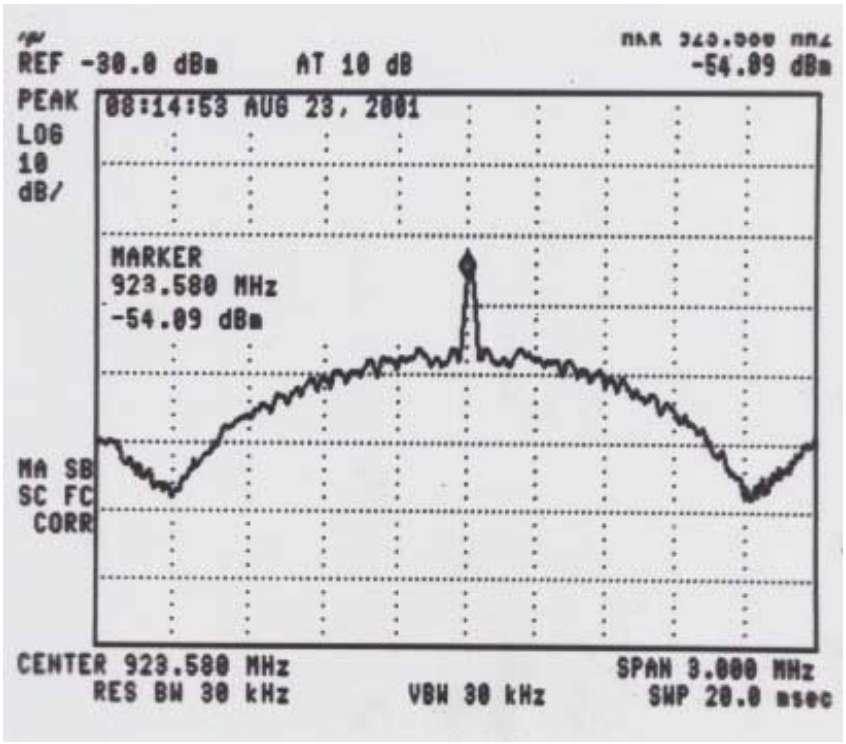


Fig. 3.1.3

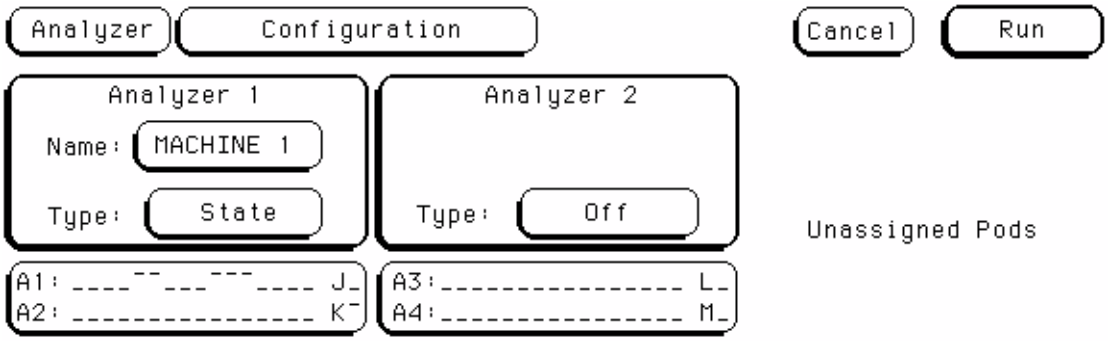
The DUT has a debug interface connector used to gain access to the data being passed between the two processors on the board. The DSP performs all the search and dispreading (correlation) functions necessary to demodulate the signal. The DSP sends an 8-bit term to the TIP processor each bit interval. The TIP processor collects and packets the message to generate a report.

Process gain data can be captured from the interface of these two processors. The output power bytes from the DSP chip can be captured at the debug header of the DUT. The table 3.1-1 defines the pinout of the header and the interconnects to the logic analyzer.

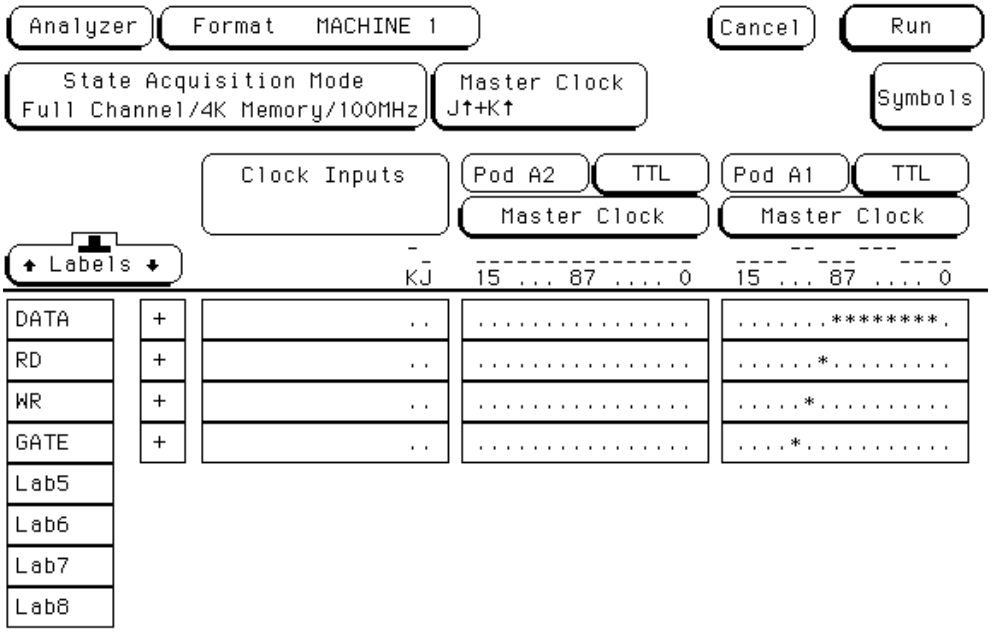
Table 3.1-1
Logic Analyzer Connections to DUT

Pod 1 pin	DUT connection
J CLK	DUT Test Interface Connector Pin 9 (RD signal between DSP and TIP)
1	DUT Test Interface Connector Pin 1 (Dbus 0 between DSP and TIP)
2	DUT Test Interface Connector Pin 2 (Dbus 0 between DSP and TIP)
3	DUT Test Interface Connector Pin 3 (Dbus 0 between DSP and TIP)
4	DUT Test Interface Connector Pin 4 (Dbus 0 between DSP and TIP)
5	DUT Test Interface Connector Pin 5 (Dbus 0 between DSP and TIP)
6	DUT Test Interface Connector Pin 6 (Dbus 0 between DSP and TIP)
7	DUT Test Interface Connector Pin 7 (Dbus 0 between DSP and TIP)
8	DUT Test Interface Connector Pin 8 (Dbus 0 between DSP and TIP)
9	DUT Test Interface Connector Pin 9 (RD signal between DSP and TIP)
10	DUT Test Interface Connector Pin 10 (WR signal between DSP and TIP)
Pod 2 pin	**DUT connection**
K CLK	DUT Test Interface Connector Pin 10 (WR signal between DSP and TIP)

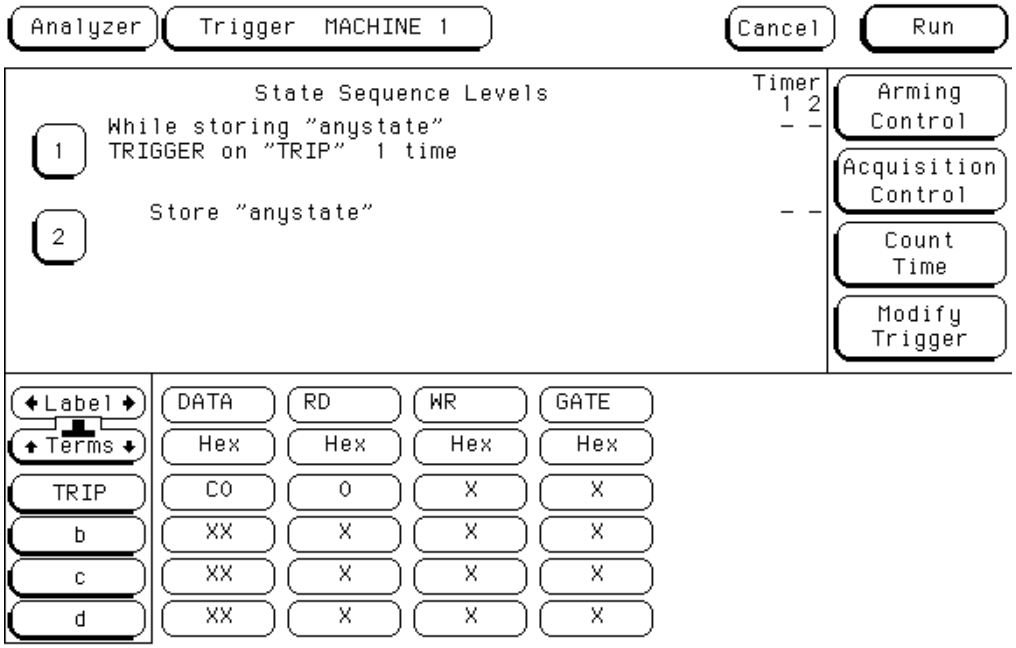
The logic analyzer must be setup to capture the data. Pods 1 and 2 are slaved to analyzer 1 in state mode. The following graphic depicts the Configuration menu settings.



Pod pin assignments are made in the Format setup dialog. The J and K clocks are enabled rising edge, one on RD and one on the WR signal from the TIP. This clocks data to and from the DSP to capture all data on the byte wide interface. The WR and RD signals are also captured for data delimitation. The gate signal is also captures. This is the signal that drives the CW/Spread state in the signal simulator.



The trigger setup tells the logic analyzer when to capture the data. Trip is denoted when the DSP sends a hex C0 to the TIP. Also, the analyzer is configured to display time interval between captured events.



When properly configured, pressing RUN on the logic analyzer will display a listing similar to that depicted in table 3.1-2.

Table 3.1-2
MACHINE 1 - State Listing

Label	>	DATA	RD	WR	GATE	Time	
Base	>	Hex	Hex	Hex	Hex	Relative	
-20		60	1	0	1	26.40	us
-19		5C	0	1	1	1.314	ms
-18		60	1	0	1	26.40	us
-17		A6	0	1	1	127.4	us
-16		00	0	1	1	296	ns
-15		60	1	0	1	27.62	us
-14		5C	0	1	1	1.313	ms
-13		60	1	0	1	26.40	us
-12		A6	0	1	1	128.0	us
-11		00	0	1	1	296	ns
-10		60	1	0	1	27.63	us
-9		5C	0	1	1	1.314	ms
-8		60	1	0	1	26.40	us
-7		A6	0	1	1	127.4	us
-6		00	0	1	1	296	ns
-5		60	1	0	1	27.62	us
-4		5C	0	1	1	1.314	ms
-3		60	1	0	1	26.40	us
-2		81	0	1	1	127.7	us
-1		80	1	0	1	15.97	us
0		C0	0	1	1	367.7	us
1		80	1	0	1	12.90	us
2		72	0	1	1	36.83	us
3		80	1	0	1	9.832	us
4		FE	0	1	1	41.13	us
5		80	1	0	1	29.47	us
6		FF	0	1	1	22.71	us
7		80	1	0	1	27.63	us
8		FF	0	1	1	23.33	us
9		80	1	0	1	27.63	us
10		F1	0	1	1	23.94	us
11		80	1	0	1	28.86	us
12		E1	0	1	1	23.33	us
13		80	1	0	1	28.86	us
14		FA	0	1	1	22.10	us
15		80	1	0	1	27.63	us
16		FF	0	1	1	23.94	us
17		80	1	0	1	27.63	us
18		F9	0	1	0	24.56	us
19		80	1	0	0	27.62	us
20		F1	0	1	0	23.94	us
21		80	1	0	0	28.86	us

22	E4	0	1	0	22.71	us
23	80	1	0	0	28.86	us
24	EC	0	1	0	22.10	us
25	80	1	0	0	28.86	us
26	FE	0	1	0	22.71	us
27	80	1	0	0	27.63	us
28	FF	0	1	0	24.56	us
29	80	1	0	0	27.62	us
30	FF	0	1	0	23.33	us
31	80	1	0	0	27.63	us
32	FB	0	1	0	24.55	us
33	80	1	0	0	27.63	us
34	F0	0	1	1	23.33	us
35	80	1	0	1	28.86	us
36	E7	0	1	1	22.71	us
37	80	1	0	1	28.86	us
38	FD	0	1	1	22.71	us
39	80	1	0	1	27.62	us
40	FF	0	1	1	23.94	us
41	80	1	0	1	27.63	us
42	FE	0	1	1	23.94	us
43	80	1	0	1	27.62	us
44	F4	0	1	1	23.94	us
45	80	1	0	1	28.86	us
46	F0	0	1	1	22.71	us
47	80	1	0	1	28.86	us
48	E4	0	1	1	23.33	us
49	80	1	0	1	28.86	us
50	FC	0	1	0	22.10	us
51	80	1	0	0	27.63	us
52	FF	0	1	0	23.94	us
53	80	1	0	0	27.62	us
54	FF	0	1	0	24.56	us
55	80	1	0	0	27.62	us
56	FF	0	1	0	23.33	us
57	80	1	0	0	27.63	us
58	EF	0	1	0	24.55	us
59	80	1	0	0	28.86	us
60	E4	0	1	0	22.10	us
61	80	1	0	0	28.86	us
62	F9	0	1	0	22.71	us
63	80	1	0	0	27.63	us
64	FE	0	1	0	24.56	us
65	80	1	0	0	27.62	us
66	F9	0	1	1	23.33	us
67	80	1	0	1	27.63	us
68	EC	0	1	1	24.55	us
69	80	1	0	1	28.86	us

The captured listing above has several important pieces of information that bears a brief description. The columns depict different pieces of data. The leftmost column (Label Base) is a line number with reference to the trip point at element 0. The Data column represents hexadecimal byte captured from the DSP to TIP data bus. This holds information going to and from the DSP. The RD column denotes whether the data in the Data column is coming from the DSP (active when RD = 0). Similarly, the WR column indicates when the DSP is getting a command from the TIP (WR=0). The Gate column denotes when the signal simulator is enabled (1) or disabled (0) to spread the signal.

At base=0 (trip) the DSP confirms that it has acquired a signal by sending a hex C0 to the TIP processor. The TIP processor acknowledges and begins demodulating data by sending a demod command (hex 80, WR=0) for each successive bit interval thereafter. While in Demod mode, the DSP starts sending correlation sums in the subsequent bytes throughout the message.

If the Gate is connected to the signal simulator gate input, the correlation sum against the spread signal is active when Gate = 1. When Gate = 0, the input signal is CW and no correlation power is achieved. The difference between the correlated leader and the uncorrelated CW is the process gain achieved by the radio. The Gate signal alternates following trip every 8 RD assertions. Also, the real signal power may lag the Gate state change by a couple bit intervals.

Note: Process Gain measurement is only valid during the leader when known "ones" are being transmitted by the signal simulator since "zeros" are on-off-keyed.

Data captured using the logic analyzer must be parsed to remove the interleaved command messages from the TIP. The data power weight is explained further in the data interpretations section following.

Data Interpretations and Process Gain Methodology:

Process gain for a Direct Sequence Spread Spectrum system is defined as the ratio of the spread bandwidth to the information bandwidth or alternatively the SNR improvement that results from the spreading of the signal bandwidth. In order to measure the process gain provided by the application of the direct sequence coding, we can compare the correlation power output of the DSP correlator for the desired spreading code versus the correlation power of a CW signal at the same input power level. The measured difference in correlation power is the process gain introduced by the spreading/despreading function.

In order to accurately measure the CW correlation power relative to the spread signal power, the transmitter provides a gating function that allows the spreading code to be turned off and on during the message leader as shown in **Figure 3.1.4**. This allows measurements to be made of the correlation power of the spread signal versus a CW tone at the same power level.

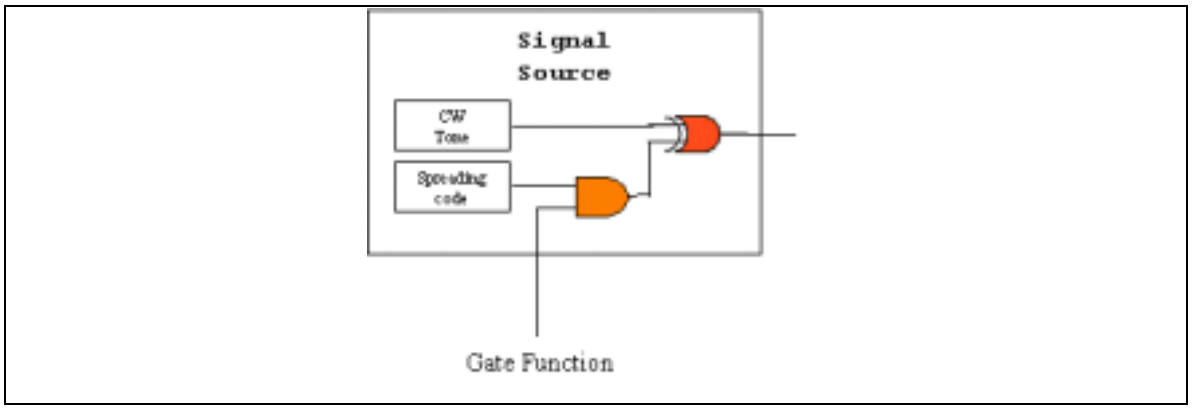


Figure 3.1.4
Spreading Function Gating Circuit

While the gate function is high, the CW signal is modulated by the spreading code and maximum correlation power is achieved ('1' bit value). When the gate function is low, only the CW tone is present and minimum correlation power is achieved ('0' bit value).

A logic analyzer is used to observe the correlation power values calculated by the DSP as shown in **Figure 3.1.5**.

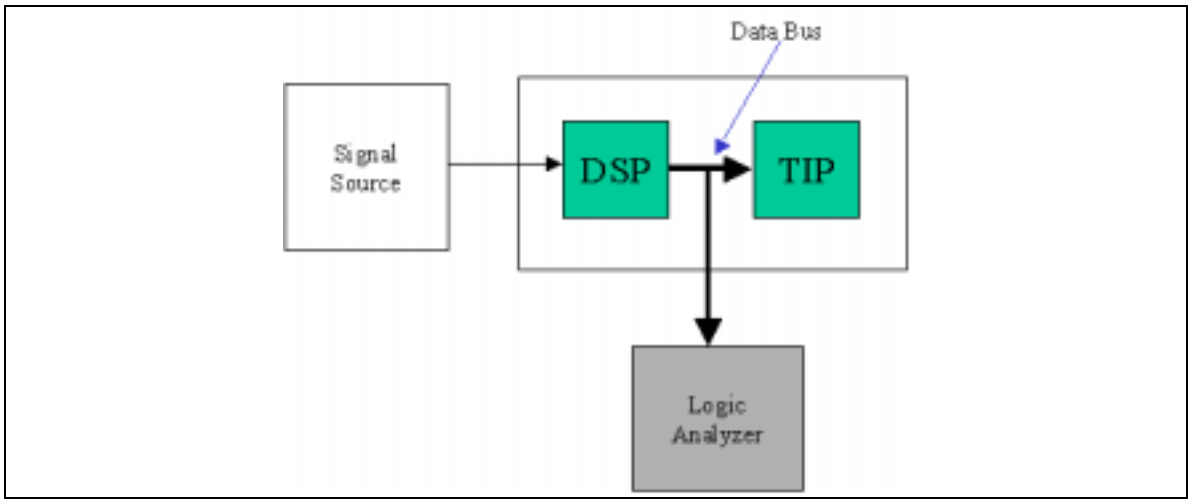


Figure 3.1.5
Data Acquisition Point

Figure 3.1.6 shows correlation power data from the DSP for a typical message. An all ones leader of 92 bits denotes the beginning of the message.

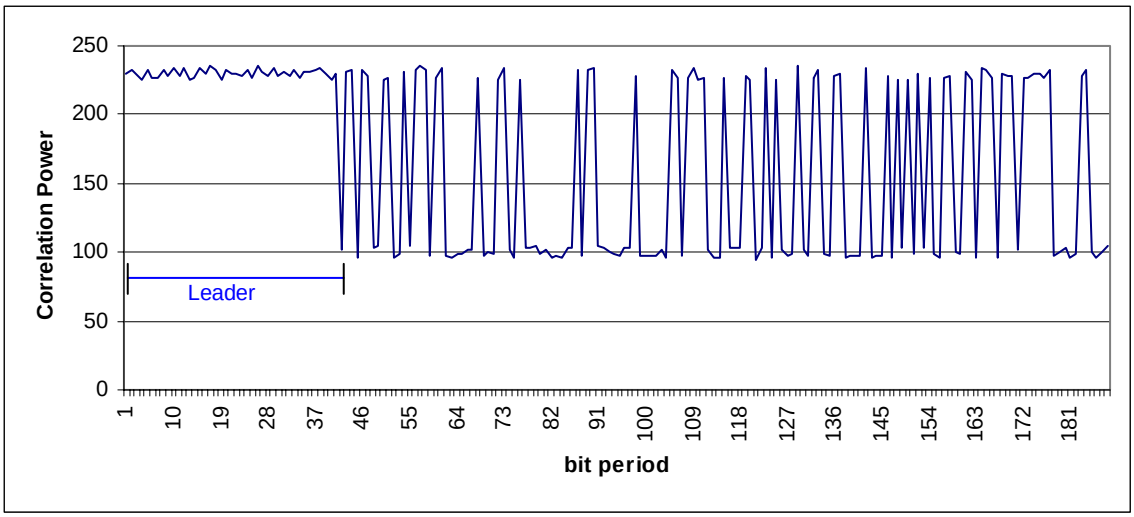
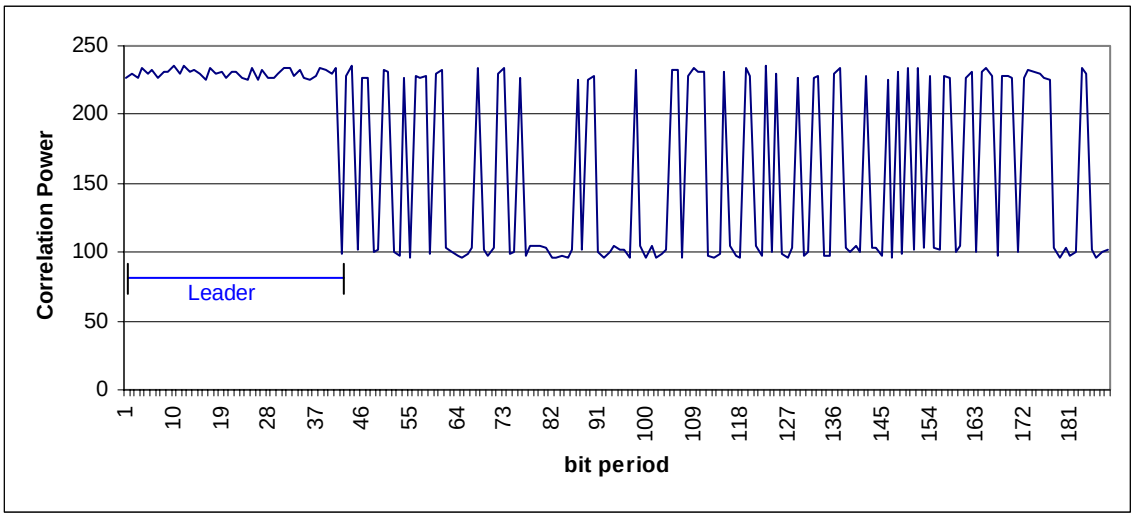
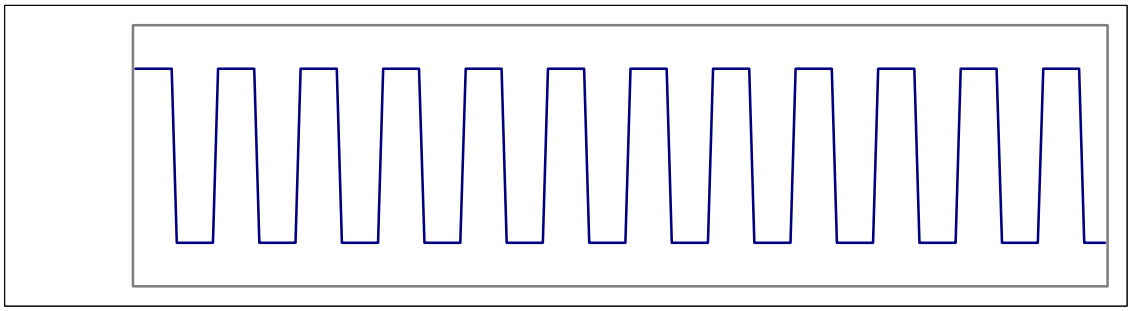


Figure 3.1.6
Correlation Power vs. bit period

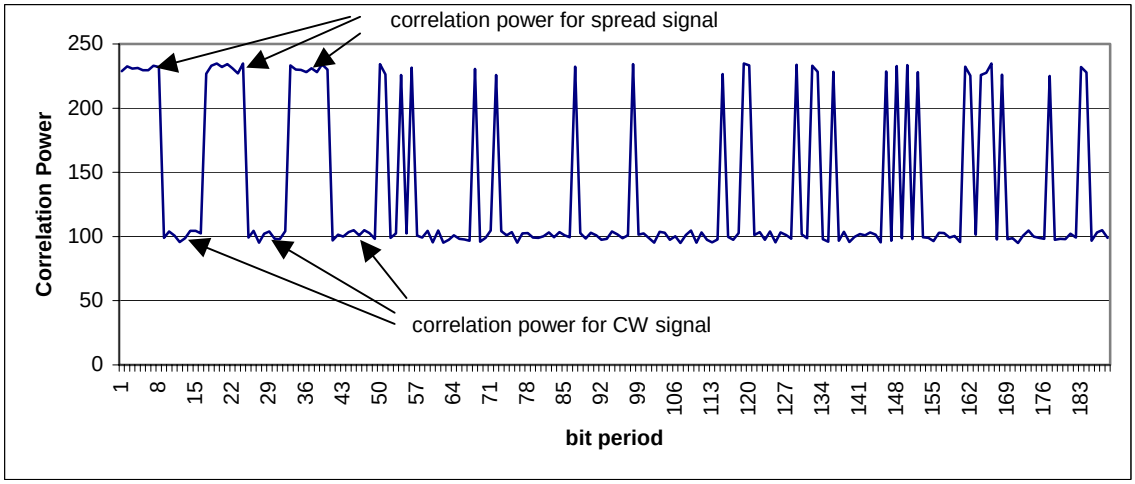
Figure 3.1.7 shows the result of the gating function on the original correlation power data. The minimum values now represent the correlation power of a pure CW signal while the maximum values represent the correlation power of the desired spread signal. Since the correlation power is sampled at baseband for both cases and the same CW tone is used for both the spread signal and the non-spread signal, the difference in correlation power represents the process gain of the system due to the despreading of the signal.



Original Spread Signal Correlation Power



Gating Function Signal



Resulting Correlation Power After Gating

Figure 3.1.7
Gating Function Applied To Transmitted Message

In order to calculate accurate values for the process gain, it is necessary to select the appropriate values from the collected data which represent only the spread signal and those values which represent only the CW signal.

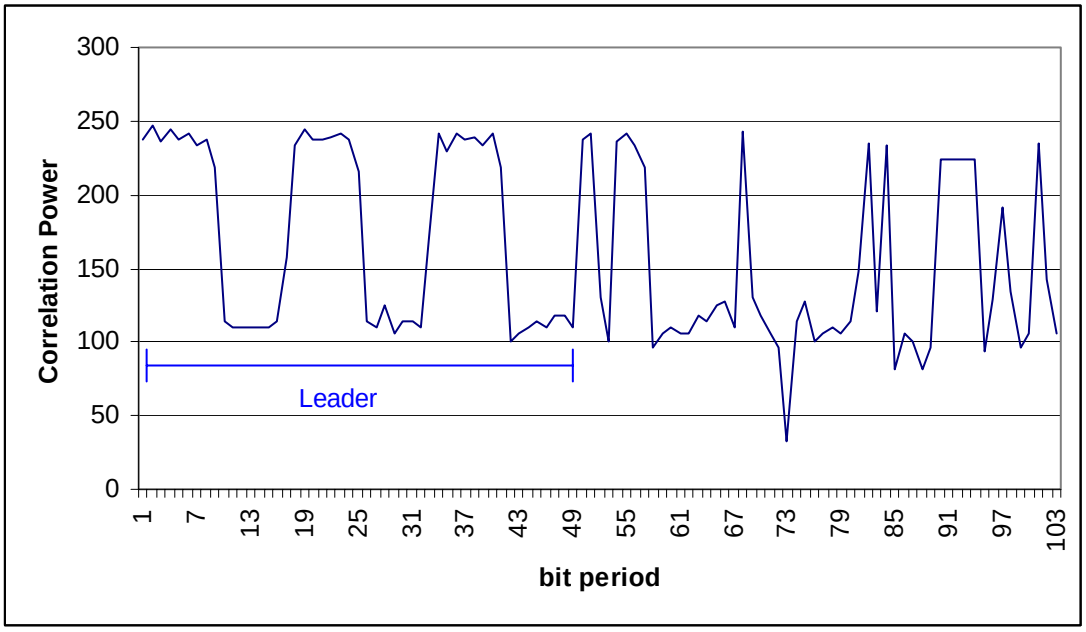


Figure 3.1.7
Captured Data Showing the Gated Leader

Figure 3.1.7 shows actual data captured from the logic analyzer for a –94 db input signal that has been gated as described above. The valid correlation values are contained in the leader which can be identified above as a symmetrical square-wave at the beginning of the message. Note that the leader consists of approximately 50 samples or bits out of the 92 '1's bits transmitted. This is because the trip algorithm requires about 40 samples in order to trip and begin demodulating the message.

First we need to discard the data following the leader. This results in the plot shown in **Figure 3.1.8** after selecting the first 50 samples.

142	114	237	114	241
237	110	238	114	218
247	110	239	110	101
236	110	241	170	106
245	110	237	242	110
237	110	216	230	114
241	114	114	241	110
233	157	110	238	118
237	234	125	239	118
218	244	106	234	110

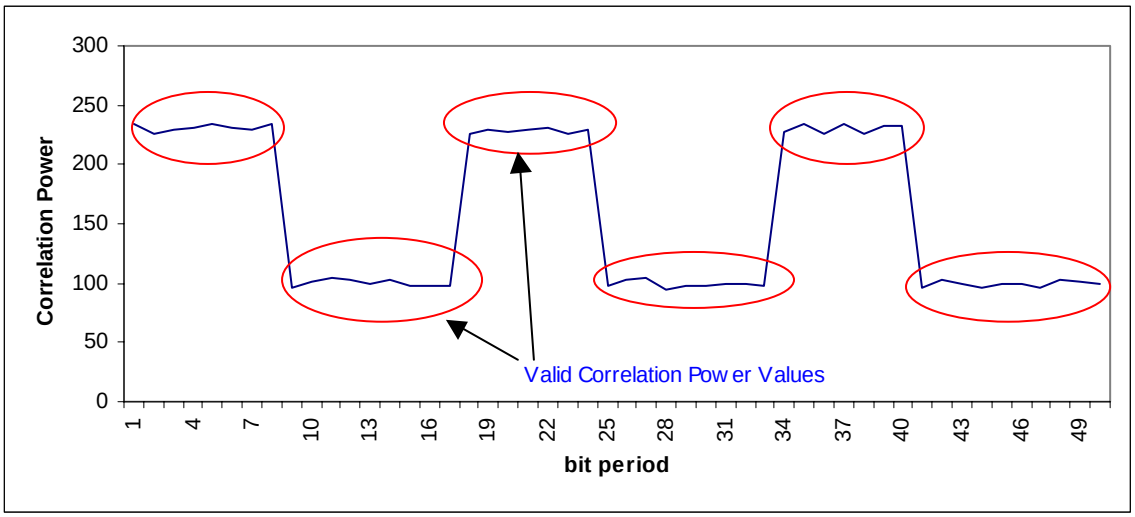


Figure 3.1.8

Now it is necessary to discard samples that occurred during the transitions of the gating function. This leaves only the valid correlation power values as shown in **Figure 3.1.9**.

	114	237	114	241
237	110	238	114	
247	110	239	110	101
236	110	241		106
245	110	237	242	110
237	110		230	114
241	114	114	241	110
233		110	238	118
237	234	125	239	118
	244	106	234	110

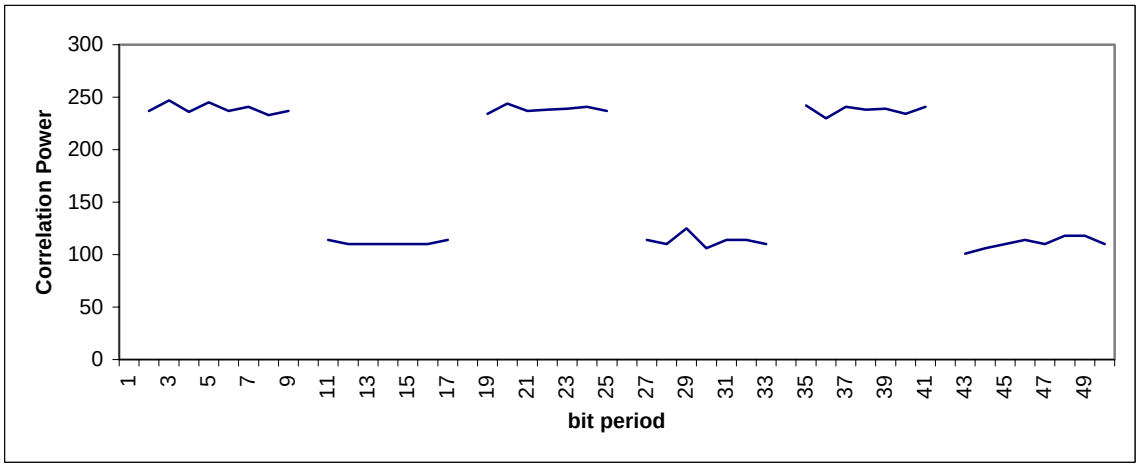


Figure 3.1.9
Valid Correlation Power

Now we convert the sample values representing the correlation power of the spread signal (maximums) to dB.

The DSP incorporates a look-up table to output the correlation power according to the following equation.

$$\textit{Correlation Power} = 10\ LOG_{10}(10^{samplevalue/106} \times 0.247)$$

Table 3.1-3

Spread Signal Correlation Power		CW Signal Correlation Power	
Sample Value	dB	Sample Value	dB
237	16.29	114	4.68
247	17.23	110	4.31
236	16.19	110	4.31
245	17.04	110	4.31
237	16.29	110	4.31
241	16.66	110	4.31
233	15.91	114	4.68
237	16.29	114	4.68
234	16.00	110	4.31
244	16.95	125	5.72
237	16.29	106	3.93
238	16.38	114	4.68
239	16.48	114	4.68
241	16.66	110	4.31
237	16.29	101	3.46
242	16.76	106	3.93
230	15.63	110	4.31
241	16.66	114	4.68
238	16.38	110	4.31
239	16.48	118	5.06
234	16.00	118	5.06
241	16.66	110	4.31
Mean	16.43		4.47

Now we take the difference of the calculated means for the spread signal correlation power and the CW signal correlation power and we achieve a process gain of 11.96 dB.

16.43 – 4.47 = 11.96 dB process gain