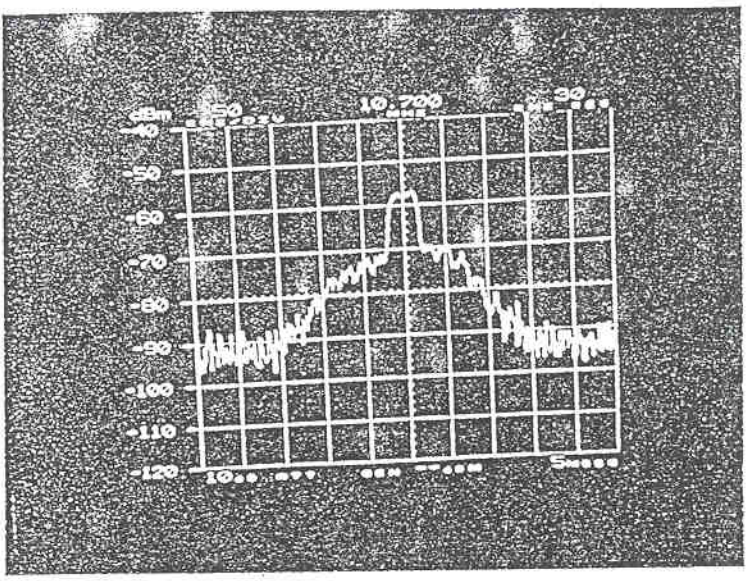

Exhibit V, Illustration V-I

Same setup as Illustration V-H with the exception that the Mini Circuits RF switch at 900 MHz has been replaced with a 3 dB splitter/combiner to apply both spread spectrum and CW signals to the receiver input at the same power. Jamming SNR = 12 dB.

TEST #3

Test Configuration #3. The 1496 output is connected to the NE604A through the Murata 110 kHz bandpass filter (normal operating condition). The integrated RSSI signal is probed with the LeCroy scope at the A to D input of the master processor. This signal will change 500 mV for each 10 dB change in signal strength input to the NE604A (100 mV for 2 dB, 50 mV for 1 dB, etc.). The Mini Circuits RF switch is switched between CW and correlated spread spectrum output (ie. the selected spread spectrum output signal from the Mini Circuits mixer generated by the chipping code from the PRC generator is in synchronization with the chipping signal presented to the receiver's 1496 decorrelator). This produces a voltage change at the A to D input of the master processor (via the integrator circuit) whose peak to peak voltage will show the processing gain of the receiver, as the master processor encounters it. This RSSI signal is used for all system acquisition and data demodulation functions and is the correct "demodulator output" to measure in our system to show compliance with 15.247(e) when the peak to peak voltage excursion is scaled with the 500 mV per 10 dB factor mentioned above (ie. 13 dB of process gain would produce a 650 mV peak to peak signal.).

The following Illustration V-J shows the oscilloscope readings of RSSI (signal) detector change at input to master processor A to D converter for three receiver signal strength inputs at 900 MHz showing minimal indication of process gain at 12 dB.

Integrated RSSI Voltage Readings vs. Signal Strength Input for the Axonn 0536-0200 Receiver with A Spread Spectrum Input Signal vs. A CW Input Signal of the Same Magnitude

SIGNAL LEVEL at 900 MHz (dBm)	RSSI LEVEL (mV)		DELTA (mV)
	CW	SPREAD SPECTRUM	
-90.0	895	1535	640
-80.0	1365	2100	735
-70.0	1960	2755	795
-60.0	2590	3225	635
-50.0	3050	3600	550

Exhibit V, Illustration V-J

NOTE: Although the RSSI delta value indicates that the process gain exceeds 12 dB in some cases, this is caused by the non-monotonic nature of the NE604 detector in its mid-band region. The readings that show the smallest deltas are the most accurate.

Testing Performed By:

Robert J. Davis, Senior RF Engineer
Axonn Corporation

Date
Axonn Corporation 0536-0200

SYSTEM PROCESSING GAIN CALCULATIONS

PROCESSING GAIN FORMULA:

Processing Gain PG (dB) = 10 * LOG (RF Bandwidth/Information Rate)

SYSTEM CONSTANTS:

Chip Clock	=	14.66 MHz/12	=	1.2217 MHz
Chip Duration	=	1/Chip Clock	=	0.8186 µSec
Bit Time	=	63 * 0.8186 µSec	=	51.5718 µSec

(One Code Repetition Per Bit, 63 Chip Code)

Bit Rate	=	1/Bit Time	=	19.3904 kHz
Narrowest Filter Bandwidth After Correlator			=	110 kHz

STATED PROCESSING GAIN:

Since the system utilizes a 110 kHz bandpass filter after the correlator it is correct to express the process gain derived from the bandwidth of this filter. This gives a correct answer (which is less) than using the system data rate from the "textbook".

For RF Bandwidth	=	2 * 1.2217 MHz	=	2.4434 MHz
PG (dB)	=	10 * LOG(2.4423/0.110)	=	13.4 dB

IMPLEMENTATION LOSSES:

Eighth Chip Acquisition Ambiguity	1 dB
2 MHz BPF	0.5 dB
Elliptic Filter on PRC	0.9 dB
Total	2.4 dB

13.4 - 2.4 dB yields minimal PG of 11 dB for worse case acquisition ambiguity. Theoretical differs from measured by approximately 1 dB in asmuch as the system produces a measured processing gain of 12 dB.

Source: "Spread Spectrum Systems" Robert C. Dixon, John Wiley and Sons © 1984, pp 258 and 259.