WIRELESS

locate, communicate, accelerate

LEON-G100/G200

quad-band GSM/GPRS Data and Voice Modules

System Integration Manual

Abstract

This document describes the features and integration of the LEON-G100/G200 quad-band GSM/GPRS data and voice modules.
The LEON-G100/G200 are complete and cost efficient solutions, bringing full feature quad-band GSM/GPRS data and voice transmission technology in a compact form factor.

29.5 x 18.9 x 3.0 mm

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Document Information	
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Document status information	
Objective Specification	This document contains target values. Revised and supplementary data will be published later.
Advance Information	This document contains data based on early testing. Revised and supplementary data will be published later.
Preliminary	This document contains data from product verification. Revised and supplementary data may be published later.
Released	This document contains the final product specification.

This document applies to the following products:

Name	Type number	Firmware version	PCN / IN
LEON-G100	LEON-G100-04S-00	07.40.01	GSM.G1-SW-10007
	LEON-G100-05S-00	07.50.00	GSM.G1-SW-10008
	LEON-G100-05A-00	07.50.00	N.A.
LEON-G200	LEON-G200-04S-00	07.40.01	GSM.G1-SW-10007
	LEON-G200-05S-00	07.50.00	GSM.G1-SW-10008

Preface

u-blox Technical Documentation

As part of our commitment to customer support, u-blox maintains an extensive volume of technical documentation for our products. In addition to our product-specific technical data sheets, the following manuals are available to assist u-blox customers in product design and development.

AT Commands Manual: This document provides the description of the supported AT commands by the LEON GSM/GPRS Voice and Data Modules to verify all implemented functionalities.

System Integration Manual: This Manual provides hardware design instructions and information on how to set up production and final product tests.

Application Note: document provides general design instructions and information that applies to all u-blox Wireless modules. See Section Related documents for a list of Application Notes related to your Wireless Module.

How to use this Manual

The LEON-G100/G200 System Integration Manual provides the necessary information to successfully design in and configure these u-blox wireless modules.

This manual has a modular structure. It is not necessary to read it from the beginning to the end.

The following symbols are used to highlight important information within the manual:

An index finger points out key information pertaining to module integration and performance.

A warning symbol indicates actions that could negatively impact or damage the module.

Questions

If you have any questions about u-blox Wireless Integration, please:

- Read this manual carefully.
- Contact our information service on the homepage http://www.u-blox.com
- Read the questions and answers on our FAQ database on the homepage http://www.u-blox.com

Technical Support

Worldwide Web

Our website (www.u-blox.com) is a rich pool of information. Product information, technical documents and helpful FAQ can be accessed 24h a day.

By E-mail

Contact the nearest of the Technical Support offices by email. Use our service pool email addresses rather than any personal email address of our staff. This makes sure that your request is processed as soon as possible. You will find the contact details at the end of the document.

Helpful Information when Contacting Technical Support

When contacting Technical Support please have the following information ready:

- Module type (e.g. LEON-G100) and firmware version
- Module configuration
- Clear description of your question or the problem
- A short description of the application
- Your complete contact details

Contents

1 System description

1.1 Overview

LEON-G100/G200 GSM/GPRS modules integrate a full-featured Release 99 GSM-GPRS protocol stack, with the following main characteristics.

- Quad band support: GSM 850 MHz, EGSM 900 MHz, DCS 1800 MHz and PCS 1900 MHz
- Power class 4 (33 dBm nominal maximum output power) for GSM/EGSM bands
- Power class 1 (30 dBm nominal maximum output power) for DCS/PCS bands
- GPRS multi-slot class 10
- All GPRS coding schemes from CS1 to CS4 are supported
- GPRS bit rate: 85.6 kb/s (max.), 53.6 kb/s (typ.) in down-link; 42.8 kb/s (max.), 26.8 kb/s (typ.) in up-link
- CS (Circuit Switched) Data calls are supported in transparent/non transparent mode up to 9.6 kb/s
- Encryption algorithms A5/1 for GSM and GPRS support
- Bearer service fax Group 3 Class 2.0 support
- Class B Mobile Stations (i.e. the data module can be attached to both GPRS and GSM services, using one service at a time)
- Network operation modes I to III are supported

GPRS multi-slot class determines the maximum number of timeslots available for upload and download and thus the speed at which data can be transmitted and received: higher classes typically allow faster data transfer rates. GPRS multi-slot class 10 uses a maximum of 4 slots in download (reception) and 2 slots in upload (transmission), with 5 slots in total.

The network automatically configures the number of timeslots used for reception or transmission (voice calls take precedence over GPRS traffic). The network also automatically configures channel encoding (CS1 to CS4).

The maximum GPRS bit rate of the mobile station depends on the coding scheme and number of time slots.

1.2 Architecture

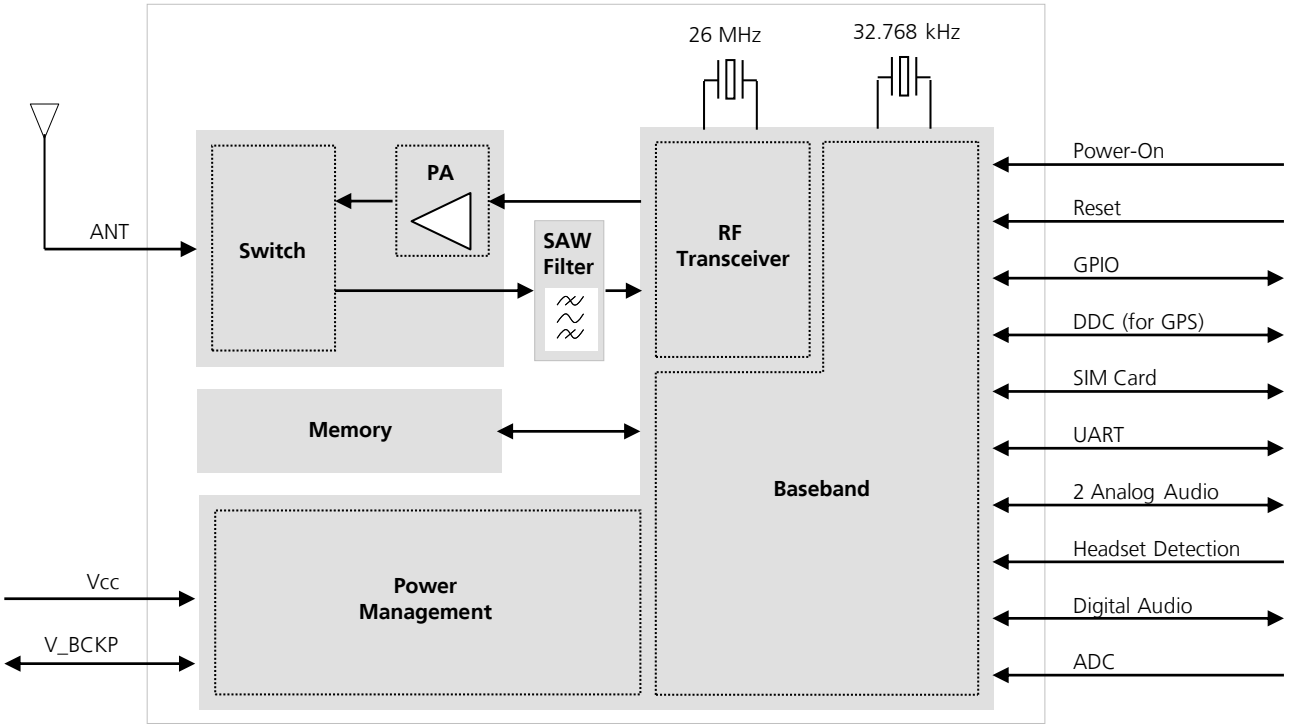

Figure 1: LEON-G100 block diagram

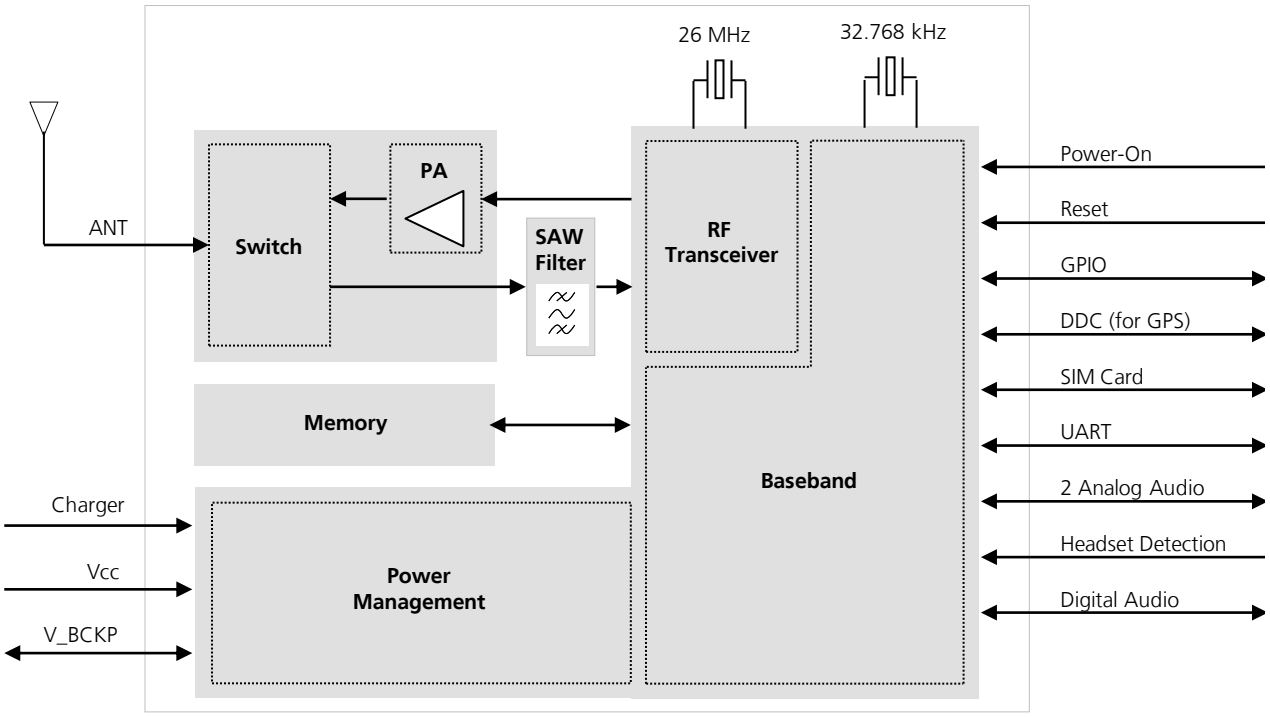

Figure 2: LEON-G200 block diagram

1.2.1 Functional blocks

LEON-G100/G200 modules consist of the following functional blocks:

- RF
- Baseband
- Power Management

1.2.1.1 RF

The RF block is composed of the following main elements:

- RF transceiver (integrated in the GSM/GPRS single chip) performing modulation, up-conversion of the baseband I/Q signals, down-conversion and demodulation of the RF received signals. The RF transceiver includes:
  - Constant gain direct conversion receiver with integrated LNAs;
  - Highly linear RF quadrature demodulator;
  - Digital Sigma-Delta transmitter modulator;
  - Fractional-N Sigma-Delta RF synthesizer;
  - 3.8 GHz VCO;
  - Digital controlled crystal oscillator.
- Transmit module, which amplifies the signals modulated by the RF transceiver and connects the single antenna input/output pin of the module to the suitable RX/TX path, via its integrated parts:
  - Power amplifier;
  - Antenna switch;
- RX diplexer SAW (band pass) filters
- 26 MHz crystal, connected to the digital controlled crystal oscillator to perform the clock reference in active or connected mode

1.2.1.2 Baseband

The Baseband block is composed of the following main elements:

- Baseband integrated in the GSM/GPRS single chip, including:
  - Microprocessor;
  - DSP (for GSM/GPRS Layer 1 and audio processing);
  - Peripheral blocks (for parallel control of the digital interfaces);
  - Audio analog front-end;
- Memory system in a multi-chip package integrating two devices:
  - NOR flash non-volatile memory;
  - PSRAM volatile memory;
- 32.768 kHz crystal, connected to the oscillator of the RTC to perform the clock reference in idle or power-off mode

1.2.1.3 Power Management

The Power Management block is composed of the following main elements:

- Voltage regulators integrated in the GSM/GPRS single chip for direct connection to battery
- Charging control circuitry

1.2.2 Hardware differences between LEON-G100 and LEON-G200

Hardware differences between the LEON-G100 and the LEON-G200 modules:

- Charging control circuitry is available on the LEON-G200 module only
- ADC input is provided on the LEON-G100 module only

1.3 Pin-out

Table 1 describes the pin-out of LEON-G100/G200 modules, with pins grouped by function.

Function	Pin	No	I/O	Description	Remarks
Power	**VCC**	50	I	Module Supply	Clean and stable supply is required: low ripple and low voltage drop must be guaranteed. Voltage provided has to be always above the minimum limit of the operating range. Consider that there are large current spike in connected mode, when a GSM call is enabled. See section 1.5.2
	GND	1, 3, 6, 7, 8, 17, 25, 36, 45, 46, 48, 49	N/A	Ground	GND pins are internally connected but good (low impedance) external ground can improve RF performances: all GND pins must be externally connected to ground
	V_BCKP	2	I/O	Real Time Clock supply	V_BCKP = 2.0 V (typical) generated by the module to supply Real Time Clock when VCC supply voltage is within valid operating range. See section 1.5.5
	VSIM	35	O	SIM supply	SIM supply automatically generated by the module. See section 1.8
	V_CHARGE - (LEON-G200)	4	I	Charger voltage supply input	**V_CHARGE and CHARGE_SENSE must be externally connected.** The external supply used as charging source must be voltage and current limited. See section 1.5.4
	CHARGE_SENSE (LEON-G200)	5	I	Charger voltage measurement input	**V_CHARGE and CHARGE_SENSE must be externally connected.** The external supply used as charging source must be voltage and current limited. See section 1.5.4
RF	**ANT**	47	I/O	RF antenna	50 Ω nominal impedance. See section 1.7, 2.2.1.1 and 2.4
Audio	**HS_DET**	18	I	Headset detection input	Internal active pull-up to 2.85 V enabled. See section 1.10.1.3
	I2S_WA	26	O	I^2S word alignment	I^2S Interface: see section 1.10.2. Check device specifications to ensure compatibility of supported modes to LEON-G100/G200 module. Add a test point to provide access to the pin for debugging.
	I2S_TXD	27	O	I^2S transmit data	I^2S Interface: see section 1.10.2. Check device specifications to ensure compatibility of supported modes to LEON-G100/G200 module. Add a test point to provide access to the pin for debugging.
	I2S_CLK	28	O	I^2S clock	I^2S Interface: see section 1.10.2. Check device specifications to ensure compatibility of supported modes to LEON-G100/G200 module. Add a test point to provide access to the pin for debugging.
	I2S_RXD	29	I	I^2S receive data	I^2S Interface: see section 1.10.2. Internal active pull-up to 2.85 V enabled. Check device specifications to ensure compatibility of supported modes to LEON-G100/G200 module. Add a test point to provide access to the pin for debugging.
	HS_P	37	O	First speaker output with low power single-ended analog audio	This audio output is used when audio downlink path is “Normal earpiece” or “Mono headset” Audio pin: see section 1.10.1
	SPK_P	38	O	Second speaker output with high power differential analog audio	This audio output is used when audio downlink path is “Loudspeaker”. Audio pin: see section 1.10.1

Function	Pin	No	I/O	Description	Remarks
	SPK_N	39	O	Second speaker output with power differential analog audio output	This audio output is used when audio downlink path is "Loudspeaker". Audio pin: see section 1.10.1
	MIC_BIAS2	41	I	Second microphone analog signal input and bias output	This audio input is used when audio uplink path is set as "Headset Microphone". Audio pin: see section 1.10.1
	MIC_GND2	42	I	Second microphone analog reference	Local ground of second microphone. Audio pin: see section 1.10.1
	MIC_GND1	43	I	First microphone analog reference	Local ground of the first microphone. Audio pin: see section 1.10.1
	MIC_BIAS1	44	I	First microphone analog signal input and bias output	This audio input is used when audio uplink path is set as "Handset Microphone". Audio pin: see section 1.10.1
SIM	**SIM_CLK**	32	O	SIM clock	SIM interface: see section 1.8. Must meet SIM specifications
	SIM_IO	33	I/O	SIM data	SIM interface: see section 1.8. Internal 4.7k pull-up to VSIM. Must meet SIM specifications
	SIM_RST	34	O	SIM reset	SIM interface: see section 1.8. Must meet SIM specifications
UART	**DSR**	9	O	UART data set ready	Circuit 107 (DSR) in V.24. See section 1.9.1.
	RI	10	O	UART ring indicator	Circuit 125 (RI) in V.24. See section 1.9.1.
	DCD	11	O	UART data carrier detect	Circuit 109 (DCD) in V.24. See section 1.9.1.
	DTR	12	I	UART data terminal ready	Internal active pull-up to 2.85 V enabled. Circuit 108/2 (DTR) in V.24. See section 1.9.1.
	RTS	13	I	UART ready to send	Internal active pull-up to 2.85 V enabled. Circuit 105 (RTS) in V.24. See section 1.9.1.
	CTS	14	O	UART clear to send	Circuit 106 (CTS) in V.24. See section 1.9.1.
	TxD	15	I	UART transmitted data	Internal active pull-up to 2.85 V enabled. Circuit 103 (TxD) in V.24. See section 1.9.1.
	RxD	16	O	UART received data	Circuit 104 (RxD) in V.24. See section 1.9.1.
DDC	**SCL**	30	O	I^2C bus clock line	**Fixed open drain. External pull-up required.** See section 1.9.2
	SDA	31	I/O	I^2C bus data line	**Fixed open drain. External pull-up required.** See section 1.9.2
ADC	**ADC1 (LEON-G100)**	5	I	ADC input	Resolution: 12 bits. See section 1.11; consider that the impedance of this input changes depending on the operative mode
GPIO	**GPIO1**	20	I/O	GPIO	See section 1.12. Add a test point to provide access to the pin for debugging.
	GPIO2	21	I/O	GPIO	See section 1.12
System	**PWR_ON**	19	I	Power-on input	**PWR_ON pin has high input impedance. Do not keep floating in noisy environment: external pull-up required.** See section 1.6.1
	RESET_N	22	I/O	Reset signal	See section 1.6.3
Reserved	**Reserved**	23			Do not connect
	Reserved	24			Do not connect
	Reserved	40			Do not connect
	Reserved (LEON-G100)	4			Do not connect

Table 1: LEON-G100/G200 pin-out

1.4 Operating modes

LEON-G100/G200 modules include several operating modes, each have different features and interfaces. Table 2 summarizes the various operating modes and provides general guidelines for operation.

Operating Mode	Description	Features / Remarks	Transition condition
General Status: Power-down			
Not-Powered Mode	VCC supply not present or below normal operating range. Microprocessor not operating. RTC only operates if supplied through **V_BCKP** pin.	Module is switched off. Application interfaces are not accessible. Internal RTC timer operates only if a valid voltage is applied to **V_BCKP** pin. Any external signal connected to UART I/F, I^2S I/F, HS_DET, or a GPIO must be set low or tri-stated to avoid an increase of module power-off consumption.	Module cannot be switched on by a falling edge provided on the **PWR_ON** input, neither by a preset RTC alarm, nor by charger detection on the **V_CHARGE** and **CHARGE_SENSE** pins.
Power-Off Mode	**VCC** supply within normal operating range. Microprocessor not operating. Only RTC runs.	Module is switched off: normal shutdown after sending the AT+CPWROFF command (refer to u-blox 2G GSM/GPRS AT Commands Manual [2]). Application interfaces are not accessible. Only internal RTC in operation. Any external signal connected to the UART I/F, I^2S I/F, **HS_DET** pin, or a GPIO must be set low or tri-stated to avoid an increase of the module power-off consumption.	Module can be switched on by a falling edge provided on the **PWR_ON** input, by a preset RTC alarm, or by charger detection on the **V_CHARGE** and **CHARGE_SENSE** pins.
General Status: Normal Operation			
Idle-Mode	Microprocessor runs with 32 kHz as reference oscillator. Module does not accept data signals from an external device.	If power saving is enabled, the module automatically enters idle mode whenever possible. Application interfaces are disabled. If hardware flow control is enabled, the **CTS** line indicates when the module is in idle (power saving configuration): the line is driven in the OFF state when the module is not prepared to accept data signals. If hardware flow control is disabled, the **CTS** line is fixed to ON state. Module by default is not set to automatically enter in idle mode whenever possible, unless power saving configuration is enabled by appropriate AT command (refer to u-blox 2G GSM/GPRS AT Commands Manual [2], AT+UPSV).	If the module is registered with the network and power saving is enabled, it automatically goes in idle mode and periodically wakes up to active mode to monitor the paging channel for the paging block reception according to network indication. If module is not registered with the network and power saving is enabled, it automatically enters idle mode and periodically wakes up to monitor external activity. Module wakes up from idle mode to active mode if an RTC alarm occurs. Module wakes up from idle mode to active mode when data is received on UART interface (refer to 1.9.1 for more details). Module wakes up from idle mode to active mode if a voice or data call incoming. Module wakes up from idle mode to active mode when the RTS input line is set to the ON state by the DTE if the AT+UPSV=2 command is sent to the module (feature not enabled by default).
Active-Mode	Microprocessor runs with 26 MHz as reference oscillator. The module is ready to accept data signals from an external device.	Module is switched on and is fully active: power saving is not enabled. The application interfaces are enabled.	

Operating Mode	Description	Features / Remarks	Transition condition
Connected-Mode	Voice or data call enabled. Microprocessor runs with 26 MHz as reference oscillator. Module is ready to accept data signals from an external device.	The module is switched on and a voice call or a data call (GSM/GPRS) is in progress. Module is fully active. Application interfaces are enabled. When call terminates, module returns to the last operating state (Idle or Active).	
General Status: Charging (LEON-G200 only)			
Pre-charge mode	Battery connected to **VCC**. Battery voltage level is below the **VCC** normal operating range. Charger connected to **V_CHARGE** and **CHARGE_SENSE** inputs with proper voltage and current characteristics. Charging of the deeply discharged battery is enabled while the module is switched off.	Module is switched off and cannot be switched on (not powered mode). The Pre-Charge phase of the charging process is enabled: charging of the deeply discharged battery is forced by HW at low current while the module is switched off	
Charge-mode	Battery connected to **VCC**. Battery voltage level is within the VCC normal operating range. Charger connected to **V_CHARGE** and **CHARGE_SENSE** inputs with proper voltage and current characteristics. Charging process enabled while the module is switched on and normal operations are enabled.	Module is switched on and normal operations are enabled (Idle mode, Active mode or Connected mode). The charging process is enabled: charging of battery is controlled by the microprocessor while the module is switched on	

Table 2: Module operating modes summary

1.5 Power management

1.5.1 Power supply circuit overview

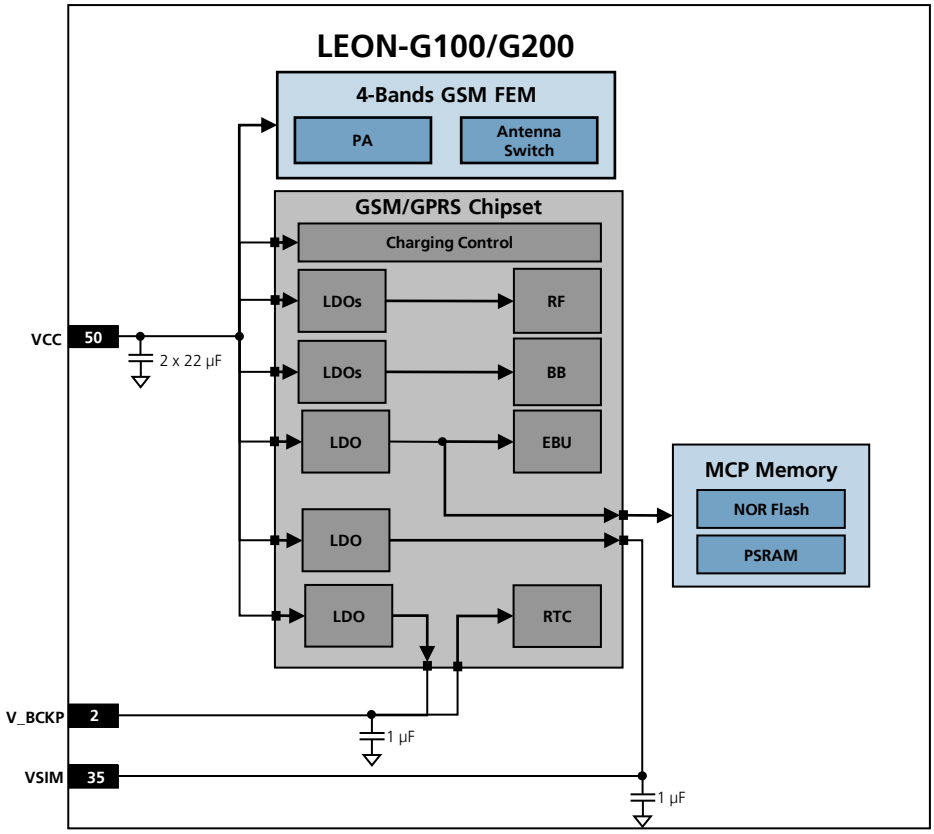

Figure 3: Power supply concept

Power supply is via **VCC** pin. This is the only one main power supply pin.

VCC pin connects the RF Power Amplifier and the integrated power management unit within the module: all supply voltages needed by the module are generated from the **VCC** supply by integrated voltage regulators.

V_BCKP is the Real Time Clock (RTC) supply. When the **VCC** voltage is within the specified extended operating range, the module supplies the RTC: 2.0 V typical are generated by the module on the **V_BCKP** pin. If the **VCC** voltage is under the minimum specified extended limit, the RTC can be externally supplied via **V_BCKP** pin.

When a 1.8 V or a 3 V SIM card type is connected, LEON-G100/G200 automatically supply the SIM card via **VSIM** pin. Activation and deactivation of the SIM interface with automatic voltage switch from 1.8 to 3 V is implemented, in accordance to the ISO-IEC 78-16-e specifications.

The integrated power management unit also provides the control state machine for system start up, including start up with discharged batteries, pre-charging and system reset control.

LEON-G100/G200 feature a power management concept optimized for most efficient use of battery power. This is achieved by hardware design utilizing power efficient circuit topology, and by power management software controlling the power saving configuration of the module. Battery management runs in the context of the operation and maintenance process:

- Battery charging control, in order to maintain the full capacity of the battery
- Collecting and processing of measurements of battery voltage

1.5.2 Module supply (VCC)

LEON-G100/G200 modules must be supplied through **VCC** pin by a DC power supply. Voltages must be stable, due to the surging consumption profile of the GSM system (described in the section 1.5.3).

Name	Description	Remarks
VCC	Module Supply	Clean and stable supply is required: low ripple and low voltage drop must be guaranteed. Voltage provided has to be always above the minimum limit of the operating range. Consider that there are large current spike in connected mode, when a GSM call is enabled.
GND	Ground	GND pins are internally connected but good (low impedance) external ground can improve RF performances: all GND pins must be externally connected to ground.

Table 3: Module supply pins

☞ **VCC** pin ESD rating is 1 kV (contact discharge). A higher protection level could be required if the line is externally accessible on the application board. A higher protection level can be achieved mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) on the line connected to this pin if it is externally accessible on the application board.

The voltage provided to **VCC** pin must be within the normal operating range limits specified in the LEON-G100/G200 Data Sheet [1]. Complete functionality of the module is only guaranteed within the specified operational normal voltage range.

☞ Note that the module cannot be switched on if the **VCC** voltage value is below the specified normal operating range minimum limit: ensure that the input voltage at **VCC** pin is above the minimum limit of the normal operating range for more than 1 second after the start of the switch-on of the module.

When LEON-G100/G200 modules are in operation, the voltage provided to **VCC** pin can exceed the normal operating range limits but must be within the extended operating range limits specified in LEON-G100/G200 Data Sheet [1]. Module reliability is only guaranteed within the specified operational extended voltage range.

☞ Note that the module switches off when **VCC** voltage value drops below the specified extended operating range minimum limit: ensure that the input voltage at **VCC** pin never drops below the minimum limit of the extended operating range when the module is switched on, not even during a GSM transmit burst, where the current consumption can rise up to maximum peaks of 2.5 A in case of a mismatched antenna load.

⚠ **Operation above the extended operating range maximum limit is not recommended and extended exposure beyond it may affect device reliability.**

⚠ **Stress beyond the VCC absolute maximum ratings may cause permanent damage to the module: if necessary, voltage spikes beyond VCC absolute maximum ratings must be limited to values within the specified boundaries by using appropriate protection.**

☞ When designing the power supply for the application, pay specific attention to power losses and transients. The DC power supply has to be able to provide a voltage profile to the VCC pin with the following characteristics:

- Voltage drop during transmit slots has to be lower than 400 mV
- Undershoot and overshoot at the start and at the end of transmit slots have to be not present
- Voltage ripple during transmit slots has to be:
  lower than 100 mVpp if $f_{ripple} \leq 200$ kHz
  lower than 10 mVpp if 200 kHz $< f_{ripple} \leq 400$ kHz
  lower than 2 mVpp if $f_{ripple} > 400$ kHz

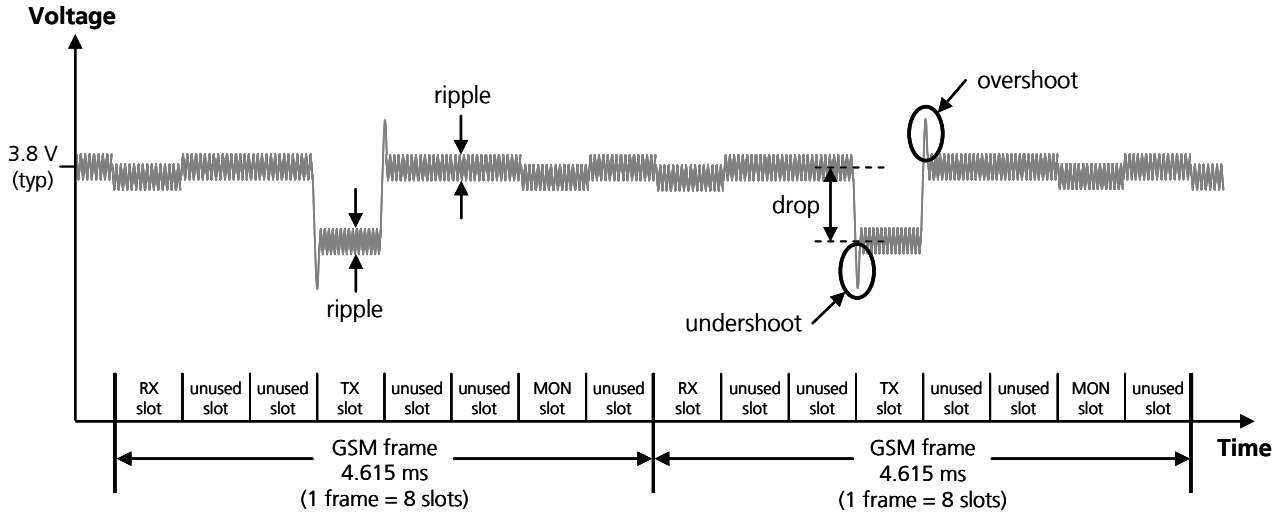

Figure 4: Description of the VCC voltage profile versus time during a GSM call

☞ Any degradation in power supply performance (due to losses, noise or transients) will directly affect the RF performance of the module since the single external DC power source indirectly supplies all the digital and analog interfaces, and also directly supplies the RF power amplifier (PA).

1.5.2.1 VCC application circuits

The LEON module must be supplied through the **VCC** pin by one (and only one) proper DC power supply from the following:

- Switching regulator
- Low Drop-Out (LDO) linear regulator
- Rechargeable Li-Ion battery
- Primary (disposable) battery

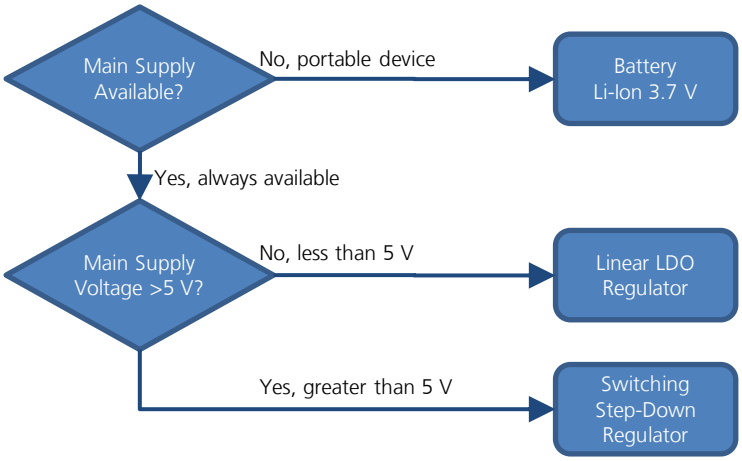

Figure 5: VCC supply concept selection

The switching step-down regulator is the typical choice when the available primary supply source has a nominal voltage much higher (e.g. greater than 5 V) than the LEON-G100/G200 operating supply voltage. The use of switching step-down provides the best power efficiency for the overall application and minimizes current drawn from main supply source.

The use of an LDO linear regulator becomes convenient for primary supplies with relatively low voltage (e.g. less than 5 V). In this case a switching regulator with a typical efficiency of 90% reduces the benefit of voltage step-down for input current savings. Linear regulators are not recommended for high voltage step-down as they will dissipate a considerable amount of power in thermal energy.

If the LEON-G100/G200 is deployed in a mobile unit with no permanent primary supply source available, then a battery is required to provide **VCC**. A standard 3-cell Lithium-Ion battery pack directly connected to **VCC** is the typical choice for battery-powered devices. Batteries with Ni-MH chemistry should be avoided, since they typically reach a maximum voltage during charging that is above the maximum rating for **VCC**.

The use of primary (disposable) batteries is uncommon, since the typical cells available are seldom capable of delivering the burst peak current for a GSM call due to high internal resistance.

The following sections highlight some design aspects for each of these supplies.

Switching regulator

The characteristics of the switching regulator connected to the **VCC** pin should meet the following requirements:

- **Power capabilities**: the switching regulator with its output circuit must be capable of providing a proper voltage value to the **VCC** pin and delivering 2.5 A current pulses with a 1/8 duty cycle to the **VCC** pin
- **Low output ripple**: the switching regulator and output circuit must be capable of providing a clean (low noise) VCC voltage profile
- **High switching frequency:** for best performance and for smaller applications select a switching frequency ≥ 600 kHz (since an L-C output filter is typically smaller for high switching frequency). Using a switching regulator with a variable switching frequency or with a switching frequency lower than 600 kHz must be carefully evaluated since this can produce noise in the **VCC** voltage profile and therefore impact and worsen GSM modulation spectrum performance. An additional L-C low-pass filter between the switching regulator output and the **VCC** supply pin can mitigate the ripple on **VCC,** but adds extra voltage drop due to resistive losses in series inductors
- **PWM mode operation**: select preferably regulators with Pulse Width Modulation (PWM) mode. Pulse Frequency Modulation (PFM) mode and PFM/PWM mode transitions while in active mode must be avoided to reduce the noise on the **VCC** voltage profile. Switching regulators able to switch between low ripple

PWM mode and high efficiency burst or PFM mode can be used, provided the mode transition occurs when the GSM module changes status from idle mode (current consumption approximately 1 mA) to active mode (current consumption approximately 100 mA): it is permissible to use a regulator that switches from the PWM mode to the burst or PFM mode at an appropriate current threshold (e.g. 60 mA)

Figure 6 and the components listed in Table 4 show an example of a high reliability power supply circuit, where the **VCC** module supply is provided by a step-down switching regulator capable to deliver 2.5 A current pulses, with low output ripple, with 1 MHz fixed switching frequency in PWM mode operation. The use of a switching regulator is suggested when the difference from the available supply rail and the **VCC** value is high: switching regulators provide good efficiency transforming a 12 V supply to the 3.8 V typical value of the **VCC** supply. The following power supply circuit example is implemented on the LEON Evaluation Board.

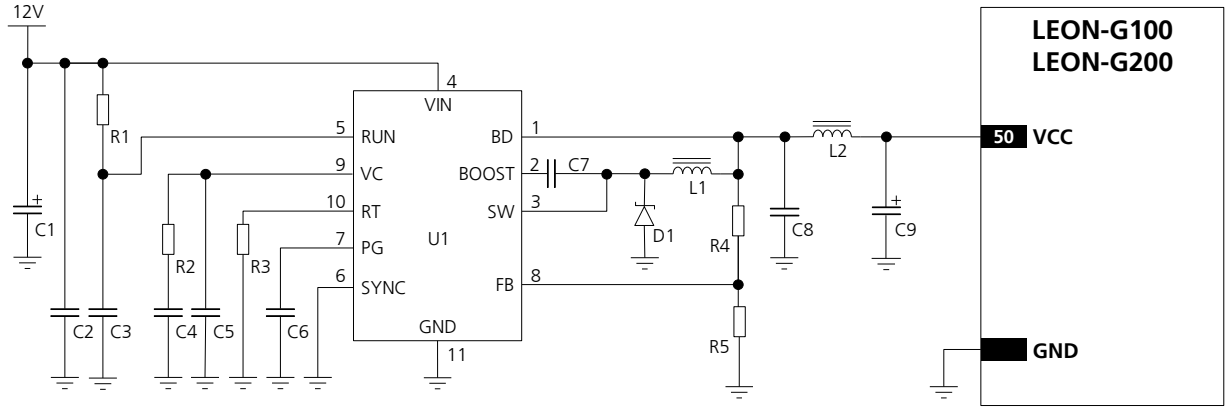

Figure 6: Suggested schematic design for the VCC voltage supply application circuit using a step-down regulator

Reference	Description	Part Number - Manufacturer
C1	47 µF Capacitor Aluminum 0810 50 V	MAL215371479E3 - Vishay
C2	10 µF Capacitor Ceramic X7R 5750 15% 50 V	C5750X7R1H106MB - TDK
C3	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C4	680 pF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71H681KA01 - Murata
C5	22 pF Capacitor Ceramic COG 0402 5% 25 V	GRM1555C1H220JZ01 - Murata
C6	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C7	470 nF Capacitor Ceramic X7R 0603 10% 25 V	GRM188R71E474KA12 - Murata
C8	22 µF Capacitor Ceramic X5R 1210 10% 25 V	GRM32ER61E226KE15 - Murata
C9	330 µF Capacitor Tantalum D_SIZE 6.3 V 45 mΩ	T520D337M006ATE045 - KEMET
D1	Schottky Diode 40 V 3 A	MBRA340T3G - ON Semiconductor
L1	10 µH Inductor 744066100 30% 3.6 A	744066100 - Wurth Electronics
L2	1 µH Inductor 7445601 20% 8.6 A	7445601 - Wurth Electronics
R1	470 kΩ Resistor 0402 5% 0.1 W	2322-705-87474-L - Yageo
R2	15 kΩ Resistor 0402 5% 0.1 W	2322-705-87153-L - Yageo
R3	33 kΩ Resistor 0402 5% 0.1 W	2322-705-87333-L - Yageo
R4	390 kΩ Resistor 0402 1% 0.063 W	RC0402FR-07390KL - Yageo
R5	100 kΩ Resistor 0402 5% 0.1 W	2322-705-70104-L - Yageo
U1	Step Down Regulator MSOP10 3.5 A 2.4 MHz	LT3972IMSE#PBF - Linear Technology

Table 4: Suggested components for VCC voltage supply application circuit using a high reliability step-down regulator

Figure 7 and the components listed in Table 5 show an example of a low cost power supply circuit, where the **VCC** module supply is provided by a step-down switching regulator capable of delivering 2.5 A current pulses, transforming a 12 V supply input.

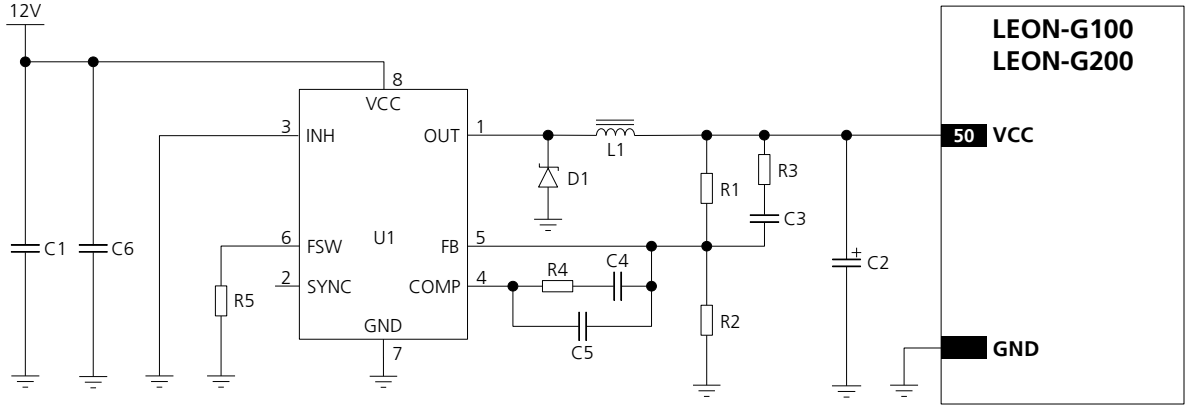

Figure 7: Suggested schematic design for the VCC voltage supply application circuit using a low cost step-down regulator

Reference	Description	Part Number - Manufacturer
C1	22 µF Capacitor Ceramic X5R 1210 10% 25 V	GRM32ER61E226KE15 – Murata
C2	100 µF Capacitor Tantalum B_SIZE 20% 6.3V 15mΩ	T520B107M006ATE015 – Kemet
C3	5.6 nF Capacitor Ceramic X7R 0402 10% 50 V	GRM155R71H562KA88 – Murata
C4	6.8 nF Capacitor Ceramic X7R 0402 10% 50 V	GRM155R71H682KA88 – Murata
C5	56 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H560JA01 – Murata
C6	220 nF Capacitor Ceramic X7R 0603 10% 25 V	GRM188R71E224KA88 – Murata
D1	Schottky Diode 25V 2 A	STPS2L25 – STMicroelectronics
L1	5.2 µH Inductor 30% 5.28A 22 mΩ	MSS1038-522NL – Coilcraft
R1	4.7 kΩ Resistor 0402 1% 0.063 W	RC0402FR-074K7L – Yageo
R2	910 Ω Resistor 0402 1% 0.063 W	RC0402FR-07910RL – Yageo
R3	82 Ω Resistor 0402 5% 0.063 W	RC0402JR-0782RL – Yageo
R4	8.2 kΩ Resistor 0402 5% 0.063 W	RC0402JR-078K2L – Yageo
R5	39 kΩ Resistor 0402 5% 0.063 W	RC0402JR-0739KL – Yageo
U1	Step Down Regulator 8-VFQFPN 3 A 1 MHz	L5987TR – ST Microelectronics

Table 5: Suggested components for VCC voltage supply application circuit using a low cost step-down regulator

Low Drop-Out (LDO) linear regulator

The characteristics of the LDO linear regulator connected to **VCC** pin should meet the following requirements:

- **Power capabilities**: the LDO linear regulator with its output circuit has to be capable to provide a proper voltage value to **VCC** pin and has to be capable to deliver 2.5 A current pulses with 1/8 duty cycle to **VCC** pin
- **Power dissipation**: the power handling capability of the LDO linear regulator has to be checked to limit its junction temperature to the maximum rated operating range (i.e. check the voltage drop from the max input voltage to the min output voltage to evaluate the power dissipation of the regulator)

Figure 8 and the components listed in Table 6 show an example of a power supply circuit, where the **VCC** module supply is provided by an LDO linear regulator capable to deliver 2.5 A current pulses, with proper power handling capability. The use of a linear regulator is suggested when the difference from the available supply rail and the VCC value is low: linear regulators provide good efficiency transforming a 5 V supply to the 3.8 V typical value of the VCC supply.

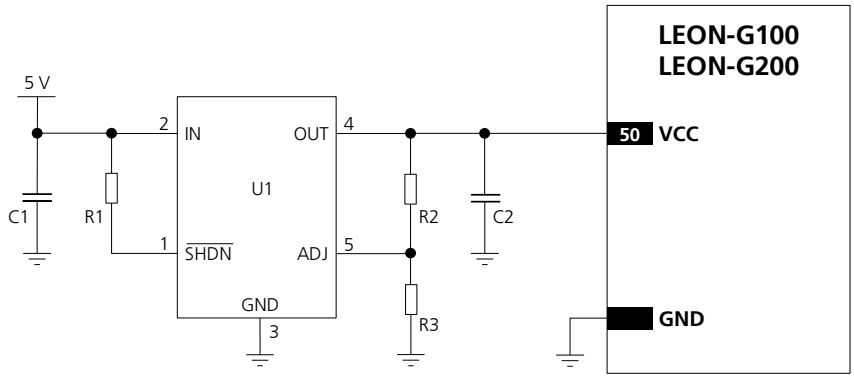

Figure 8: Suggested schematic design for the VCC voltage supply application circuit using an LDO linear regulator

Reference	Description	Part Number - Manufacturer
C1	10 µF Capacitor Ceramic X5R 0603 20% 6.3 V	GRM188R60J106ME47 - Murata
C2	10 µF Capacitor Ceramic X5R 0603 20% 6.3 V	GRM188R60J106ME47 - Murata
R1	47 kΩ Resistor 0402 5% 0.1 W	RC0402JR-0747KL - Yageo Phycomp
R2	4.7 kΩ Resistor 0402 5% 0.1 W	RC0402JR-074K7L - Yageo Phycomp
R3	2.2 kΩ Resistor 0402 5% 0.1 W	RC0402JR-072K2L - Yageo Phycomp
U1	LDO Linear Regulator ADJ 3.0 A	LT1764AEQ#PBF - Linear Technology

Table 6: Suggested components for VCC voltage supply application circuit using an LDO linear regulator

Rechargeable Li-Ion battery

The characteristics of the rechargeable Li-Ion battery connected to **VCC** pin should meet the following requirements:

- **Maximum pulse and DC discharge current**: the rechargeable Li-Ion battery with its output circuit has to be capable to deliver 2.5 A current pulses with 1/8 duty cycle to **VCC** pin and has to be capable to deliver a DC current greater than the module maximum average current consumption to **VCC** pin. Note that the maximum pulse discharge current and the maximum DC discharge current are not always reported in batteries data sheet, but the maximum DC discharge current is typically almost equal to the battery capacity in Ampere-hours divided by 1 hour
- **DC series resistance**: the rechargeable Li-Ion battery with its output circuit has to be capable to avoid a VCC voltage drop greater than 400 mV during transmit bursts
- **Maximum charging voltage** (overcharge detection voltage): if the charging process is managed by the GSM module, the overcharge detection voltage of the used battery pack, which enables battery protection, must be greater or equal than 4.3 V, to be charged by the GSM module
- **Charging operating temperature range**: if the charging process is managed by the GSM module, the charging operating temperature range of the used battery pack must include the 0°C-40°C range, to be charged by the GSM module
- **Maximum DC charging current**: the rechargeable Li-Ion battery has to be capable to be charged by the charging current provided by the selected external charger. Note that the maximum DC charging current is not always reported in batteries data sheet, but the maximum DC charging current is typically almost equal to the battery capacity in Ampere-hours divided by 1 hour

Primary (disposable) battery

The characteristics of the primary (non-rechargeable) battery connected to **VCC** pin should meet the following requirements:

- **Maximum pulse and DC discharge current**: the no-rechargeable battery with its output circuit has to be capable to deliver 2.5 A current pulses with 1/8 duty cycle to **VCC** pin and has to be capable to deliver a DC current greater than the module maximum average current consumption to **VCC** pin. Note that the maximum pulse and the maximum DC discharge current is not always reported in batteries data sheet, but the maximum DC discharge current is typically almost equal to the battery capacity in Ampere-hours divided by 1 hour
- **DC series resistance**: the no-rechargeable battery with its output circuit has to be capable to avoid a VCC voltage drop greater than 400 mV during transmit bursts

Additional hints for the VCC supply application circuits

To reduce voltage drops, use a low impedance power source. The resistance of the power supply lines (connected to **VCC** and **GND** pins of the module) on the application board and battery pack should also be considered and minimized: cabling and routing must be as short as possible in order to minimize power losses.

To avoid undershoot and overshoot on voltage drops at the start and at the end of a transmit burst during a GSM call (when current consumption on the VCC supply can rise up to 2.5 A in the worst case), place a 330 µF low ESR capacitor (e.g. KEMET T520D337M006ATE045) located near **VCC** pin of LEON-G100/G200.

To reduce voltage ripple and noise, place near **VCC** pin of the LEON-G100/G200 the following components:

- 100 nF capacitor (e.g Murata GRM155R61A104K) to filter digital logic noises from clocks and data sources
- 10 nF capacitor (e.g. Murata GRM155R71C103K) to filter digital logic noises from clocks and data sources
- 10 pF capacitor (e.g. Murata GRM1555C1E100J) to filter transmission EMI in the DCS/PCS bands
- 39 pF capacitor (e.g. Murata GRM1555C1E390J) to filter transmission EMI in the GSM/EGSM bands

☞ Note that the Figure 9 shows the complete configuration but the mounting of the each single component depends on application design.

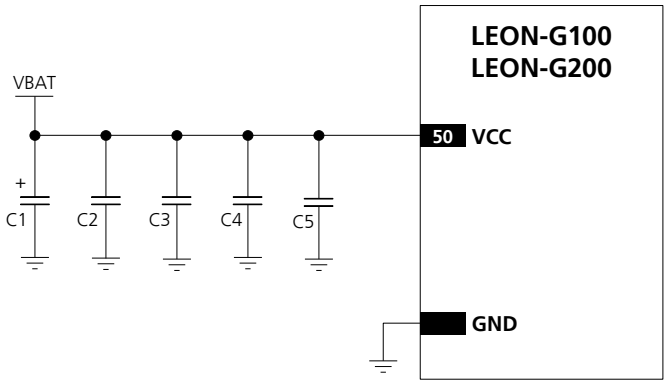

Figure 9: Suggested schematics design to reduce voltage ripple, noise and avoid undershoot and overshoot on voltage drops

Reference	Description	Part Number - Manufacturer
C1	330 µF Capacitor Tantalum D_SIZE 6.3 V 45 mΩ	T520D337M006ATE045 - KEMET
C2	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
C3	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C4	39 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1E390JA01 - Murata
C5	10 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1E100JA01 - Murata

Table 7: Suggested components to reduce voltage ripple and noise and avoid undershoot and overshoot on voltage drops

1.5.3 Current consumption profiles

During operation, the current consumed by LEON-G100/G200 through **VCC** pin can vary by several orders of magnitude. This is applied to ranges from the high peak of current consumption during the GSM transmitting bursts at maximum power level in connected mode, to the low current consumption in idle mode when power saving configuration is enabled.

1.5.3.1 Current consumption profiles – Connected mode

When a GSM call is established, the **VCC** consumption is determined by the current consumption profile typical of the GSM transmitting and receiving bursts.

The current consumption peak during a transmission slot is strictly dependent on the transmitted power, which is regulated by the network. If the module transmits in GSM talk mode in the GSM 850 or in the EGSM 900 band at the maximum power control level (32.2 dBm typical transmitted power in the transmit slot/burst), the current consumption can reach up to 2500 mA (with highly unmatched antenna) for 576.9 µs (width of the transmit slot/burst) with a periodicity of 4.615 ms (width of 1 frame = 8 slots/bursts), so with a 1/8 duty cycle, according to GSM TDMA.

During a GSM call, current consumption is in the order of 100-200 mA in receiving or in monitor bursts and is about 30-50 mA in the inactive unused bursts (low current period). The more relevant contribution to determine the average current consumption is set by the transmitted power in the transmit slot.

An example of current consumption profile of the data module in GSM talk mode is shown in Figure 10.

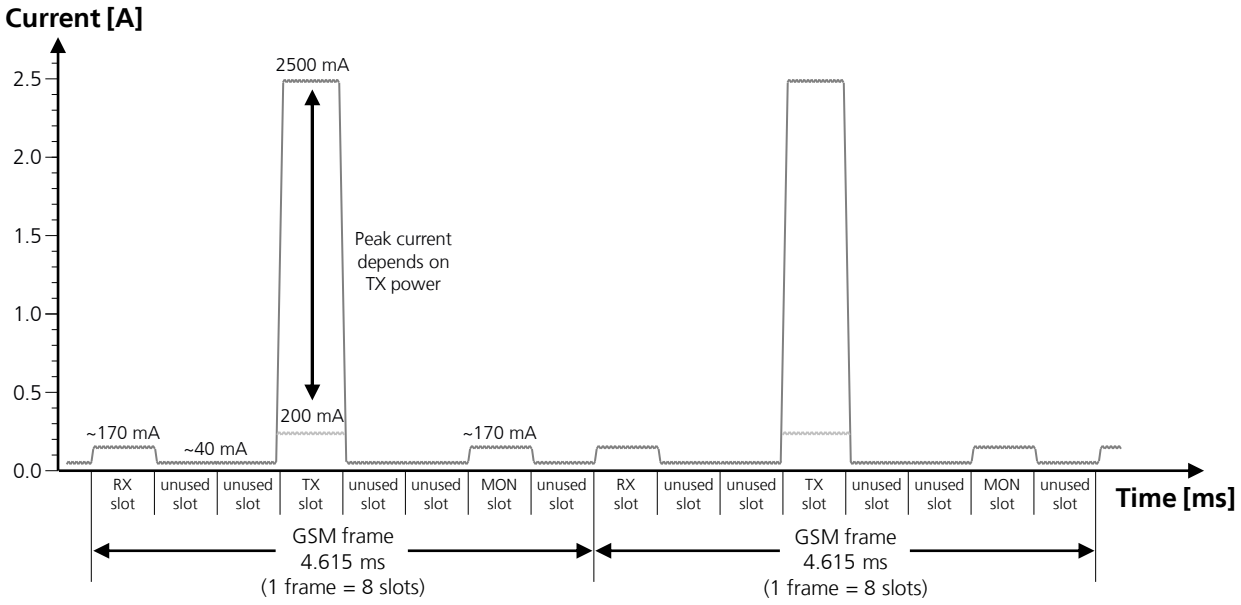

Figure 10: Description of the VCC current consumption profile versus time during a GSM call (1 TX slot)

When a GPRS connection is established there is a different VCC current consumption profile also determined by the transmitting and receiving bursts. In contrast to a GSM call, during a GPRS connection more than one slot can be used to transmit and/or more than one slot can be used to receive. The transmitted power depends on network conditions and sets the peak of current consumption, but following the GPRS specifications the maximum transmitted power can be reduced if more than one slot is used to transmit, so the maximum peak of current consumption is not as high as can be the case in a GSM call.

If the module transmits in GPRS class 10 connected mode in the GSM 850 or in the EGSM 900 band at the maximum power control level (30.5 dBm typical transmitted power in the transmit slot/burst), the current consumption can reach up to 1800 mA (with highly unmatched antenna) for 1.154 ms (width of the 2 transmit slots/bursts) with a periodicity of 4.615 ms (width of 1 frame = 8 slots/bursts), so with a 1/4 duty cycle, according to GSM TDMA.

In the following figure is reported the current consumption profiles with 2 slots used to transmit.

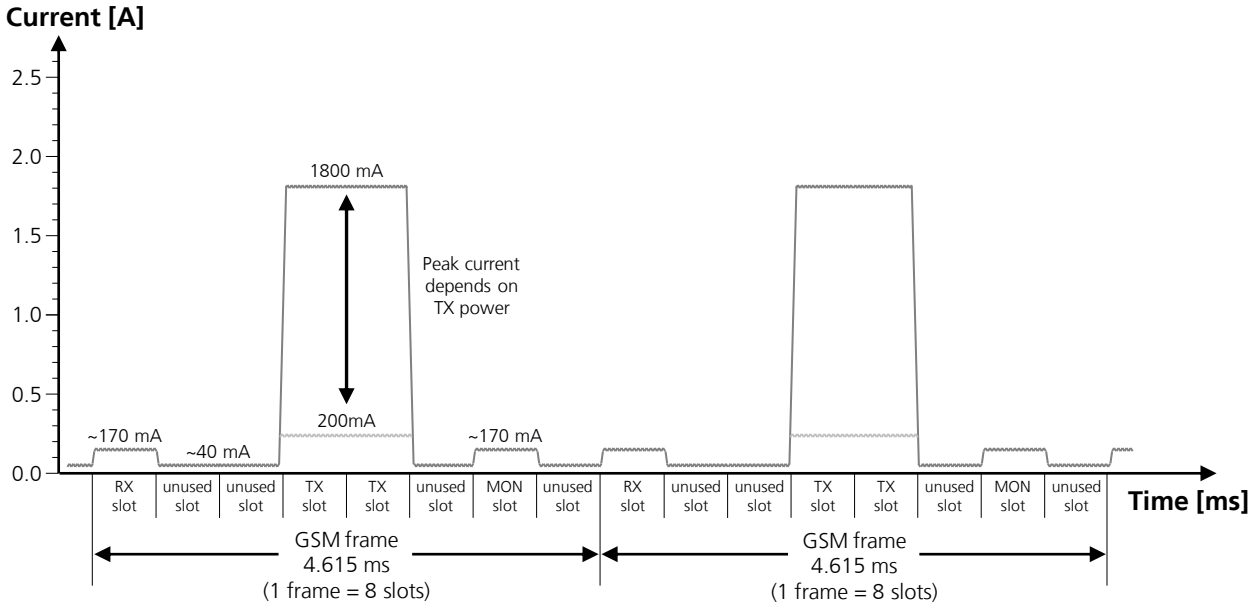

Figure 11: Description of the VCC current consumption profile versus time during a GPRS connection (2 TX slots)

1.5.3.2 Current consumption profiles – Cyclic idle/active mode (power saving enabled)

The power saving configuration is by default disabled, but it can be enabled using the appropriate AT command (refer to u-blox 2G GSM/GPRS AT Commands Manual [2], AT+UPSV command). When the power saving is enabled, the module automatically enters idle-mode whenever possible.

When power saving is enabled, the module is registered or attached to a network and a voice or data call is not enabled, the module automatically enters idle-mode whenever possible, but it must periodically monitor the paging channel of the current base station (paging block reception), in accordance to GSM system requirements. When the module monitors the paging channel, it wakes up to active mode, to enable the reception of paging block. In between, the module switches to idle-mode. This is known as GSM discontinuous reception (DRX).

The module processor core is activated during the paging block reception, and automatically switches its reference clock frequency from the 32 kHz used in idle-mode to the 26 MHz used in active-mode.

The time period between two paging block receptions is defined by the network. It can vary from 470.76 ms (width of 2 GSM multiframes = 2 x 51 GSM frames = 2 x 51 x 4.615 ms) up to 2118.42 ms (width of 9 GSM multiframes = 9 x 51 frames = 9 x 51 x 4.615 ms): this is the paging period parameter, fixed by the base station through broadcast channel sent to all users on the same serving cell.

An example of the current consumption profile of the data module when power saving is enabled is shown in Figure 12: the module is registered with the network, automatically goes into idle mode and periodically wakes up to active mode to monitor the paging channel for paging block reception (cyclic idle/active mode).

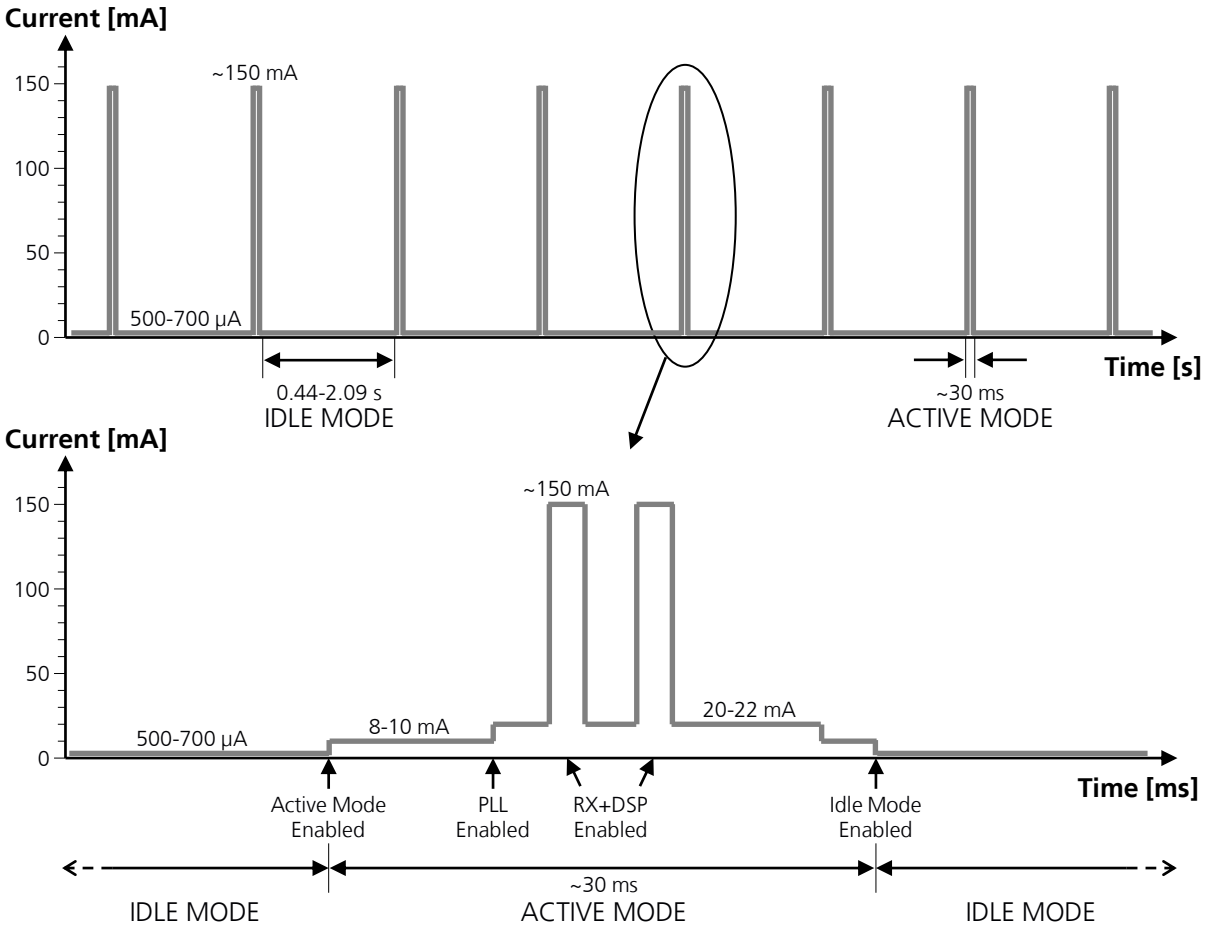

Figure 12: Description of the VCC current consumption profile versus time when power saving is enabled: the module is in idle mode and periodically wakes up to active mode to monitor the paging channel for paging block reception

1.5.3.3 Current consumption profiles – Fixed active mode (power saving disabled)

Power saving configuration is by default disabled, or it can be disabled using the appropriate AT command (refer to u-blox 2G GSM/GPRS AT Commands Manual [2], AT+UPSV command). When power saving is disabled, the module doesn't automatically enter idle-mode whenever possible: the module remains in active mode.

The module processor core is activated during active-mode, and the 26 MHz reference clock frequency is used.

An example of the current consumption profile of the data module when power saving is disabled is shown in Figure 13: the module is registered with the network, active-mode is maintained, and the receiver and the DSP are periodically activated to monitor the paging channel for paging block reception.

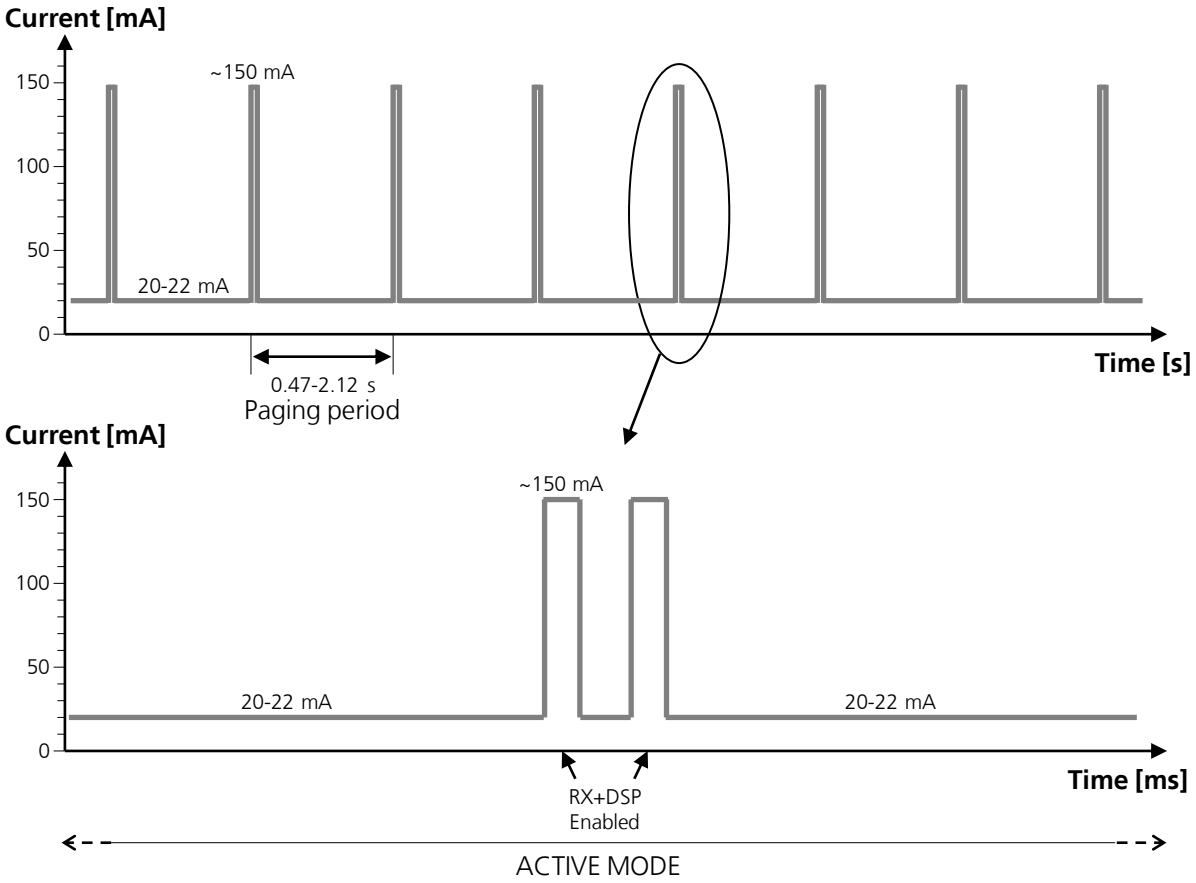

Figure 13: Description of the VCC current consumption profile versus time when power saving is disabled: active-mode is always held, and the receiver and the DSP are periodically activated to monitor the paging channel for paging block reception

1.5.4 Battery charger (LEON-G200 only)

For battery charging functionalities the module is provided with integrated circuitry and software. Two pins are available to connect the positive pole of the external DC supply used as charger.

Name	Description	Remarks
V_CHARGE	Charger Voltage Supply Input	V_CHARGE and CHARGE_SENSE pins must be externally connected together.
CHARGE_SENSE	Charger Voltage Measurement Input	V_CHARGE and CHARGE_SENSE pins must be externally connected together.

Table 8: Battery charger pins

☞ **V_CHARGE** and **CHARGE_SENSE** pins ESD rating is 1 kV (contact discharge). A higher protection level could be required if the lines are externally accessible on the application board. A higher protection level can be achieved mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) on the lines connected to these pins if they are externally accessible on the application board.

The **V_CHARGE** pin is the charger supply input: it sinks the charge current that is typically in the order of several hundred of mA. The **CHARGE_SENSE** pin is connected to an internal ADC converter to measure the charging voltage: it senses the charger voltage and sinks a few µA.

☞ **V_CHARGE** and **CHARGE_SENSE** pins must be externally connected together as shown in Figure 14.

☞ There may not be any capacitor on the charge path: a straight connection must be provided between the output of the external supply used as charging source and **V_CHARGE** and **CHARGE_SENSE** pins of the module.

☞ If the battery charging process is not managed by the GSM module, **V_CHARGE** and **CHARGE_SENSE** pins can be left floating on the application board.

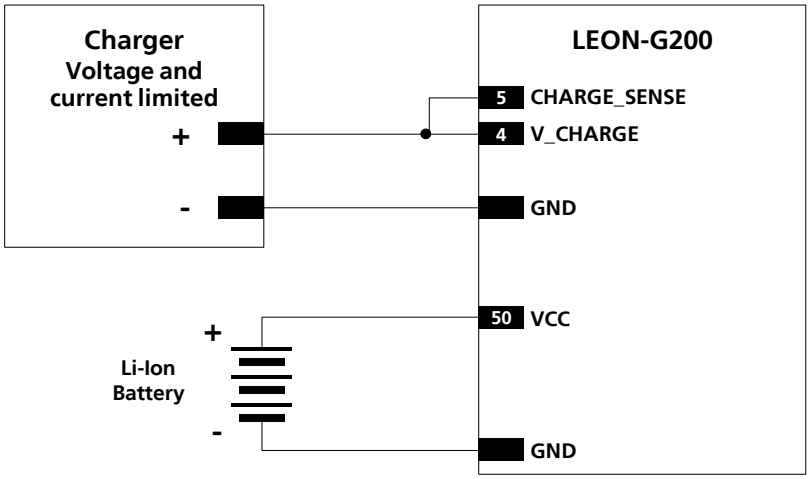

Figure 14: Connection of an external DC supply used as charger and a Li-Ion battery to the LEON-G200 module

⚠ **To prevent damage to the module and the battery, use only chargers that comply with the characteristics given in section 1.5.4.2.**

1.5.4.1 Charging process description

A valid charger is recognized if the voltage provided to **V_CHARGE** and **CHARGE_SENSE** pins are within the operating range limits (5.6 V minimum, 15 V maximum). If the module is switched off, the charger circuitry generates the power on in charging mode after charger detection.

The algorithm that controls battery charging, implements a classic Li-Ion battery charging process, divided into 4 phases:

1. Pre-Charge, at low current, for deeply discharged batteries (**VCC** voltage within 0 V and 3.1 V typical)
2. Fast Charge, at the maximum current provided by the external DC supply used as charger that must be current limited, for discharged batteries (**VCC** voltage within 3.1 V typical and 4.2 V typical)
3. Top Charge, to complete the over-charging of the batteries, after the maximum voltage is reached (**VCC** voltage equal to 4.2 V typical)
4. Trickle Charge, to maintain the battery at higher level of charge, if the external DC supply used as charger remains connected

If the batteries are deeply discharged (**VCC** voltage within 0 V and 3.1 V typical with 7% tolerance due to change in temperature and life time), and the device is in not-powered mode, the charger circuit starts pre-charging when a valid voltage is provided to **V_CHARGE** and **CHARGE_SENSE** pins of the module. In the pre-charging phase, the charge transistor switch mounted inside the module is pulsed with a 100 Hz clock and

an on-time of 12.5% of a period. This means the average charge current is reduced to avoid overheating of charger parts and to gently charge the deeply discharged batteries: the average pre-charge current is ~1/8 (i.e. 12.5%) of the current provided by the external charger, so it is ~1/8 of the external charger current limit. Pre-charging phase is hardware controlled and continues as long as the **VCC** voltage reaches the 3.1 V typical limit, so the module is able to start the following fast charging phase.

During fast charging phase (following the pre-charging phase) the charge transistor switch mounted inside the module is pulsed with a 100 Hz and an on-time of 99% of a period: the average charge current is almost equal (i.e. 99%) to the current provided by the external charger, so it is almost equal to the external charger current limit. The remaining off time (i.e. 1% of a period) is used to check if the external charger is still connected since detection is critical when charging switch is closed.

The integrated charging circuit doesn't have any voltage or current limitation, therefore the charger must be chosen very carefully: during the fast charging phase, the battery is charged with the maximum DC current provided by the external DC supply used as charger, which must be current limited as described in the charger specification section.

When the battery voltage reaches the nominal maximum voltage (4.2 V typical with 2% tolerance due to change in temperature and life time), charging enters the constant voltage phase (top charge algorithm): in this phase the average charging current decreases until the battery is completely charged.

After the constant voltage phase, the battery is maintained at a higher level of charge with the trickle charge algorithm until an external charger is connected to the module.

The charging process is enabled only within the temperature range from 0°C to 40°C, with a 5°C hysteresis to prevent rapid switching on and off as the temperature drifts around the set point: charging is disabled when the temperature falls below 0°C and then enabled when it rises above 5°C; charging is disabled when the measured temperature rises above 40°C and then enabled when falls below 35°C.

Battery over-voltage detection is implemented to switch-off charging if the battery is removed during charging. The **VCC** over-voltage threshold level is set to the nominal value of 4.47 V (evaluated with 2% of tolerance due to change in temperature and life time).

The charging process is disabled when an external charger is removed from **V_CHARGE** and **CHARGE_SENSE** pins.

1.5.4.2 External charger specification

It is suggested to use a charger with the following electrical characteristics:

- 6 V DC voltage
- 500 mA current limit (if it is less than the maximum DC charging current specified by the used battery)

To avoid damage to the module, the external supply used as charging source must be voltage and current limited, with a voltage limit ≦ 15 V and a current limit ≦ 1.0 A.

DC supplies with fold-back current protection cannot be used as charger for the module.

The V-I output characteristics of the external supply used as charger must be within the valid area delineated by:

- the maximum acceptable charging voltage (equal to 15 V in any case)
- the minimum open circuit voltage valid for charger detection (equal to 5.6 V in any case)
- the maximum acceptable charging current (equal to 1.0 A or to the maximum DC charging current specified by the used battery if it is less than 1.0 A)
- the minimum charging current (specified by the application, e.g. 400 mA)

Maximum voltage

The voltage limit of the external charger must be ≦ 15 V. Since the module is not provided with an internal overvoltage protection circuit on **V_CHARGE** and **CHARGE_SENSE** pins, the charging voltage must be lower or

equal to the maximum acceptable charging voltage value of 15 V at any time: voltage spikes that may occur during connection or disconnection of the charger must be limited within this value, so the external supply used as charging source must be voltage limited with a voltage limit ≦ 15 V.

Minimum voltage

The charger must be able to provide a minimum open circuit output voltage ≧ 5.6 V for the valid charger detection.

Maximum current

The current limit of the external charger must be ≦ 1.0 A (that is the module absolute maximum rating as charging current) and must be lower than the maximum DC charging current specified by the used battery. Since the module is not provided with an internal over-current protection circuit on **V_CHARGE** and **CHARGE_SENSE** pins, the charging current must be lower or equal to the maximum acceptable charging current value at any time: current spikes that may occur during charger connection or disconnection must be limited within this value, so the external supply used as charging source must be current limited with a proper current limit.

Minimum current

A minimum acceptable value for the charging current is not specified, but the charging current value should be large enough to perform the whole battery charging process within the time interval defined by the application and the charging current value should be greater than the highest possible average current consumption of the system that is supplied by the battery (i.e. the module plus any additional device on the application board) to let the increase of the battery level while the system reaches its highest current consumption. For example, if the battery supplies only the module and the charging current value is equal to 400 mA, the battery level can be increased also when the module reaches its highest current consumption (during a GPRS connection). If some other devices are supplied by the battery beside the module, when the battery is deeply discharged (VCC below 3.1 V typical), the module is switched off and the pre-charging current (~1/8 of the external charger current limit) is enabled: this current should be greater than the highest possible average current consumption of the system to let the increase of the battery level while the system reaches its highest current consumption.

For example, Figure 15 shows the valid area for the charger V-I output characteristics using a battery with a maximum DC charging current equal to 600 mA: the maximum acceptable charging current is defined by the battery requirement (600 mA).

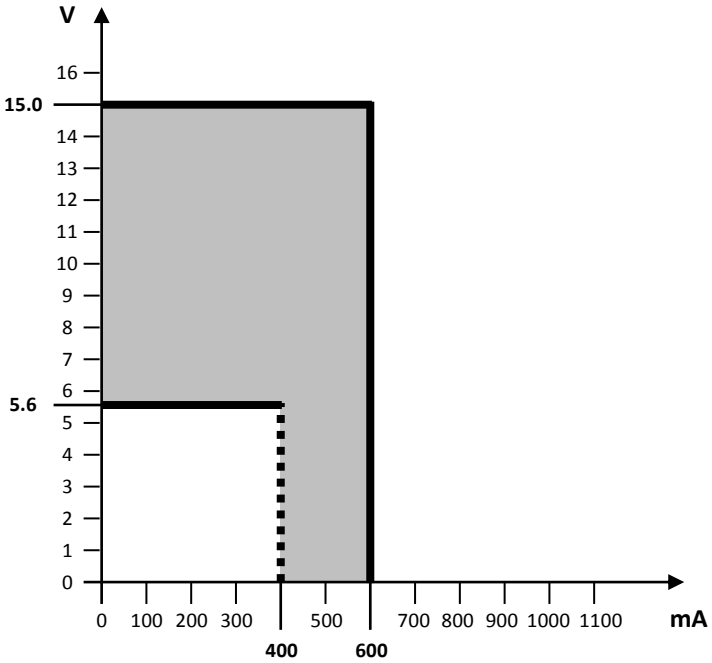

Figure 15: Valid area for the charger V-I output characteristics using a battery with a max DC charging current equal to 600 mA

For example, Figure 16 shows the valid area for the charger V-I output characteristics using a battery with a maximum DC charging current greater than 1000 mA: the maximum acceptable charging current is defined by the module requirement (1000 mA).

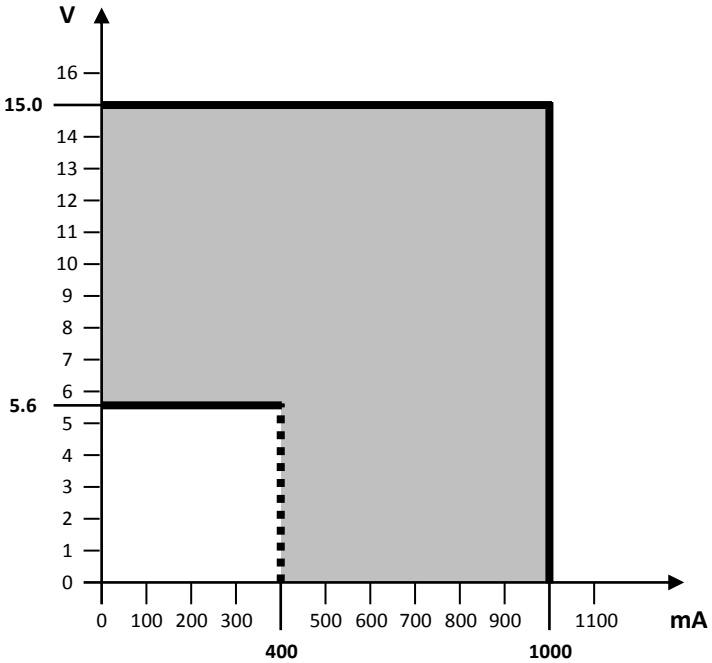

Figure 16: Valid area for the charger V-I output characteristics using a battery with a max DC charging current greater than 1 A

1.5.5 RTC Supply (V_BCKP)

V_BCKP connects the Real Time Clock (RTC) supply, generated internally by a linear regulator integrated in the module chipset. The output of this linear regulator is enabled when the main voltage supply providing the module through VCC is within the valid operating range, or if the module is switched-off.

Name	Description	Remarks
V_BCKP	Real Time Clock supply	V_BCKP = 2.0 V (typical) generated by the module to supply Real Time Clock when VCC supply voltage is within valid operating range.

Table 9: Real Time Clock supply pin

☞ **V_BCKP** pin ESD rating is 1 kV (contact discharge). A higher protection level could be required if the line is externally accessible on the application board. A higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) on the line connected to this pin if it is externally accessible on the application board.

The RTC provides the time reference (date and time) of the module, also in power-off mode, since the RTC runs when the **V_BCKP** voltage is within its valid range (specified in LEON-G100/G200 Data Sheet [1]). The RTC block is able to provide programmable alarm functions by means of the internal 32.768 kHz clock.

The RTC block has very low, but highly temperature dependent power consumption. For example at 25°C and a **V_BCKP** voltage of 2.0 V the power consumption is approximately 2 µA, whereas at 85°C and an equal voltage it increases to 5 µA.

The RTC can be supplied from an external back-up battery through **V_BCKP**, when the main voltage supply is not provided to the module through **VCC**. This enables the time reference (date and time) to run even when the main supply is not provided to the module. The module cannot switch on if a valid voltage is not present on **VCC**, even when RTC is supplied through **V_BCKP** (meaning that **VCC** is mandatory to switch-on the module).

If **V_BCKP** is left unconnected and the main voltage supply of the module is removed from **VCC**, the RTC is supplied from the 1 µF buffer capacitor mounted inside the module. However, this capacitor is not able to provide a long buffering time: within 0.5 seconds the voltage on **V_BCKP** will fall below the valid range (1 V min).

☞ If RTC is not required when **VCC** supply is removed, **V_BCKP** can be left floating on the application board.

If RTC has to run for a time interval of T [seconds] at 25°C and **VCC** supply is removed, place a capacitor of nominal capacitance of C [µF] at the **V_BCKP** pin. Choose the capacitor using the following formula:

C [µF] = (Current_Consumption [µA] x T [seconds]) / Voltage_Drop [V] = 2 x T [seconds]

The current consumption of the RTC is around 2 µA at 25°C, and the voltage drop is equal to 1 V (from the **V_BCKP** typical value of 2.0 V to the valid range minimum limit of 1.0 V).

For example, a 100 µF capacitor (such as the Murata GRM43SR60J107M) can be placed at **V_BCKP** to provide a long buffering time. This capacitor will hold **V_BCKP** voltage within its valid range for around 50 seconds at 25°C, after the **VCC** supply is removed. If a very long buffering time is required, a 70 mF super-capacitor (e.g. Seiko Instruments XH414H-IV01E) can be placed at **V_BCKP**, with a 4.7 k series resistor to hold the **V_BCKP** voltage within its valid range for around 10 hours at 25°C, after the **VCC** supply is removed. The purpose of the series resistor is to limit the capacitor charging current due to the big capacitor specifications, and also to let a fast rise time of the voltage value at the **V_BCKP** pin after **VCC** supply has been provided. These capacitors will allow the time reference to run during a disconnection of the **VCC** supply.

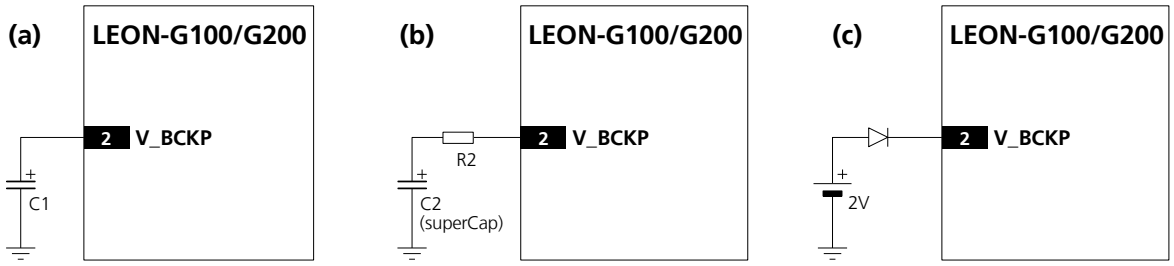

Figure 17: Real time clock supply (V_BCKP) application circuits: (a) using a 100 µF capacitor to let the RTC run for 50 seconds at 25°C; (b) using a 70 mF capacitor to let the RTC run for ~10 hours at 25°C when the VCC supply is removed; (c) using a not rechargeable battery

Reference	Description	Part Number - Manufacturer
C1	100 µF Tantalum Capacitor	GRM43SR60J107M - Murata
R2	4.7 kΩ Resistor 0402 5% 0.1 W	RC0402JR-074K7L - Yageo Phycomp
C2	70 mF Capacitor	XH414H-IV01E - Seiko Instruments

Table 10: Example of components for V_BCKP buffering

If longer buffering time is required to allow the time reference to run during a disconnection of the **VCC** supply, a rechargeable battery, which has to be able to provide a 2.0 V nominal voltage and must not exceed the maximum operating voltage value of 2.25 V, can be connected to the **V_BCKP** pin with a proper series resistor. Otherwise a not rechargeable battery, which has to be able to provide a 2.0 V nominal voltage and must not exceed the maximum operating voltage value of 2.25 V, can be connected to the **V_BCKP** pin with a proper series resistor and a proper series diode. The purpose of the series resistor is to limit the battery charging current due to the battery specifications, and also to let a fast rise time of the voltage value at the **V_BCKP** pin after **VCC** supply has been provided. The purpose of the series diode is to avoid a current flow from the **V_BCKP** pin of the module to the not rechargeable battery.

1.6 System functions

1.6.1 Module power on

The power-on sequence of the module is initiated in one of 4 ways:

- Rising edge on the **VCC** pin to a valid voltage as module supply
- Low level on the **PWR_ON** signal
- RTC alarm
- Charger detection on the **V_CHARGE** and **CHARGE_SENSE** pins (LEON-G200 only)

Name	Description	Remarks
PWR_ON	Power-on input	PWR_ON pin has high input impedance. Do not keep floating in noisy environment: external pull-up required.

Table 11: Power-on pin

PWR_ON pin ESD rating is 1 kV (contact discharge). A higher protection level could be required if the line is externally accessible on the application board. A higher protection level can be achieved mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) on the line connected to this pin if it is externally accessible on the application board.

1.6.1.1 Rising edge on VCC

When a supply is connected to **VCC** pin, the module supply supervision circuit controls the subsequent activation of the power up state machines: the module is switched-on when the voltage rises up to the **VCC** normal operating range minimum limit (3.35 V) starting from a voltage value lower than 2.25 V.

1.6.1.2 Low level on the PWR_ON

Power-on sequence of the module starts when a low level is forced on the **PWR_ON** signal for at least 5 ms.

The electrical characteristics of the **PWR_ON** input pin are different from the other digital I/O interfaces: the high and the low logic levels have different operating ranges and the pin is tolerant against voltages up to the battery voltage. The detailed electrical characteristics are described in LEON-G100/G200 Data Sheet [1].

☞ **PWR_ON** pin has high input impedance and is weakly pulled to the high level on the module. Avoid keep it floating in noisy environment. To hold the high logic level stable, the **PWR_ON** pin must be connected to a pull-up resistor (e.g. 100 kΩ) biased by a supply rail present on the application board, in range from 1.8 V to 4.5 V, which supply rail should be available when the module is in power-off mode.

If **PWR_ON** input is connected to a push button that shorts the **PWR_ON** pin to ground, the **V_BCKP** supply pin or the **VCC** supply pin of the module can be used to bias the pull-up resistor.

If **PWR_ON** input is connected to an external device (e.g. application processor), it is suggested to use an open drain output of the external device with an external pull-up. Connect the pull-up the **V_BCKP** supply pin or the **VCC** supply pin of the module, or to another supply rail present on the application board, in range from 1.8 V to 4.5 V, which supply rail should be available when the module is in power-off mode.

If **PWR_ON** pin is connected to a push-pull output pin of an application processor, the pull-up can be provided to pull high the **PWR_ON** level when the application processor is switched off. If the high-level voltage of the push-pull output pin of the application processor is greater than 2.0 V, the **V_BCKP** supply cannot be used to bias the pull-up resistor: the supply rail of the application processor or the **VCC** supply can be used. Using a push-pull output of the external device, take care to fix the proper level in all the possible scenarios to avoid an inappropriate switch-on of the module.

☞ The module can be switched-on by forcing a low level for at least 5 ms on the **PWR_ON** pin: the module is not switched-on by a falling edge provided on the **PWR_ON** pin. The suggested **PWR_ON** pull-up resistor value is 100 kΩ: lower resistance value will increase the module power-off consumption.

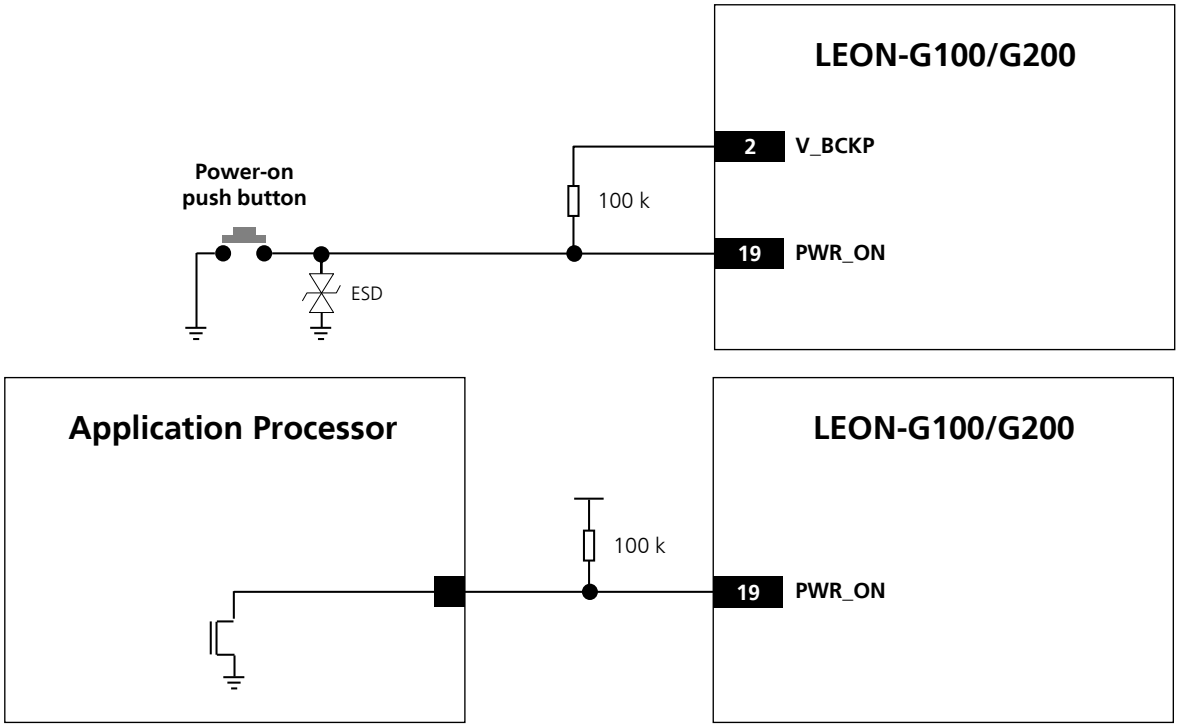

Figure 18: Power on (PWR_ON) application circuits using a push button or using an application processor

1.6.1.3 RTC alarm

The module can be switched-on by the RTC alarm if a valid voltage is applied to **VCC** pin, when Real Time Clock system reaches a pre-defined scheduled time. The RTC system will then initiate the boot sequence by indicating to the power management unit to turn on power. Also included in this setup is an interrupt signal from the RTC block to indicate to the baseband processor, that a RTC event has occurred.

1.6.1.4 Charger detection on V_CHARGE and CHARGE_SENSE pins (LEON-G200 only)

The module can be switched-on by a charger: when a voltage value within the valid range for charger detection is applied to the module **V_CHARGE** and **CHARGE_SENSE** pins (See LEON-G100/G200 Data Sheet [1]), the module is switched on in charge mode.

1.6.1.5 Additional considerations

The module is switched on when the voltage rises up to the **VCC** normal operating range: the first time that the module is used, it is switched on in this way. Then, the proper way to switch-off the module is by means of the AT+CPWROFF command. When the module is in power-off mode, i.e. the AT+CPWROFF command has been sent and a voltage value within the normal operating range limits is still provided to the **VCC** pin, the digital input-output pads of the baseband chipset (i.e. all the digital pins of the module) are locked in tri-state (i.e. floating). The power down tri-state function isolates the pins of the module from its environment, when no proper operation of the outputs can be guaranteed. To avoid an increase of the module current consumption in power down mode, any external signal of the digital interfaces connected to the module must be set low or tri-stated when the module is in not-powered mode or in the power-off mode.

The module can be switched on from power-off mode by forcing a proper start-up event (i.e. a low level on the **PWR_ON** pin, or an RTC alarm, or a charger detection). After the detection of a start-up event, all the digital pins of the module are held in tri-state until all the internal LDO voltage regulators are turned on in a defined power-on sequence. Then, as described in Figure 19, the baseband core continues to be held in reset state for a time interval: the module still pulls the **RESET_N** pin low and any signal from the module digital interfaces is held in reset state. The reset state of all the digital pins is reported in the pin description table of the LEON-G100/G200 Data Sheet [1]. When the module releases the **RESET_N** pin, the level at this pin will be pulled

high by the action of the internal pull-up and the configuration of the module interfaces will start: during this phase any digital pin is set in a proper sequence from reset state to the default operational configuration. The module is fully ready to operate when all the interfaces are configured.

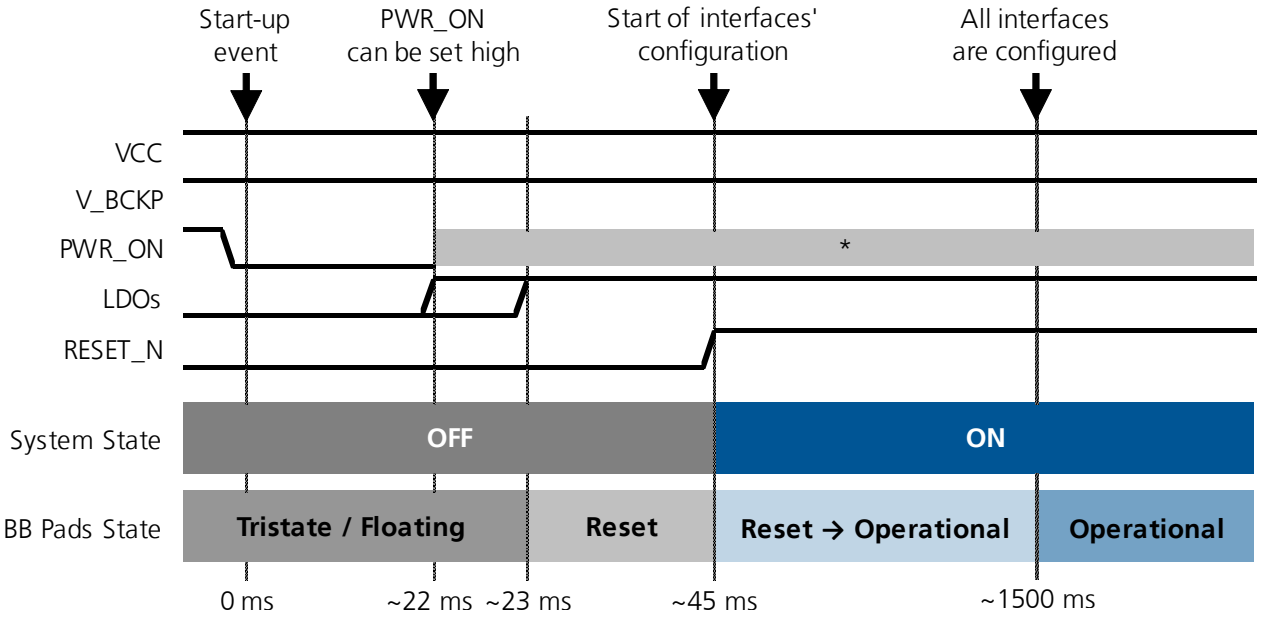

Figure 19: Power on sequence description (* - the PWR_ON signal state is not relevant during this phase)

1.6.2 Module power off

The correct way to switch off LEON-G100/G200 modules is by means of the AT command AT+CPWROFF (more details in u-blox 2G GSM/GPRS AT Commands Manual [2]): in this way the current parameter settings are saved in the module's non-volatile memory and a proper network detach is performed.

An under-voltage shutdown will be done if **VCC** falls below the extended operating range minimum limit (see LEON-G100/G200 Data Sheet [1]), but in this case the current parameter settings are not saved in the module's non-volatile memory and a proper network detach cannot be performed.

When the AT+CPWROFF command is sent, the module starts the switch-off routine replying OK on the AT interface: during this phase, the current parameter settings are saved in the module's non-volatile memory, a network detach is performed and all module interfaces are disabled (i.e. the digital pins are locked in tri-state by the module). Since the time to perform a network detach depends on the network settings, the duration of this phase can differ from the typical value reported in Figure 20. At the end of the switch-off routine, the module pulls the **RESET_N** pin low to indicate that it is in power-off mode: all the digital pins are locked in tri-state by the module and all the internal LDO voltage regulators except the RTC supply (**V_BCKP**) are turned off in a defined power-off sequence. The module remains in power-off mode as long as a switch-on event doesn't occur (i.e. a low level on the **PWR_ON** pin, or an RTC alarm, or a charger detection), and enters not-powered mode if the supply is removed from the **VCC** pin.

☞ To avoid an increase of module current consumption in power-down mode, any external signal connected to the module digital pins (UART interface, Digital audio interface, HS_DET, GPIOs) must be set low or tri-stated when the module is in the not-powered or power-off modes. If the external signals connected to the module digital pins cannot be set low or tri-stated, insert a switch (e.g. Texas Instruments SN74CB3Q16244, or Texas Instruments TS5A3159, or Texas Instruments TS5A63157) between the two-circuit connections. Set the switch to high impedance when the module is in power-down mode (to avoid an increase of the module power consumption).

The power-off sequence is described in Figure 20.

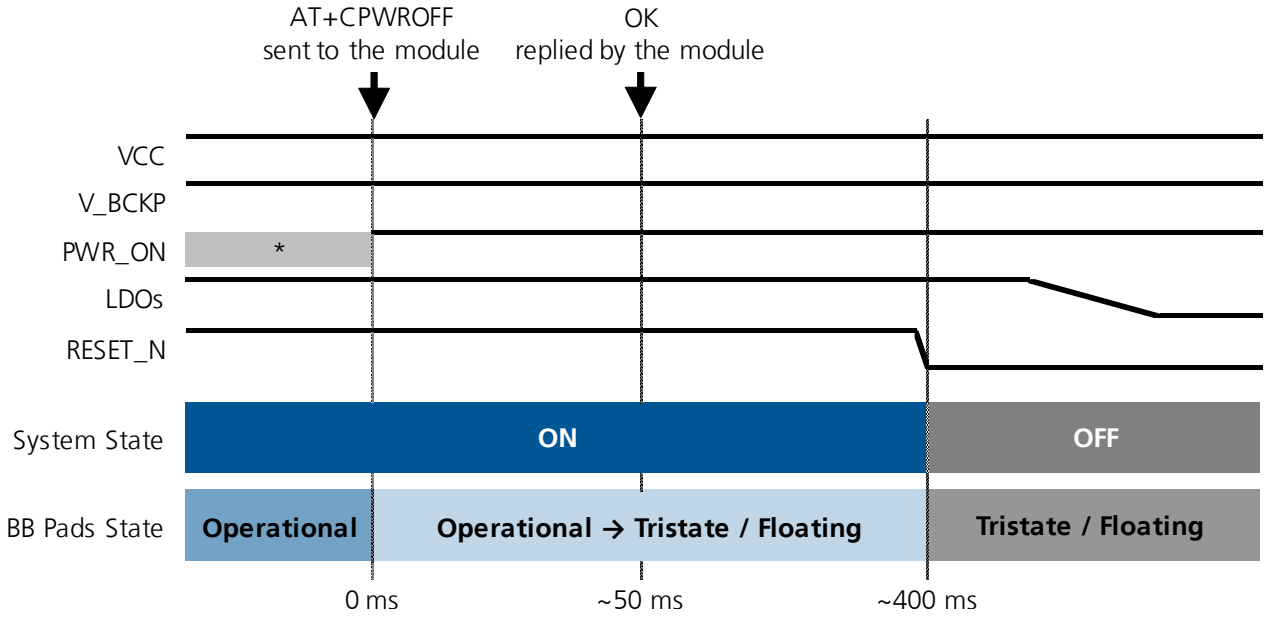

Figure 20: Power off sequence description (* - the PWR_ON signal state is not relevant during this phase)

1.6.3 Module reset

LEON-G100/G200 modules can be reset using the **RESET_N** pin: when the **RESET_N** pin is forced low for at least 50 ms, an "external" or "hardware" reset is performed, that causes an asynchronous reset of the entire module, except for the RTC. Forcing an "external" or "hardware" reset, the current parameter settings are not saved in the module's non-volatile memory and a proper network detach is not performed.

LEON-G100/G200 modules can also be reset by means of the AT command AT+CFUN (more details in u-blox 2G GSM/GPRS AT Commands Manual [2]): in this case an "internal" or "software" reset is performed, that causes, like the "external" or "hardware" reset, an asynchronous reset of the entire module except for the RTC. Forcing an "internal" or "software" reset, the current parameter settings are saved in the module's non-volatile memory and a proper network detach is performed.

The **RESET_N** pin is pulled low by the module when the module is in power-off mode or an internal reset occurs. In these cases an internal open drain FET pulls the line low.

Name	Description	Remarks
RESET_N	Reset signal	A series Schottky diode is integrated in the module as protection. An internal 12.6 kΩ pull-up resistor pulls the line to 1.88 V when the module is not in the reset state. An internal open drain FET pulls the line low when an internal reset occurs and when the module is in power down mode.

Table 12: Reset pin

☞ **RESET_N** pin ESD rating is 1 kV (contact discharge). A higher protection level could be required if the line is externally accessible on the application board. A higher protection level can be achieved mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) on the line connected to this pin if it is externally accessible on the application board.

☞ For more details about the general precautions for ESD immunity about **RESET_N** pin please refer to chapter 2.5.1.

The electrical characteristics of **RESET_N** are different from the other digital I/O interfaces. The high and low logic levels have different operating ranges and absolute maximum ratings. The detailed electrical characteristics are described in the LEON-G100/G200 Data Sheet [1].

As described in the Figure 21, a series Schottky diode is mounted inside the module on the **RESET_N** pin to increase the maximum allowed input voltage up to 4.5 V as operating range. Nevertheless the module senses a low level when the **RESET_N** pin is forced low from the external.

As described in Figure 21, the module has an internal pull-up resistor (12.6 kΩ typical) which pulls the level on the **RESET_N** pin to 1.88 V (typical) when the module is not in reset state. Therefore an external pull-up is not required on the application board.

Forcing **RESET_N** low for at least 50 ms will cause an external reset of the module. When **RESET_N** is released from the low level, the module automatically starts its power-on reset sequence.

If **RESET_N** is connected to an external device (e.g. an application processor on an application board) an open drain output can be directly connected without any external pull-up. Otherwise, use a push-pull output. Make sure to fix the proper level on **RESET_N** in all possible scenarios, to avoid unwanted reset of the module.

The reset state of each digital pin is reported in the pin description table in the LEON-G100/G200 Data Sheet [1].

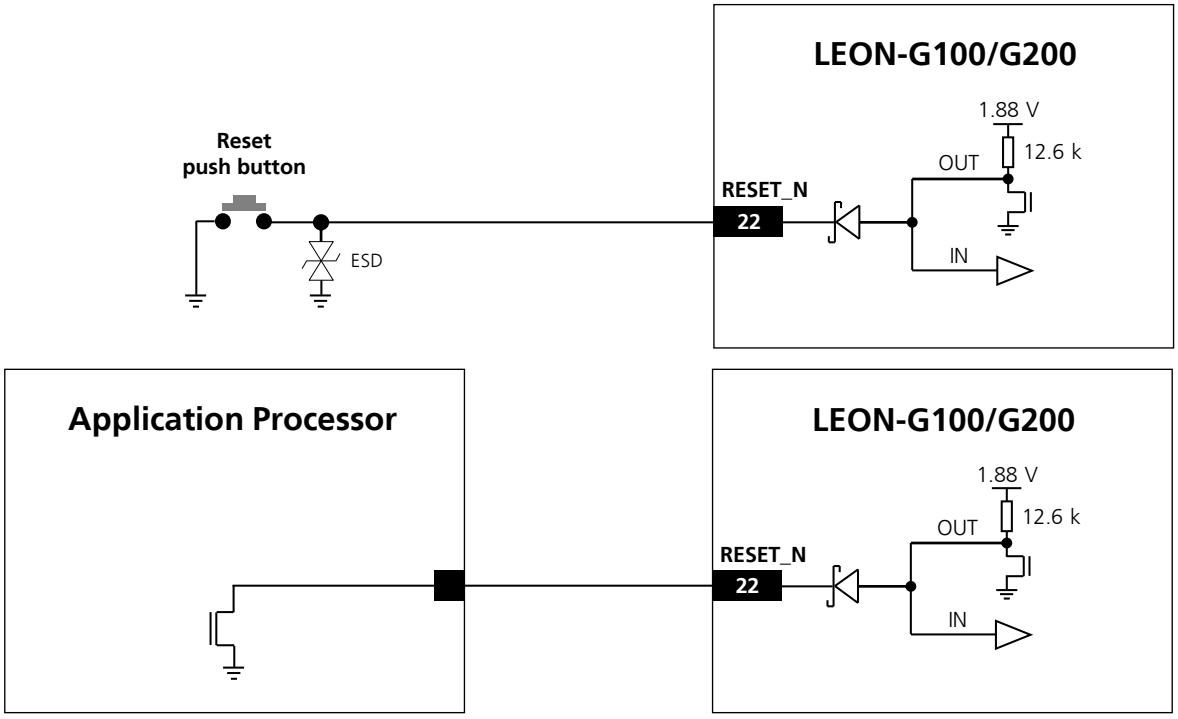

Figure 21: Application circuits to reset the module using a push button or using an application processor

When the module is in power-off mode or an internal reset occurs, **RESET_N** is pulled low by the module itself: **RESET_N** acts as an output pin in these cases since an internal open drain FET (illustrated in Figure 21 and in Figure 22) pulls the line low.

The **RESET_N** pin can indicate to an external application that the module is switched on and is not in the reset state: **RESET_N** is high in these cases and is low otherwise. To sense the **RESET_N** level (i.e. both the high level and the low level), the external circuit has to be able to cause a small current through the series Schottky diode integrated in the module as protection (illustrated in Figure 21 and Figure 22) by means of a very weak pull-down. One of the following application circuits can be implemented to determine the **RESET_N** status:

- **RESET_N** connected to an LED that emits light when the module is powered up and not in reset state and doesn't emit light otherwise, through a biased inverting NPN transistor, with a series base resistor with a resistance value greater or equal to 330 kΩ
- **RESET_N** connected to an input pin of an application processor that senses a low logic level (0 V) when the module is powered up and is not in reset state and senses a high logic level (i.e. 3.0 V) otherwise, through an inverting and level shifting NPN transistor, with a series base resistor with a resistance value greater or equal to 330 kΩ
- **RESET_N** connected to an input pin of the application processor that senses a high logic level (1.8 V) when the module is powered up and is not in reset state and senses a low logic level (0 V) otherwise, through a weak pull-down resistor, with a resistance value greater or equal to 680 kΩ.

Examples of application circuits to sense the **RESET_N** level are shown in the Figure 22.

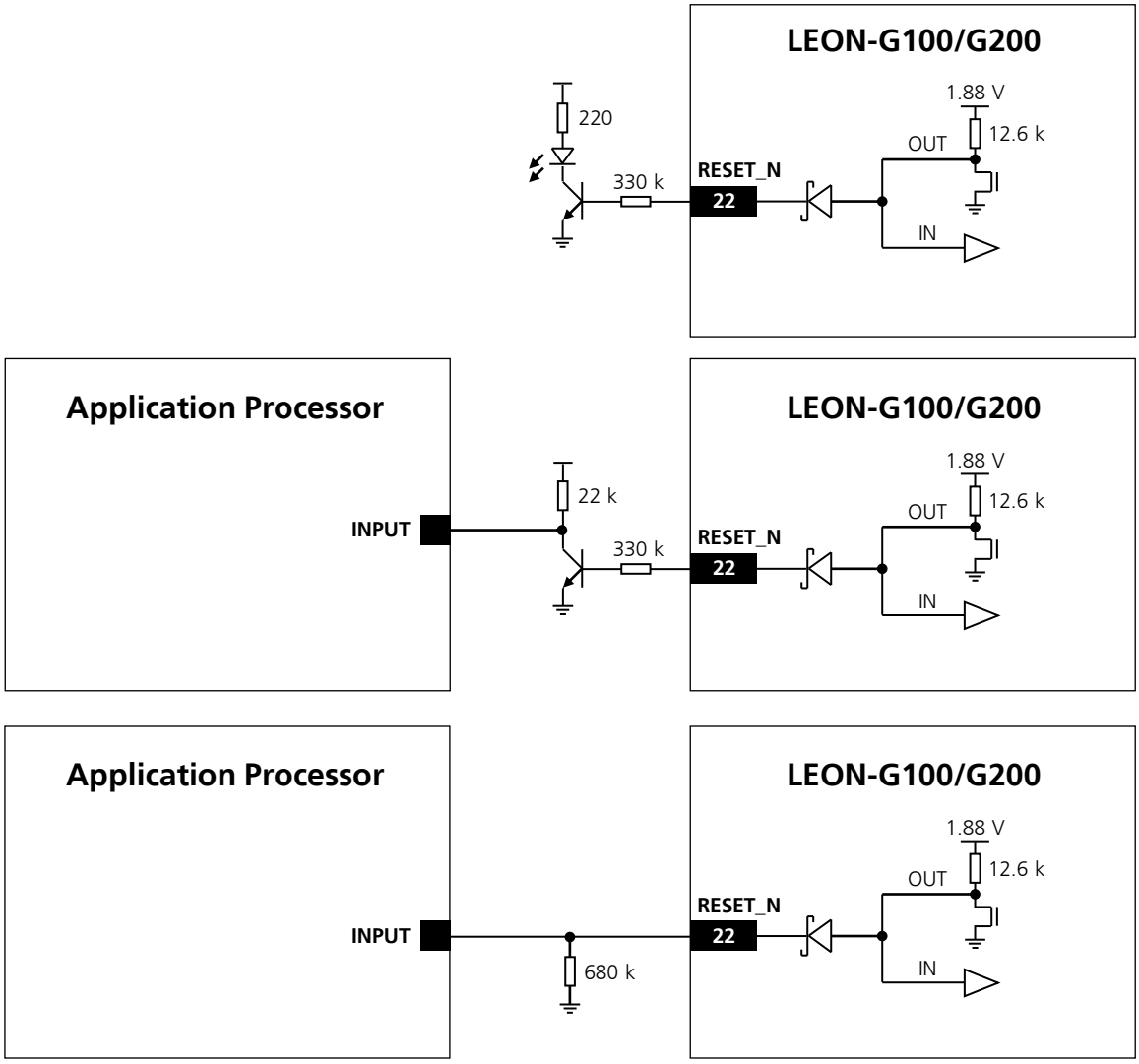

Figure 22: Application circuits to sense if the module is in the reset state

The **RESET_N** is set low by the module for 160 µs to indicate that an internal reset occurs.

The exact low level time interval depends on the implemented circuit, since the fall time of the **RESET_N** low pulse depends on the pull-down value, which must be greater or equal to 680 kΩ.

For example, if LEON **RESET_N** pin is connected through a 680 kΩ pull-down resistor to an input pin of an application processor in the 1.8 V domain (i.e. Vih = 0.7 x 1.8 V = 1.26 V, Vil = 0.3 x 1.8 V = 0.54 V), the low level time interval will be ~145 µs, since the 680 kΩ pull-down forces a ~35 µs 100%-0% fall time, as illustrated in the Figure 23.

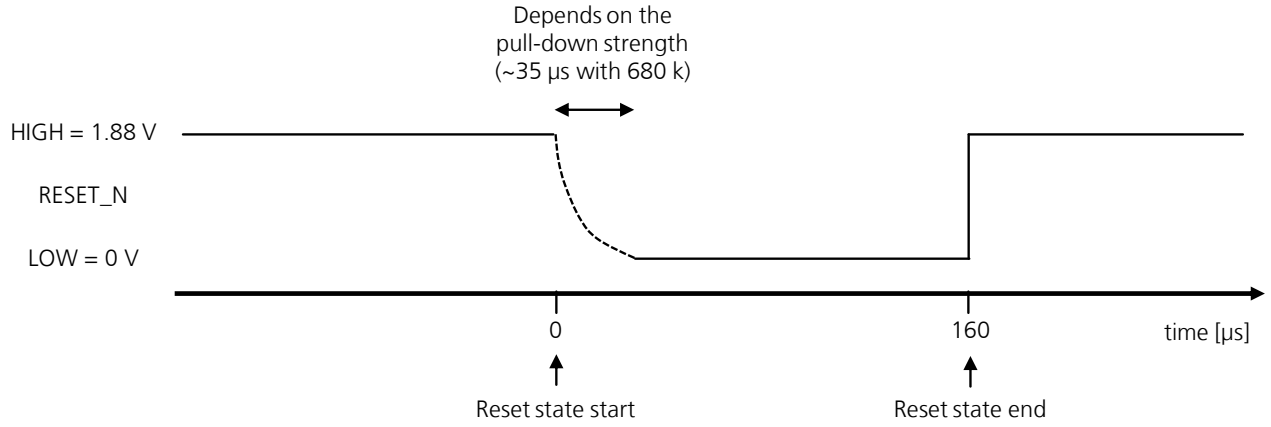

Figure 23: RESET_N behavior due to an internal reset

1.7 RF connection

The **ANT** pin has 50 Ω nominal impedance and must be connected to the antenna through a 50 Ω transmission line to allow transmission and reception of radio frequency (RF) signals in the GSM operating bands.

Name	Description	Remarks
ANT	RF antenna	50 Ω nominal impedance.

Table 13: Antenna pin

ANT port ESD rating is 4 kV (contact discharge). A higher protection level could be required if the line is externally accessible on the application board. A higher protection level can be achieved with an external high pass filter, consists of a 15 pF capacitor (e.g. Murata GRM1555C1H150JA01) and a 39 nH coil (e.g. Murata LQG15HN39NJ02) connected to the **ANT** port. Note that antenna detection functionality will be not provided implementing this high pass filter for ESD protection on the ANT port.

Choose an antenna with optimal radiating characteristics for the best electrical performance and overall module functionality. An internal antenna, integrated on the application board, or an external antenna, connected to the application board through a proper 50 Ω connector, can be used. See section 2.4 and 2.2.1.1 for further details regarding antenna guidelines.

The recommendations of the antenna producer for correct installation and deployment (PCB layout and matching circuitry) must be followed.

If an external antenna is used, the PCB-to-RF-cable transition must be implemented using either a suitable 50 Ω connector, or an RF-signal solder pad (including GND) that is optimized for 50 Ω characteristic impedance.

If antenna supervisor functionality is required, the antenna should have built in DC diagnostic resistor to ground to get proper antenna detection functionality (See section 2.4.3 Antenna detection functionality).

1.8 SIM interface

An SIM card interface is provided on the board-to-board pins of the module. High-speed SIM/ME interface is implemented as well as automatic detection of the required SIM supporting voltage.

Both 1.8 V and 3 V SIM types are supported: activation and deactivation with automatic voltage switch from 1.8 to 3 V is implemented, according to ISO-IEC 78-16-e specifications. The SIM driver supports the PPS (Protocol and Parameter Selection) procedure for baud-rate selection, according to the values determined by the SIM Card.

Table 14 describes the board-to-board pins related to the SIM interface:

Name	Description	Remarks
VSIM	SIM supply	1.80 V typical or 2.85 V typical automatically generated by the module
SIM_CLK	SIM clock	3.25 MHz clock frequency
SIM_IO	SIM data	Internal 4.7 kΩ pull-up to **VSIM**
SIM_RST	SIM reset	

Table 14: SIM Interface pins

A low capacitance ESD protection (e.g. Infineon ESD8V0L2B-03L or AVX USB0002RP or AVX USB0002DP) must be placed near the SIM card holder on each line (**VSIM**, **SIM_IO**, **SIM_CLK**, **SIM_RST**). SIM interface pins ESD rating is 1 kV (contact discharge): higher protection level is required if the lines are connected to a SIM card holder/connector, so they are externally accessible on the application board.

For more details about the general precautions for ESD immunity about SIM pins please refer to chapter 2.5.1.

Figure 24 shows the minimal circuit connecting the LEON and the SIM card.

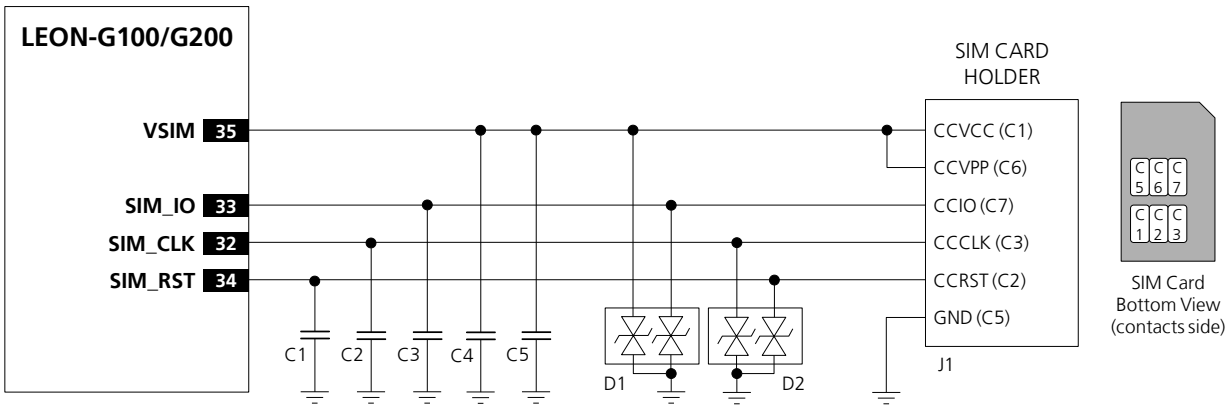

Figure 24: SIM interface application circuit

Reference	Description	Part Number - Manufacturer
C1, C2, C3, C4	47 pF Capacitor Ceramic COG 0402 5% 25 V	GRM1555C1H470JZ01 - Murata
C5	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
D1, D2	ESD Transient Voltage Suppressor	USB0002RP or USB0002DP - AVX
J1	SIM Card Holder	Various Manufacturers, C707-10M006-136-2 - Amphenol Corporation

Table 15: Example of components for SIM card connection

When connecting the module to a SIM card holder, perform the following steps on the application board:

- Bypass digital noise via a 100 nF capacitor (e.g. Murata GRM155R71C104KA01) on the SIM supply (**VSIM**)
- To prevent RF coupling, connect a 47 pF bypass capacitor (e.g. Murata GRM1555C1H470JZ01) at each SIM signal (**VSIM**, **SIM_CLK**, **SIM_IO**, **SIM_RST**) to ground near the SIM connector
- Mount very low capacitance ESD protection (e.g. Infineon ESD8V0L2B-03L or AVX USB0002RP) near the SIM card connector
- Limit capacitance and series resistance on each SIM signal to match the requirements for the SIM interface (27.7 ns is the maximum allowed rise time on the **SIM_CLK** line, 1.0 µs is the maximum allowed rise time on the **SIM_IO** and **SIM_RST** lines): always route the connections to keep them as short as possible

1.8.1 SIM functionality

The following SIM services are supported:

- Abbreviated Dialing Numbers (ADN)
- Fixed Dialing Numbers (FDN)
- Last Dialed Numbers (LDN)
- Service Dialing Numbers (SDN)

SIM Toolkit R96 is supported.

1.9 Serial Communication

1.9.1 Asynchronous serial interface (UART)

The UART interface is a 9-wire unbalanced asynchronous serial interface that provides an AT commands interface, GPRS data and CSD data, software upgrades.

The UART interface provides RS-232 functionality conforming with ITU-T V.24 Recommendation [4], with CMOS compatible signal levels: 0 V for low data bit or ON state, and 2.85 V for high data bit or OFF state. An external voltage translator (Maxim MAX3237) is required to provide RS-232 compatible signal levels. For the detailed electrical characteristics refer to the LEON-G100/G200 Data Sheet [1].

LEON-G100/G200 modules are designed to operate as a GSM/GPRS modem, which represents the data circuit-terminating equipment (DCE) as described by the ITU-T V.24 Recommendation [4]. A customer application processor connected to the module through the UART interface represents the data terminal equipment (DTE).

☞ The signal names of the LEON-G100/G200 UART interface conform to ITU-T V.24 Recommendation [4].

The UART interface includes the following lines:

Name	Description	Remarks
DSR	Data set ready	Module output, functionality of ITU-T V.24 Circuit 107 (Data set ready)
RI	Ring Indicator	Module output, functionality of ITU-T V.24 Circuit 125 (Calling indicator)
DCD	Data carrier detect	Module output, functionality of ITU-T V.24 Circuit 109 (Data channel received line signal detector)
DTR	Data terminal ready	Module input, functionality of ITU-T V.24 Circuit 108/2 (Data terminal ready) Internal active pull-up to 2.85 V enabled.
RTS	Ready to send	Module hardware flow control input, functionality of ITU-T V.24 Circuit 105 (Request to send) Internal active pull-up to 2.85 V enabled.
CTS	Clear to send	Module hardware flow control output, functionality of ITU-T V.24 Circuit 106 (Ready for sending)
TxD	Transmitted data	Module data input, functionality of ITU-T V.24 Circuit 103 (Transmitted data) Internal active pull-up to 2.85 V enabled.
RxD	Received data	Module data output, functionality of ITU-T V.24 Circuit 104 (Received data)

Table 16: UART pins

☞ UART interface pins ESD rating is 1 kV (contact discharge). A higher protection level could be required if the lines are externally accessible on the application board. A higher protection level can be achieved mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) on the lines connected to these pins if they are externally accessible on the application board.

1.9.1.1 UART features

UART interface is controlled and operated with:

- AT commands according to 3GPP TS 27.007 [5]
- AT commands according to 3GPP TS 27.005 [6]
- AT commands according to 3GPP TS 27.010 [7]
- u-blox AT commands

All flow control handshakes are supported by the UART interface and can be set by appropriate AT commands (see u-blox 2G GSM/GPRS AT Commands Manual [2]): hardware flow control (RTS/CTS), software flow control (XON/XOFF), or no flow control.

Autobauding is supported. It can be enabled or disabled by an AT command (see u-blox 2G GSM/GPRS AT Commands Manual [2]). Autobauding is enabled by default.

☞ Hardware flow control is enabled by default.

☞ For the complete list of supported AT commands and their syntax refer to the u-blox 2G GSM/GPRS AT Commands Manual [2].

☞ Autobauding result can be unpredictable with spurious data if idle-mode (power-saving) is entered and the hardware flow control is disabled.

The following baud rates can be configured using AT commands:

- 2400 b/s

- 4800 b/s
- 9600 b/s
- 19200 b/s
- 38400 b/s
- 57600 b/s
- 115200 b/s (default value when autobauding is disabled)

The following baud-rates are available with autobauding only:

- 1200 b/s
- 230400 b/s

Automatic frame recognition is supported: this feature is enabled in conjunction with autobauding only, which is enabled by default. The frame format can be:

- 8N1 (8 data bits, No parity, 1 stop bit)
- 8E1 (8 data bits, even parity, 1 stop bit)
- 8O1 (8 data bits, odd parity, 1 stop bit)
- 8N2 (8 data bits, No parity, 2 stop bits)

The default frame configuration with fixed baud rate is 8N1, described in the Figure 25.

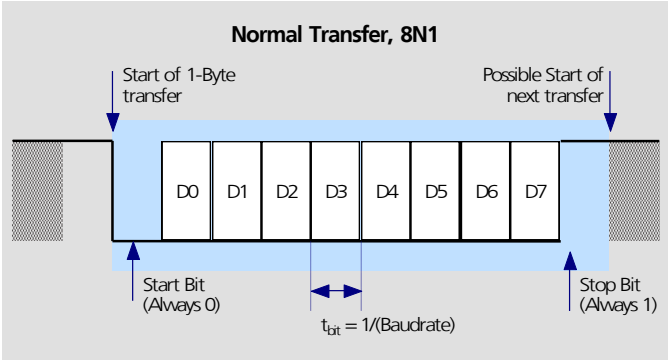

Figure 25: UART default frame format (8N1) description

1.9.1.2 UART signal behavior (AT commands interface case)

See Table 2 for a description of operating modes and states referred to in this section.

At the module switch-on, before the initialization of the UART interface (each pin is first tristated and then set to its relative reset state reported in the pin description table in LEON-G100/G200 Data Sheet [1] (see the power on sequence description in Figure 19). At the end of the boot sequence, the UART interface is initialized, the module is by default in active mode and the UART interface is enabled. The configuration and the behavior of the UART signals after the boot sequence are described below.

☞ For a complete description of data and command mode please refer to u-blox 2G GSM/GPRS AT Commands Manual [2].

RxD signal behavior

The module data output line (**RxD**) is set by default to OFF state (high level) at UART initialization. The module holds **RxD** in OFF state until no data is transmitted by the module.

TxD signal behavior

The module data input line (**TxD**) is set by default to OFF state (high level) at UART initialization. The **TxD** line is then held by the module in the OFF state if the line is not activated by the DTE: an active pull-up is enabled inside the module on the **TxD** input.

CTS signal behavior

The module hardware flow control output (**CTS** line) is set to the ON state (low level) at UART initialization.

If the hardware flow control is enabled (for more details please refer to u-blox 2G GSM/GPRS AT Commands Manual [2], AT&K, AT\Q, AT+IFC AT command) the **CTS** line indicates when the module is in active mode and the UART interface is enabled: the module drives the **CTS** line to the ON state or to the OFF state when it is either able or not able to accept data from the DTE (refer to chapter 1.9.1.3 for the complete description).

If the hardware flow control is not enabled, the **CTS** line is always held in the ON state after UART initialization.

☞ When the power saving configuration is enabled and the hardware flow-control is not implemented in the DTE/DCE connection, data sent by the DTE can be lost: the first character sent when the module is in idle-mode won't be a valid communication character (refer to chapter 1.9.1.3 for the complete description).

☞ During the MUX mode, the **CTS** line state is mapped to FCon / FCoff MUX command for flow control issues outside the power saving configuration while the physical **CTS** line is still used as a power state indicator. For more details please refer to Mux Implementation Application Note [14].

RTS signal behavior

The hardware flow control input (**RTS** line) is set by default to the OFF state (high level) at UART initialization. The **RTS** line is then held by the module in the OFF state if the line is not activated by the DTE: an active pull-up is enabled inside the module on the **RTS** input.

If the HW flow control is enabled (for more details please refer to u-blox GSM/GPRS AT Commands Manual [2] AT&K, AT\Q, AT+IFC command description) the **RTS** line is monitored by the module to detect permission from the DTE to send data to the DTE itself. If the **RTS** line is set to OFF state, any on-going data transmission from the module is immediately interrupted or any subsequent transmission forbidden until the **RTS** line changes to ON state.

☞ The DTE must be able to still accept a certain number of characters after the **RTS** line has been set to OFF state: the module guarantees the transmission interruption within 2 characters from **RTS** state change.

If AT+UPSV=2 is set and HW flow control is disabled, the **RTS** line is monitored by the module to manage the power saving configuration:

- When an OFF-to-ON transition occurs on the **RTS** input line, the module switches from idle-mode to active-mode after 20 ms and the module doesn't enter idle-mode until the **RTS** input line is held in the ON state
- If **RTS** is set to OFF state by the DTE, the module automatically enters idle-mode whenever possible as in the AT+UPSV=1 configuration (cyclic idle/active mode)

For more details please refer to chapter 1.9.1.3 and u-blox 2G GSM/GPRS AT Commands Manual [2], AT+UPSV command.

DSR signal behavior

If AT&S0 is set, the **DSR** module output line is set by default to ON state (low level) at UART initialization and is then always held in the ON state.

If AT&S1 is set, the **DSR** module output line is set by default to OFF state (high level) at UART initialization. The **DSR** line is then set to the OFF state when the module is in command mode and is set to the ON state when the module is in data mode.

DTR signal behavior

The **DTR** module input line is set by default to OFF state (high level) at UART initialization. The **DTR** line is then held by the module in the OFF state if the line is not activated by the DTE: an active pull-up is enabled inside the module on the **DTR** input. Module behavior according to **DTR** status depends on the AT command configuration (see u-blox 2G GSM/GPRS AT Commands Manual [2], &D AT command).

DCD signal behavior

If AT&C0 is set, the **DCD** module output line is set by default to ON state (low level) at UART initialization and is then always held in the ON state.

If AT&C1 is set, the **DCD** module output line is set by default to OFF state (high level) at UART initialization. The **DCD** line is then set by the module in accordance with the carrier detect status: ON if the carrier is detected, OFF otherwise. In case of voice call **DCD** is set to ON state when the call is established. For a data call there are the following scenarios:

- **GPRS data communication**: Before activating the PPP protocol (data mode) a dial-up application must provide the ATD*99***<context_number># to the module: with this command the module switches from command mode to data mode and can accept PPP packets. The module sets the **DCD** line to the ON state, then answers with a CONNECT to confirm the ATD*99 command. Please note that the **DCD** ON is not related to the context activation but with the data mode
- **CSD data call**: To establish a data call the DTE can send the ATD<number> command to the module which sets an outgoing data call to a remote modem (or another data module). Data can be transparent (non reliable) or non transparent (with the reliable RLP protocol). When the remote DCE accepts the data call, the module DCD line is set to ON and the CONNECT <communication baudrate> string is returned by the module. At this stage the DTE can send characters through the serial line to the data module which sends them through the network to the remote DCE attached to a remote DTE

RI signal behavior

The **RI** module output line is set by default to the OFF state (high level) at UART initialization. Then, during an incoming call, the **RI** line is switched from OFF state to ON state with a 4:1 duty cycle and a 5 s period (ON for 1 s, OFF for 4 s, see Figure 26), until the DTE attached to the module sends the ATA string and the module accepts the incoming data call. The RING string sent by the module (DCE) to the serial port at constant time intervals is not correlated with the switch of the **RI** line to the ON state.

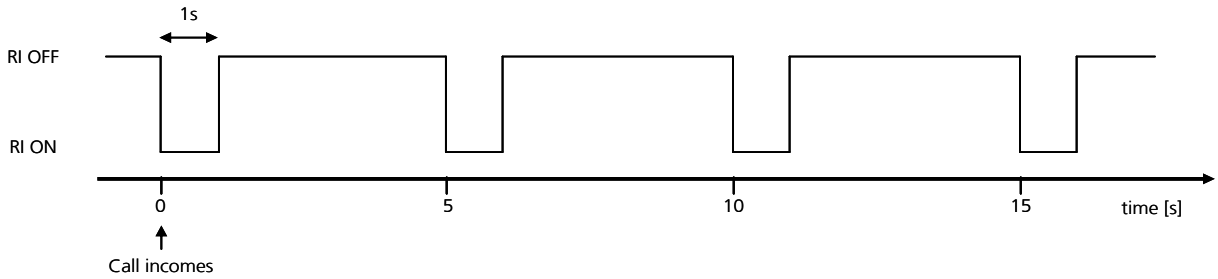

Figure 26: RI behavior during an incoming call

The **RI** line can notify an SMS arrival. When the SMS arrives, the **RI** line switches from OFF to ON for 1 s (see Figure 27), if the feature is enabled by the proper AT command (please refer to u-blox 2G GSM/GPRS AT Commands Manual [2], AT+CNMI command).

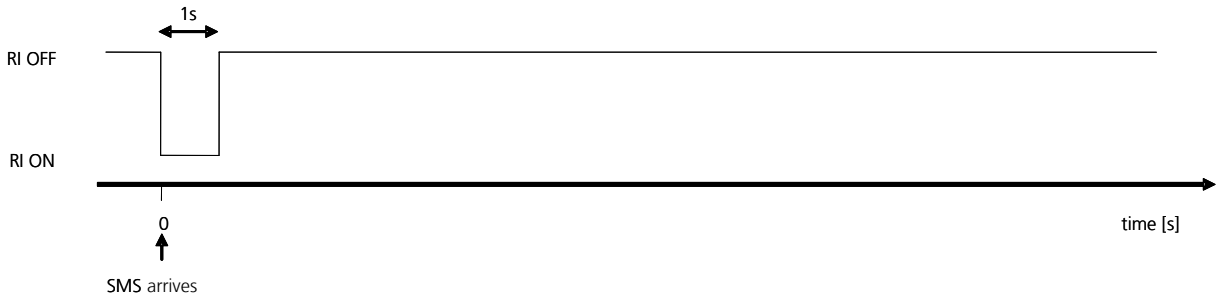

Figure 27: RI behavior at SMS arrival

1.9.1.3 UART and power-saving

The power saving configuration is controlled by the AT+UPSV command (for the complete description please refer to u-blox 2G GSM/GPRS AT Commands Manual [2], AT+UPSV command). When power saving is enabled, the module automatically enters idle-mode whenever possible, otherwise the active-mode is maintained by the module. The AT+UPSV command sets the module power saving configuration, but also configures the UART behavior in relation to the power saving configuration. The conditions for the module entering idle-mode also depend on the UART power saving configuration.

The different power saving configurations that can be set by the AT+UPSV command are described in the following subchapters and are summarized in Table 17. For more details on the command description please refer to u-blox AT commands Manual [2].

AT+UPSV	HW flow control	RTS line	Communication during idle mode and wake up
0	Enabled (AT&K3)	ON	Data sent by the DTE will be correctly received by the module.
0	Enabled (AT&K3)	OFF	Data sent by the module will be buffered by the module and will be correctly received by the DTE when it will be ready to receive data (i.e. **RTS** line will be ON).
0	Disabled (AT&K0)	ON	Data sent by the DTE will be correctly received by the module.
0	Disabled (AT&K0)	OFF	Data sent by the module will be correctly received by the DTE if it is ready to receive data, otherwise data will be lost.
1	Enabled (AT&K3)	ON	Data sent by the DTE will be buffered by the DTE and will be correctly received by the module when active-mode is entered.
1	Enabled (AT&K3)	OFF	Data sent by the module will be buffered by the module and will be correctly received by the DTE when it is ready to receive data (i.e. **RTS** line will be ON).
1	Disabled (AT&K0)	ON	When a low-to-high transition occurs on the **TxD** input line, the module switches from idle-mode to active-mode after 20 ms: this is the "wake up time" of the module. As a consequence, the first character sent when the module is in idle-mode (i.e. the wake up character) won't be a valid communication character because it can't be recognized, and the recognition of the subsequent characters is guaranteed only after the complete wake-up (i.e. after 20 ms).
1	Disabled (AT&K0)	OFF	Data sent by the module will be correctly received by the DTE if it is ready to receive data, otherwise data will be lost.
2	Enabled (AT&K3)	ON	Not Applicable: HW flow control cannot be enabled with AT+UPSV=2.
2	Enabled (AT&K3)	OFF	Not Applicable: HW flow control cannot be enabled with AT+UPSV=2.
2	Disabled (AT&K0)	ON	The module is forced in active-mode and it doesn't enter idle-mode until **RTS** line is set to OFF state. When a high-to-low (i.e. OFF-to-ON) transition occurs on the **RTS** input line, the module switches from idle-mode to active-mode after 20 ms: this is the "wake up time" of the module.

AT+UPSV	HW flow control	RTS line	Communication during idle mode and wake up
2	Disabled (AT&K0)	OFF	When a low-to-high transition occurs on the **TxD** input line, the module switches from idle-mode to active-mode after 20 ms: this is the "wake up time" of the module. As a consequence, the first character sent when the module is in idle-mode (i.e. the wake up character) won't be a valid communication character because it can't be recognized, and the recognition of the subsequent characters is guaranteed only after the complete wake-up (i.e. after 20 ms).

Table 17: UART and power-saving summary

AT+UPSV=0: power saving disabled, fixed active-mode

The module doesn't enter idle-mode and the **CTS** line is always held in the ON state after UART initialization. The UART interface is enabled and data can be received. This is the default configuration.

AT+UPSV=1: power saving enabled, cyclic idle/active mode

The module automatically enters idle-mode whenever possible, and periodically wakes up from idle-mode to active-mode to monitor the paging channel of the current base station (paging block reception), in accordance to GSM system requirements.

Idle-mode time is fixed by network parameters and can be up to ~2.1 s. When the module is in idle-mode, a data transmitted by the DTE will be lost if hardware flow control is disabled, otherwise if hardware flow control is enabled, data will be buffered by the DTE and will be correctly received by the module when active-mode is entered.

When the module wakes up to active-mode, the UART interface is enabled and data can be received. When a character is received, it forces the module to stay in the active-mode for a longer time.

The active-mode duration depends by:

- Network parameters, related to the time interval for the paging block reception (minimum of ~11 ms)
- Time period from the last data received at the serial port during the active-mode: the module doesn't enter idle-mode until a timeout expires. This timeout is configurable by the +UPSV AT command, from 40 GSM frames (~184 ms) up to 65000 GSM frames (300 s). Default value is 2000 GSM frames (~9.2 s).

  Every subsequent character received during the active-mode, resets and restarts the timer; hence the active-mode duration can be extended indefinitely.

The behavior of hardware flow-control output (**CTS** line) during normal module operations with power-saving and HW flow control enabled (cyclic idle-mode and active-mode) is illustrated in Figure 28.

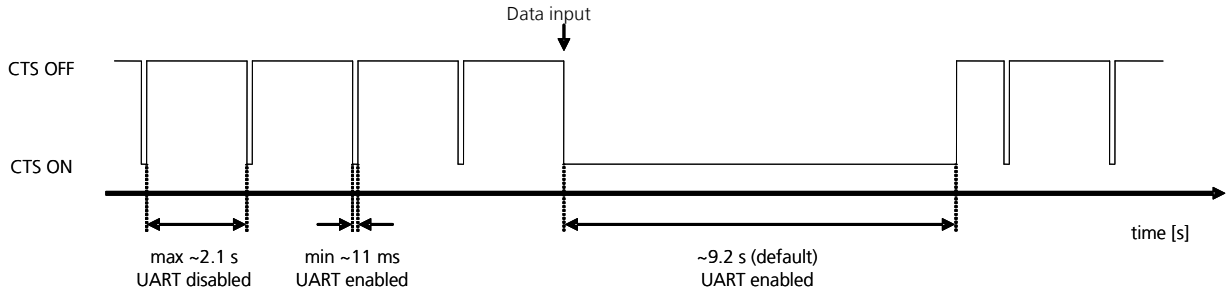

Figure 28: CTS behavior with power saving enabled: the CTS line indicates when the module is able (CTS = ON = low level) or not able (CTS = OFF = high level) to accept data from the DTE and communicate through the UART interface

AT+UPSV=2: power saving enabled and controlled by the RTS line

The module behavior is the same as for +UPSV=1 case if the **RTS** line is set to OFF by the DTE.

When an OFF-to-ON transition occurs on the **RTS** input line, the module switches from idle-mode to active-mode after 20 ms and then the module doesn't enter the idle-mode until the **RTS** input line is held in the ON state. This configuration can only be enabled with the module HW flow control disabled.

Even if HW flow control is disabled, if the **RTS** line is set to OFF by the DTE, the **CTS** line is set by the module accordingly to its power saving configuration (like for +UPSV=1 with HW flow control enabled).

When the **RTS** line is set to OFF by the DTE, the timeout to enter idle-mode from the last data received at the serial port during the active-mode is the one previously set with the AT+UPSV=1 configuration or it is the default value.

Wake up from idle-mode to active-mode via data reception

If a data is transmitted by the DTE during the module idle-mode, it will be lost (not correctly received by the module) in the following cases:

- +UPSV=1 with hardware flow control disabled
- +UPSV=2 with hardware flow control disabled and RTS line set to OFF

When the module is in idle-mode, the **TxD** input line of the module is always configured to wake up the module from idle-mode to active-mode via data reception: when a low-to-high transition occurs on the **TxD** input line, it causes the wake-up of the system. The module switches from idle-mode to active-mode after 20 ms from the first data reception: this is the "wake up time" of the module. As a consequence, the first character sent when the module is in idle-mode (i.e. the wake up character) won't be a valid communication character because it can't be recognized, and the recognition of the subsequent characters is guaranteed only after the complete wake-up (i.e. after 20 ms).

Figure 29 and Figure 30 show an example of common scenarios and timing constraints:

- HW flow control set in the DCE, and no HW flow control set in the DTE, needed to see the **CTS** line changing on DCE
- Power saving configuration is active and the timeout from last data received to idle-mode start is set to 2000 frames (AT+UPSV=1,2000)

Figure 29 shows the case where DCE is in idle mode and a wake-up is forced. In this scenario the only character sent by the DTE is the wake-up character; as a consequence, the DCE will return to idle-mode when the timeout from last data received expires. (2000 frames without data reception).

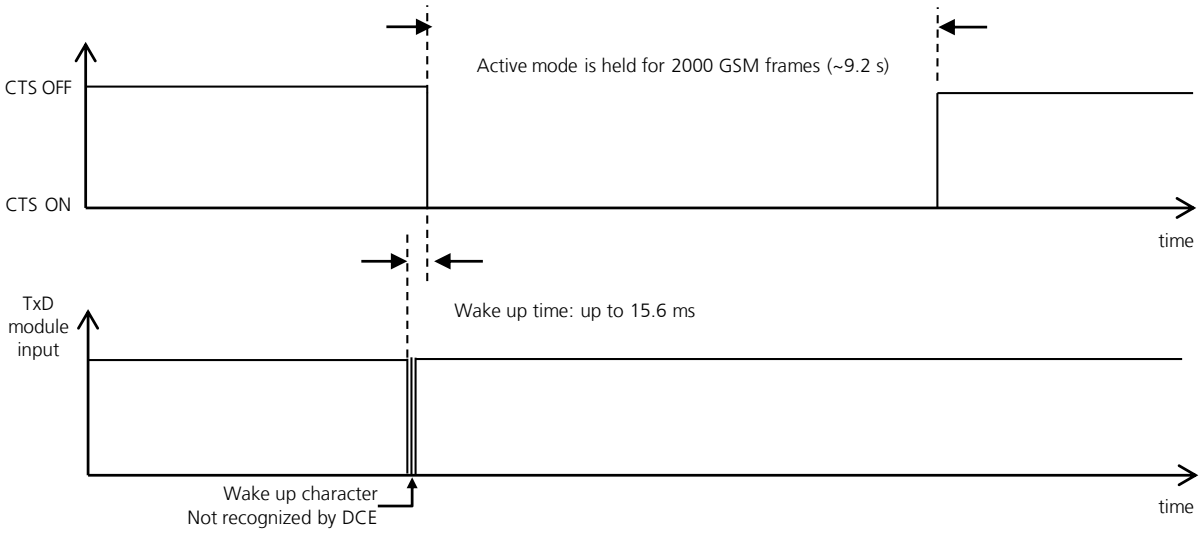

Figure 29: Wake-up via data reception without further communication

Figure 30 shows the case where in addition to the wake-up character further (valid) characters are sent. The wake up character wakes-up the DCE. The other characters must be sent after the "wake up time" of 20 ms. If this condition is met, the characters are recognized by the DCE. The DCE is allowed to re-enter idle-mode after 2000 GSM frames from the latest data reception.

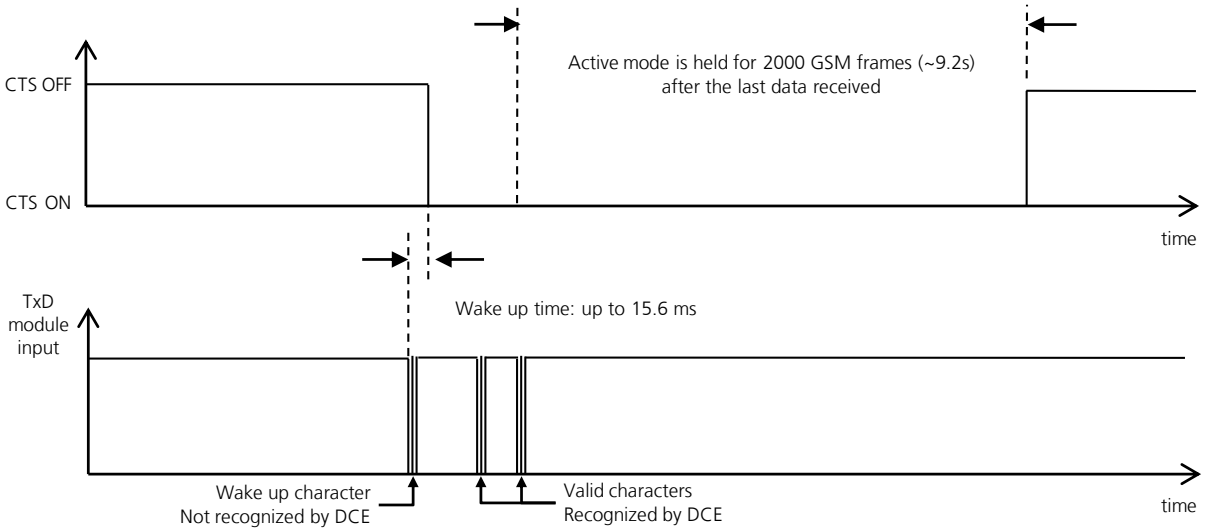

Figure 30: Wake-up via data reception with further communication

- The "wake-up via data reception" feature can't be disabled.
- The "wake-up via data reception" feature can be used in both +UPSV=1 and +UPSV=2 case (when **RTS** line is set to OFF).
- In command mode, if autobauding is enabled and HW flow control is not implemented by the DTE, the DTE must always send a character to the module before the "AT" prefix set at the beginning of each command line: the first character will be ignored if the module is in active-mode, or it will represent the wake up character if the module is in idle-mode.
- In command mode, if autobauding is disabled, the DTE must always send a dummy "AT" to the module before each command line: the first character will not be ignored if the module is in active-mode (i.e. the module will reply "OK"), or it will represent the wake up character if the module is in idle-mode (i.e. the module won't reply).
- No wake-up character or dummy "AT" is required from the DTE during connected-mode since the module continues to be in active-mode and doesn't need to be woken-up. Furthermore in data mode a wake-up character or a dummy "AT" would affect the data communication.

1.9.1.4 UART application circuits

Providing the full RS-232 functionality (using the complete V.24 link)

For complete RS-232 functionality conforming to ITU-T Recommendation [4] in DTE/DCE serial communication, the complete UART interface of the module (DCE) must be connected to the DTE as described in Figure 31.

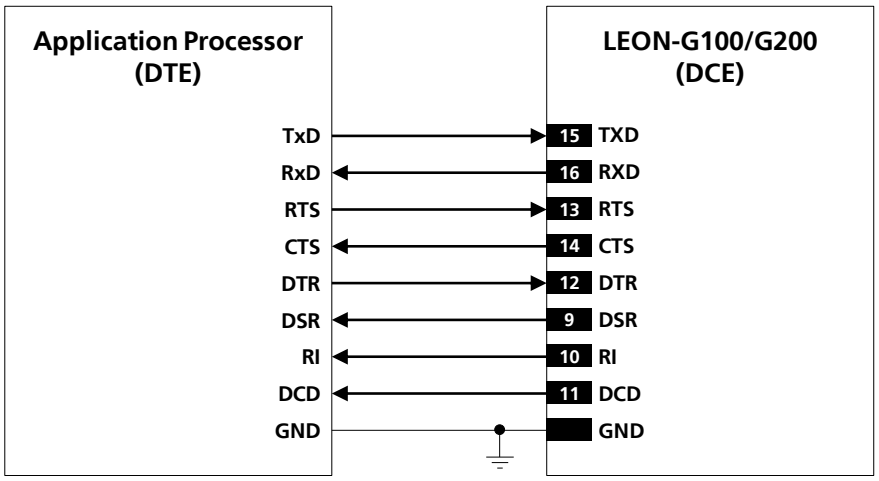

Figure 31: UART interface application circuit with complete V.24 link in the DTE/DCE serial communication

Providing the TxD, RxD, RTS and CTS lines only (not using the complete V.24 link)

If the functionality of the **DSR**, **DCD**, **RI** and **DTR** lines is not required in the application, or the lines are not available, the application circuit described in Figure 32 must be implemented:

- Connect the module **DTR** input line to GND, since the module requires **DTR** active (low electrical level)
- Leave **DSR**, **DCD** and **RI** lines of the module unconnected and floating

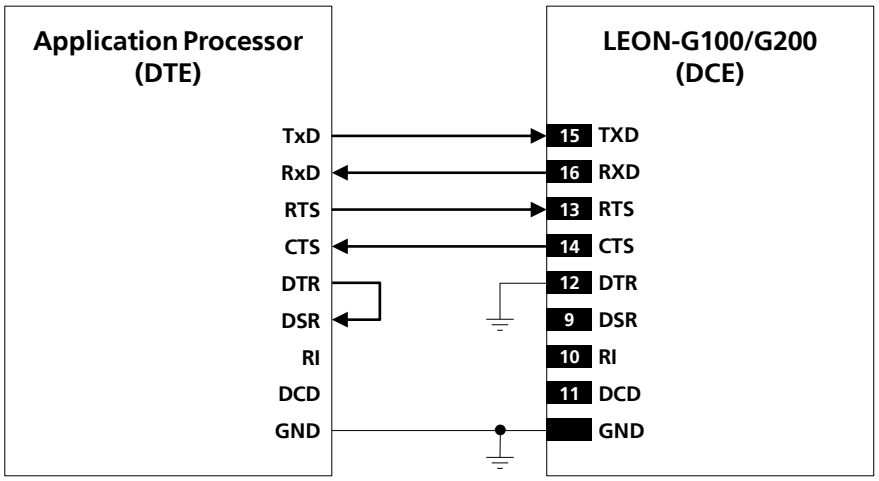

Figure 32: UART interface application circuit with partial V.24 link (5-wire) in the DTE/DCE serial communication

If only **TxD**, **RxD**, **RTS** and **CTS** lines are provided as described in Figure 32 the procedure to enable the power saving depends on the HW flow-control status. If HW flow-control is enabled (AT&K3, that is the default setting) the power saving will be activated by AT+UPSV=1. Through this configuration, when the module is in idle-mode, a data transmitted by the DTE will be buffered by the DTE and will be correctly received by the module when active-mode is entered.

If the HW flow-control is disabled (AT&K0), the power saving can be enabled by AT+UPSV=2. The module is in idle-mode until a high-to-low (i.e. OFF-to-ON) transition on the **RTS** input line will switch the module from

idle-mode to active-mode after 20 ms. The module will be forced in active-mode if the **RTS** input line is held in the ON state.

Providing the TxD and RxD lines only (not using the complete V24 link)

If the functionality of the **CTS**, **RTS**, **DSR**, **DCD**, **RI** and **DTR** lines is not required in the application, or the lines are not available, the application circuit described in Figure 33 must be implemented:

- Connect the module **CTS** output line to the module **RTS** input line, since the module requires **RTS** active (low electrical level) if HW flow-control is enabled (AT&K3, that is the default setting), and **CTS** is active (low electrical level) when the module is in active mode, the UART interface is enabled and the HW flow-control is enabled
- Connect the module **DTR** input line to GND, since the module requires **DTR** active (low electrical level)
- Leave **DSR**, **DCD** and **RI** lines of the module unconnected and floating

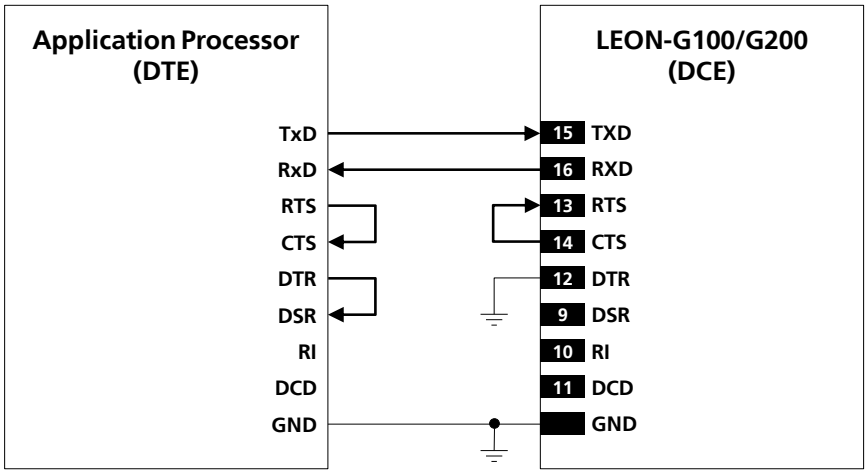

Figure 33: UART interface application circuit with partial V.24 link (3-wire) in the DTE/DCE serial communication

If only **TxD** and **RxD** lines are provided as described in Figure 33 and HW flow-control is disabled (AT&K0), the power saving will be enabled by AT+UPSV=1. The module enters active-mode 20 ms after a low-to-high transition on the **TxD** input line; the recognition of the subsequent characters is guaranteed until the module is in active-mode.

☞ A data delivered by the DTE can be lost using this configuration and the following settings:

- HW flow-control enabled in the module (AT&K3, that is the default setting)
- Module power saving enabled by AT+UPSV=1
- HW flow-control disabled in the DTE

In this case the first character sent when the module is in idle-mode will be a wake-up character and won't be a valid communication character (refer to chapter 1.9.1.3 for the complete description).

☞ If power saving is enabled the application circuit with the **TxD** and **RxD** lines only is not recommended. During command mode the DTE must send to the module a wake-up character or a dummy "AT" before each command line (refer to chapter 1.9.1.3 for the complete description), but during data mode the wake-up character or the dummy "AT" would affect the data communication.

Additional considerations

☞ To avoid an increase in module power consumption, any external signal connected to the UART must be set low or tri-stated when the module is in power-down mode. If the external signals in the application circuit connected to the UART cannot be set low or tri-stated, a multi channel digital switch (e.g. Texas Instruments SN74CB3Q16244) or a single channel analog switch (e.g. Texas Instruments TS5A3159 or Texas Instruments TS5A63157) must be inserted between the two-circuit connections and set to high impedance when the module is in power-down mode.

☞ It is highly recommended to provide on an application board a direct access to **RxD** and **TxD** lines of the module (in addition to access to these lines from an application processor). This enables a direct connection of PC (or similar) to the module for execution of Firmware upgrade over the UART. Note that the module FW upgrade over UART (using the **RxD** and **TxD** pins) starts at the module switch-on or when the module is released from the reset state: it is suggested to provide access to the **PWR_ON** pin, or to provide access to the **RESET_N** pin, or to provide access to the enabling of the DC supply connected to the **VCC** pin, to start the module firmware upgrade over the UART.

1.9.1.5 MUX Protocol (3GPP 27.010)

The module has a software layer with MUX functionality complaint with 3GPP 27.010 [7].

This is a data link protocol (layer 2 of OSI model) using HDLC-like framing and operates between the module (DCE) and the application processor (DTE). The protocol allows simultaneous sessions over the UART. Each session consists of a stream of bytes transferring various kinds of data like SMS, CBS, GPRS, AT commands in general. This permits, for example, SMS to be transferred to the DTE when a data connection is in progress.

The following channels are defined:

- Channel 0: control channel
- Channel 1 – 5: AT commands /data connection
- Channel 6: GPS tunneling

For more details please refer to GSM Mux implementation Application Note [14].

1.9.2 DDC (I^2C) interface

1.9.2.1 Overview

An I^2C compatible Display Data Channel (DDC) interface for serial communication is implemented. This interface is intended exclusively to access u-blox GPS receivers.

Name	Description	Remarks
SCL	I^2C bus clock line	Fixed open drain. External pull-up required.
SDA	I^2C bus data line	Fixed open drain. External pull-up required.

Table 18: DDC pins

☞ DDC (I^2C) interface pins ESD rating is 1 kV (contact discharge). A higher protection level could be required if the lines are externally accessible on the application board. A higher protection level can be achieved mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) on the lines connected to these pins if they are externally accessible on the application board.

To be complaint with the I²C bus specifications, the module pads of the bus interface are open drain output and pull up resistors must be used. Since the pull-up resistors are not mounted on the module, they must be mounted externally. Resistor values must conform to the I²C bus specifications [8]. If LEON-G100/G200 modules are connected through the DDC bus to a single u-blox GPS receiver only (only one device is connected on the DDC bus), use a pull-up resistor of 4.7 kΩ. Pull-ups must be connected to a supply voltage of 2.85 V (typical), since this is the voltage domain of the DDC pins (for detailed electrical characteristics see the LEON-G100/G200 Data Sheet [1]).

DDC Slave-mode operation is not supported, the module can act as master only.

Two lines, serial data (**SDA**) and serial clock (**SCL**), carry information on the bus. **SCL** is used to synchronize data transfers, and **SDA** is the data line. Since both lines are open drain outputs, the DDC devices can only drive them low or leave them open. The pull-up resistor pulls the line up to the supply rail if no DDC device is pulling it down to GND. If the pull-ups are missing, **SCL** and **SDA** lines are undefined and the DDC bus will not work.

The signal shape is defined by the values of the pull-up resistors and the bus capacitance. Long wires on the bus will increase the capacitance. If the bus capacitance is increased, use pull-up resistors with nominal resistance value lower than 4.7 kΩ, to match the I²C bus specifications [8] regarding rise and fall times of the signals.

☞ Capacitance and series resistance must be limited on the bus to match the I²C specifications [8] (1.0 µs is the maximum allowed rise time on the **SCL** and **SDA** lines): route connections as short as possible.

☞ The module doesn't enter idle-mode when the DDC (I²C) interface is enabled, even if power saving is enabled by the AT+UPSV command.

☞ If the pins are not used as DDC bus interface, they can be left floating on the application board.

1.9.2.2 DDC application circuit

The **SDA** and **SCL** lines can only be used to connect the LEON module to a u-blox GPS module: LEON DDC (I²C) interface is enabled by the +UGPS AT command only (for more details please refer to u-blox 2G GSM/GPRS AT Commands Manual [2]).

GPIO2 is driven as output by the +UGPS AT command to switch-on or switch-off the u-blox GPS module, connecting **GPIO2** to the active-high enable pin (or the active-low shutdown pin) of the voltage regulator that supplies the u-blox GPS module on the application board.

The application circuit for the connection of a LEON wireless module to a u-blox 3.0 V GPS receiver is illustrated in Figure 34 and the suggested components are listed in Table 19. A pull-down resistor is mounted on the **GPIO2** line to avoid a switch on of the GPS module when the LEON module is switched-off and its digital pins are tri-stated.

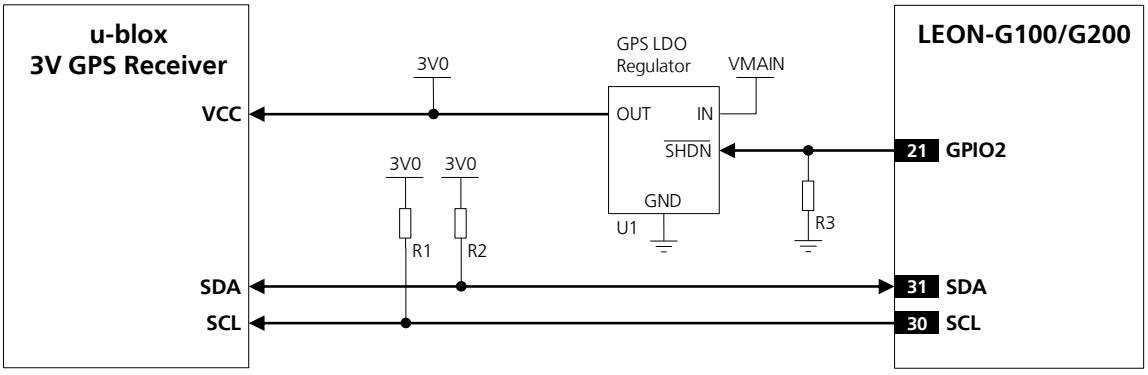

Figure 34: Application circuit for 3V u-blox GPS receivers

Reference	Description	Part Number - Manufacturer
R1, R2, R3	4.7 kΩ Resistor 0402 5% 0.1 W	RC0402JR-074K7L - Yageo Phycomp
U1	Voltage Regulator for GPS Receiver	See GPS Receiver Hardware Integration Manual

Table 19 - Component for DDC application circuit

1.9.2.3 DDC application circuit for LEON-G100/G200 upcoming version

☞ This section applies to the upcoming FW/HW version of LEON-G100/G200.

The **SDA** and **SCL** lines can be used only to connect the LEON module to a u-blox GPS receiver: LEON DDC (I^2C) interface is enabled by the +UGPS AT command only (for more details refer to u-blox 2G GSM/GPRS AT Commands Manual [2]).

GPIO2 is driven as an output by the +UGPS AT command to switch on or to switch off the u-blox GPS receiver, connecting **GPIO2** to the active-high enable pin (or the active-low shutdown pin) of the voltage regulator that supplies the u-blox GPS module on the application board.

The pin **#23** is driven as an input by the +UGPS AT command to sense when the u-blox GPS module is ready to send data.

The pin **#24** is driven as an output by the +UGPS AT command to provide a synchronization timing signal to the u-blox GPS module.

The application circuit for the connection of a LEON wireless module to a u-blox 3.0 V GPS receiver is illustrated in Figure 35 and the suggested components are listed in Table 20. A pull-down resistor is mounted on the **GPIO2** line to avoid a switch on of the GPS module when the LEON module is switched-off and its digital pins are tri-stated.

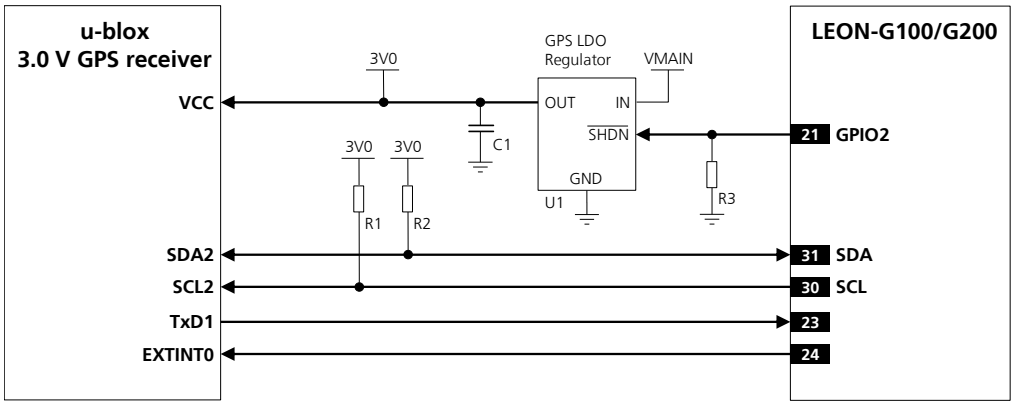

Figure 35: Application circuit for u-blox 3.0 V GPS receiver

Reference	Description	Part Number - Manufacturer
R1, R2, R3	4.7 kΩ Resistor 0402 5% 0.1 W	RC0402JR-074K7L - Yageo Phycomp
U1	Voltage Regulator for GPS Receiver	See GPS Receiver Hardware Integration Manual

Table 20: Components for application circuit for u-blox 3.0 V GPS receiver

1.10 Audio

LEON-G100/G200 modules provide four analog and one digital audio interfaces:

- Two microphone inputs:
  - First microphone input can be used for direct connection of the electret condenser microphone of a handset. This input is used when the main uplink audio path is "Handset Microphone" (refer to u-blox 2G GSM/GPRS AT Commands Manual [2]; AT+USPM command: <main_uplink> parameter)
  - Second microphone input can be used for direct connection of the electret condenser microphone of a headset. This input is used when the main uplink audio path is "Headset Microphone" (refer to u-blox 2G GSM/GPRS AT Commands Manual [2]; AT+USPM command: <main_uplink> parameter)
- Two speaker outputs:
  - First speaker output is a single ended low power audio output that can be used to directly connect the receiver (earpiece) of a handset or a headset. This output is used when the main downlink audio path is "Normal earpiece" or "Mono headset" (refer to u-blox 2G GSM/GPRS AT Commands Manual [2]; AT+USPM command: <main_downlink> parameter). These two downlink path profiles use the same physical output but have different sets of audio parameters (Refer to u-blox 2G GSM/GPRS AT Commands Manual [2]: AT+USGC, AT+UDBF, AT+USTN commands)
  - Second speaker output is a differential high power audio output that can be used to directly connect a speaker or a loud speaker used for ring-tones or for speech in hands-free mode. This output is used when audio downlink path is "Loudspeaker" (refer to u-blox 2G GSM/GPRS AT Commands Manual [2]; AT+USPM command, <main_downlink> and <alert_sound> parameters)
- Headset detection input:
  - If enabled, causes the automatic switch of uplink audio path to "Headset Microphone" and downlink audio path to "Mono headset". Enabling/disabling the detection can be controlled by parameter <headset_indication> in AT+USPM command (refer to u-blox 2G GSM/GPRS AT Commands Manual [2])
- I^2S digital audio interface:
  - This path is selected when parameters <main_uplink> and <main_downlink> in AT+USPM command (refer to u-blox 2G GSM/GPRS AT Commands Manual [2]) are respectively "I^2S input line" and "I^2S output line"

☞ Not all combinations of Input-Output audio paths are allowed. Please check audio command AT+USPM in u-blox 2G GSM/GPRS AT Commands Manual [2] for allowed combinations of audio path and for their switching during different use cases (speech/alert tones).

☞ The default values for audio parameters tuning commands (Refer to u-blox 2G GSM/GPRS AT Commands Manual [2]; AT+UMGC, AT+UUBF, AT+UHFP, AT+USGC, AT+UDBF, AT+USTN commands) are tuned for audio device connected as suggested above (i.e. Handset microphone connected on first microphone input, headset microphone on second microphone input). For a different connection, (i.e. connection of a Hands Free microphone) these parameters should be changed on the audio path corresponding to the connection chosen.

1.10.1 Analog Audio interface

1.10.1.1 Uplink path (microphone inputs)

The TX (uplink) path of the analog audio front-end on the module consists of two identical microphone circuits. Two electret condenser microphones can be directly connected to the two available microphone inputs.

The main required electrical specifications for the electret condenser microphone are 2.2 kΩ as maximum output impedance at 1 kHz and 2 V maximum standard operating voltage.

Board-to-board pins related to the uplink path (microphones inputs) are:

- First microphone input:
  - **MIC_BIAS1**: single ended supply to the first microphone and represents the microphone signal input
  - **MIC_GND1**: local ground for the first microphone
- Second microphone input:
  - **MIC_BIAS2**: single ended supply to the second microphone and represents the microphone signal input
  - **MIC_GND2**: local ground for the second microphone

For a description of the internal function blocks see Figure 40.

1.10.1.2 Downlink path (speaker outputs)

The RX (downlink) path of the analog audio front-end of the module consists of two speaker outputs available on the following pins:

- First speaker output:
  - **HS_P**: low power single ended audio output. This pin is internally connected to the output of the single ended audio amplifier of the chipset
- Second speaker output:
  - **SPK_N/SPK_P**: high power differential audio output. These two pins are internally connected to the output of the high power differential audio amplifier of the chipset

See Figure 40 for a description of the internal function blocks.

Warning: excessive sound pressure from headphones can cause hearing loss.

Detailed electrical characteristics of the low power single-ended audio receive path and the high power differential audio receive path can be found in LEON-G100/G200 Data Sheet [1].

Table 21 lists the signals related to analog audio functions.

Name	Description	Remarks
HS_DET	Headset detection input	Internal active pull-up to 2.85 V enabled.
HS_P	First speaker output with low power single-ended analog audio	This audio output is used when audio downlink path is "Normal earpiece" or "Mono headset"
SPK_P	Second speaker output with high power differential analog audio	This audio output is used when audio downlink path is "Loudspeaker".
SPK_N	Second speaker output with power differential analog audio output	This audio output is used when audio downlink path is "Loudspeaker".
MIC_BIAS2	Second microphone analog signal input and bias output	This audio input is used when audio uplink path is set as "Headset Microphone". Single ended supply output and signal input for the second microphone.
MIC_GND2	Second microphone analog reference	Local ground of second microphone. Used for "Headset microphone" path.
MIC_GND1	First microphone analog reference	Local ground of the first microphone. Used for "Handset microphone" path
MIC_BIAS1	First microphone analog signal input and bias output	This audio input is used when audio uplink path is set as "Handset Microphone". Single ended supply output and signal input for first microphone.

Table 21: Analog Audio Signal Pins

All audio lines on an Application Board must be routed in pairs, be embedded in GND (have the ground lines as close as possible to the audio lines), and maintain distance from noisy lines such as VCC and from components such as switching regulators.

Audio pins ESD rating is 1 kV (contact discharge). A higher protection level could be required if the lines are externally accessible on the application board. A higher protection level can be achieved mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) on the lines connected to these pins if they are externally accessible on the application board.

If the audio pins are not used, they can be left floating on the application board.

1.10.1.3 Handset mode

Handset mode is the default audio operating mode of LEON-G100/G200 modules. In this mode the main uplink audio path is "Handset microphone", the main downlink audio path is "Normal earpiece" (refer to u-blox 2G GSM/GPRS AT Commands Manual [2]; AT+USPM command: <main_uplink>, <main_downlink> parameters).

- Handset microphone must be connected to inputs **MIC_BIAS1/MIC_GND1**
- Handset receiver must be connected to output **HS_P**

Figure 36 shows an example of an application circuit connecting a handset (with a 2.2 kΩ electret microphone and a 32 Ω receiver) to the LEON-G100/G200 modules. The following actions should be done on the application circuit:

- Mount a series capacitor on the **HS_P** line to decouple the bias
- Mount a 10 µF ceramic capacitor (e.g. Murata GRM188R60J106M) if connecting a 32 Ω receiver, or a load with greater impedance (such as a single ended analog input of a codec). Otherwise if a 16 Ω receiver is connected to the line, a ceramic capacitor with greater nominal capacitance must be used: a 22 µF series capacitor (e.g. Murata GRM21BR60J226M) is required
- Mount a 82 nH series inductor (e.g. Murata LQG15HS82NJ02) on each microphone line and a 27 pF bypass capacitor (e.g. Murata GRM1555C1H270J) on all audio lines to minimize RF coupling and TDMA noise

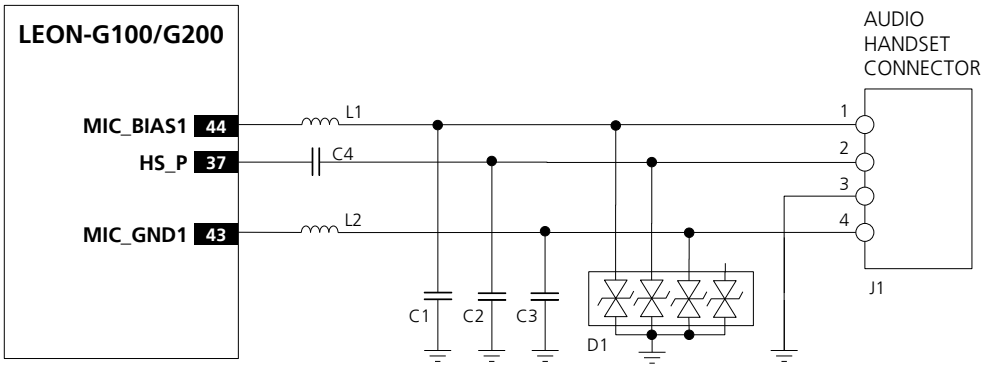

Figure 36: Handset connector application circuit

Reference	Description	Part Number - Manufacturer
C1, C2, C3	27 pF Capacitor Ceramic COG 0402 5% 25 V	GRM1555C1H270JZ01 - Murata
C4	10 µF Capacitor Ceramic X5R 0603 20% 6.3V	GRM188R60J106M - Murata
L1, L2	82 nH Multilayer inductor 0402 (self resonance frequency ~1 GHz)	LQG15HS82NJ02 - Murata
J1	Audio Handset Jack Connector, 4Ckt (4P4C)	52018-4416 - Molex
D1	Varistor Array for ESD protection	CA05P4S14THSG - EPCOS

Table 22: Example of components for handset connection

1.10.1.4 Headset mode

The audio path is automatically switched from handset mode to headset mode when a rising edge is detected by the module on **HS_DET** pin. The audio path returns to the handset mode when the line returns to low level.

In headset mode the main uplink audio path is "Headset microphone", the main downlink audio path is "Mono headset" (refer to u-blox 2G GSM/GPRS AT Commands Manual [2]; AT+USPM command: <main_uplink>, <main_downlink> parameters).

The audio path used in headset mode:

- Headset microphone must be connected to **MIC_BIAS2/MIC_GND2**
- Headset receiver must be connected to **HS_P**

Figure 37 shows an application circuit connecting a headset (with a 2.2 kΩ electret microphone and a 32 Ω receiver) to the LEON-G100/G200 modules. Pin 1 & 2 are shorted in the headset connector, causing **HS_DET** to be pulled low. When the headset plug is inserted **HS_DET** is pulled internally by the module, causing a rising edge for detection.

Perform the following steps on the application board (as shown in Figure 37; the list of components to be mounted is shown in Table 23):

- Mount a series capacitor on the **HS_P** line to decouple the bias. 10 µF ceramic capacitor (e.g. Murata GRM188R60J106M) is required if a 32 Ω receiver or a load with greater impedance (as a single ended analog input of a codec) is connected to the line. 22 µF series capacitor (e.g. Murata GRM21BR60J226M) is required if a 16 Ω receiver is connected to the line
- Mount a 82 nH series inductor (e.g. Murata LQG15HS82NJ02) on each microphone line, and a 27 pF bypass capacitor (e.g. Murata GRM1555C1H270J) on all audio lines to minimize RF coupling and the TDMA noise

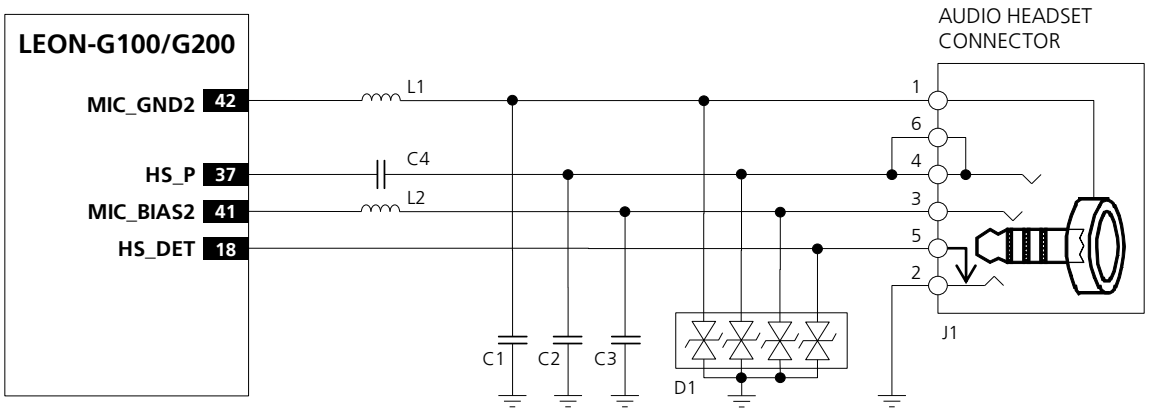

Figure 37: Headset mode application circuit

Reference	Description	Part Number - Manufacturer
C1, C2, C3	27 pF Capacitor Ceramic COG 0402 5% 25 V	GRM1555C1H270JZ01 - Murata
C4	10 µF Capacitor Ceramic X5R 0603 20% 6.3V	GRM188R60J106M - Murata
L1, L2	82nH Multilayer inductor 0402 (self resonance frequency ~1 GHz)	LQG15HS82NJ02 - Murata
J1	Audio Headset 2.5 mm Jack Connector	SJ1-42535TS-SMT - CUI, Inc.
D1	Varistor Array for ESD protection	CA05P4S14THSG - EPCOS

Table 23: Example of components for headset jack connection

1.10.1.5 Hands-free mode

Hands-free mode can be implemented using a loudspeaker and a dedicated microphone.

Hands-free functionality is implemented using appropriate DSP algorithms for voice-band handling (echo canceller and automatic gain control), managed via software (Refer to u-blox 2G GSM/GPRS AT Commands Manual [2]; AT+UHFP command).

In this mode the main downlink audio path must be "Loudspeaker", the main uplink audio path can be "Handset microphone" or "Headset microphone" (refer to u-blox 2G GSM/GPRS AT Commands Manual [2]; AT+USPM command: <main_uplink>, <main_downlink> parameters). Use of an uplink audio path for hands-free makes it unavailable for another device (handset/headset). Therefore:

- Microphone can be connected to the input pins **MIC_BIAS1/MIC_GND1** or **MIC_BIAS2/MIC_GND2**
- High power loudspeaker must be connected to the output pins **SPK_P/SPK_N**

☞ The default parameters for audio uplink profiles "Handset microphone" and "Headset microphone" (refer to u-blox 2G GSM/GPRS AT Commands Manual [2]; AT+UMGC, AT+UUBF, AT+UHFP) are for a handset and a headset microphone. To implement hands-free mode, these parameters should be changed on the audio path corresponding to the connection chosen. Procedure to tune parameters for hands-free mode (gains, echo canceller) can be found in LEON Audio Application Note [12].

When hands-free mode is enabled, the audio output signal on **HS_P** is disabled.

☞ The physical width of the high-power audio outputs lines on the application board must be wide enough to minimize series resistance.

Figure 38 shows an application circuit for hands-free mode. In this example the LEON-G100/G200 modules are connected to an 8 Ω speaker and a 2.2 kΩ electret microphone. Insert an 82 nH series inductor (e.g. Murata LQG15HS82NJ02) on each microphone line, and a 27 pF bypass capacitor (e.g. Murata GRM1555C1H270J) on all audio lines to minimize RF coupling and the TDMA noise.

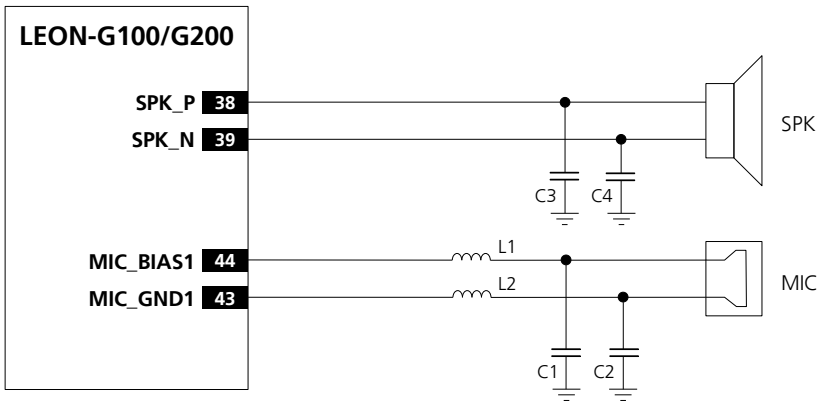

Figure 38: Hands free mode application circuit

Reference	Description	Part Number - Manufacturer
C1, C2, C3, C4	27 pF Capacitor Ceramic COG 0402 5% 25 V	GRM1555C1H270JZ01 - Murata
L1, L2	82nH Multilayer inductor 0402 (self resonance frequency ~1 GHz)	LQG15HS82NJ02 - Murata
SPK	Loudspeaker	
MIC	Active Elected Microphone	

Table 24: Example of components for hands-free connection

1.10.1.6 Connection to an external analog audio device

When the LEON-G100/G200 module analog audio output has to be connected to an external audio device, **HS_P** analog audio output can be used.

- A 10 µF series capacitor (e.g. Murata GRM188R60J106M) must be inserted between the **HS_P** output and the single ended analog input of the external audio device (to decouple the bias)
- An additional single ended to differential circuit is required for audio devices with a differential analog input. The signal levels can be adapted by setting gain using AT commands, but additional circuitry must be inserted if the **HS_P** output level of the module is too high for the input of the audio device

If LEON-G100/G200 module analog audio input has to be connected to an external audio device, **MIC_BIAS1**/ **MIC_GND1** can be used (default analog audio input of the module).

- Insert a 10 µF series capacitor (e.g. Murata GRM188R60J106M) between the single ended analog output of the external audio device and **MIC_BIAS1**
- Connect the reference of the single ended analog output of the external audio device to **MIC_GND1**. If the external audio device is provided with a differential analog output, insert an additional differential to single ended circuit. The signal levels can be adapted by setting gain using AT commands, but additional circuitry must be inserted if the output level of the audio device is too high for **MIC_BIAS1**

Examples of connecting LEON-G100/G200 modules to external audio applications are illustrated in the Figure 39 and Table 25.

To enable the audio path corresponding to these input/output, please refer to u-blox 2G GSM/GPRS AT Commands Manual [2], AT+USPM command.

To tune audio levels for the external device please refer to u-blox 2G GSM/GPRS AT Commands Manual [2], AT+USGC, AT+UMGC commands.

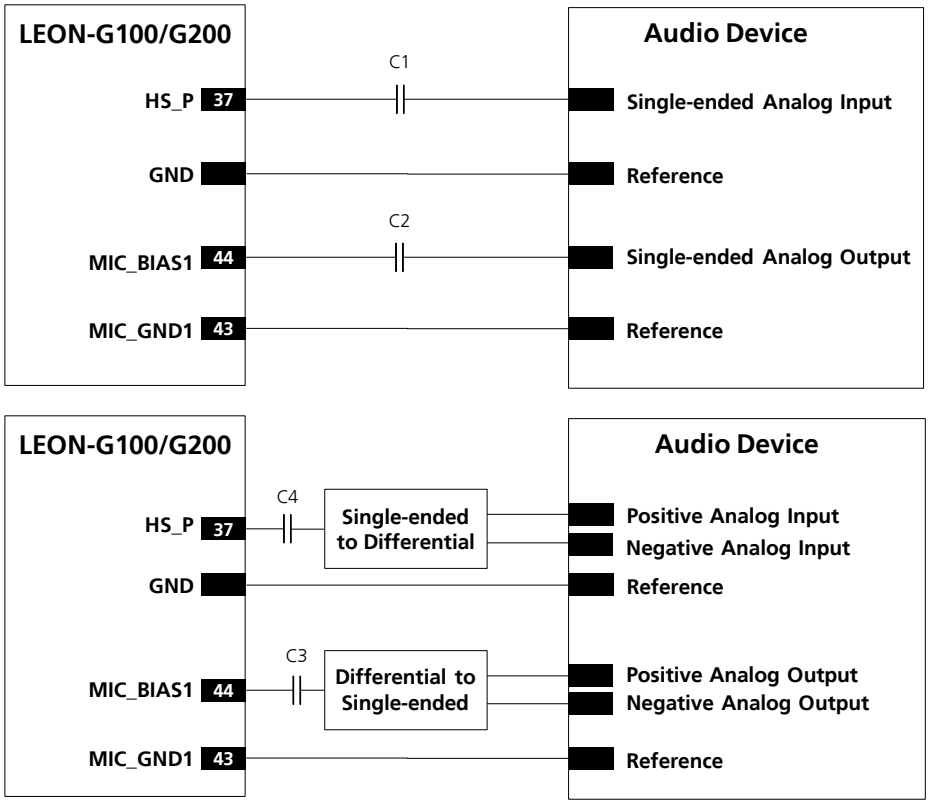

Figure 39: Application circuits to connect the LEON module to external audio devices with proper single-ended or differential analog audio inputs/outputs

Reference	Description	Part Number - Manufacturer
C1, C2, C3, C4	10 µF Capacitor X5R 0603 5% 6.3 V	GRM188R60J106M - Murata

Table 25: Example of components for the connection to an Audio Device

1.10.2 Digital Audio interface

LEON-G100/G200 support a bidirectional 4-wire I²S digital audio interface. The module acts as master only. The I²S pins are listed in Table 26:

Name	Description	Remarks
I2S_WA	I²S word alignment	Module output (master).[1]
I2S_TXD	I²S transmit data	Module output [1]
I2S_CLK	I²S clock	Module output (master) [1]
I2S_RXD	I²S receive data	Module input [1] Internal active pull-up to 2.85 V enabled.

Table 26: I²S interface pins

☞ I²S interface pins ESD rating is 1 kV (contact discharge). A higher protection level could be required if the lines are externally accessible on the application board. A higher protection level can be achieved mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) on the lines connected to these pins if they are externally accessible on the application board.

The I²S interface can be can be used in two modes:

- PCM mode: I2Sx
- Normal I²S mode: I2Sy

Beyond the supported transmission modality, the main difference between the PCM mode and the normal I²S mode is represented by the logical connection to the digital audio processing system integrated in the chipset firmware (see Figure 40):

- PCM mode provides complete audio processing functionality
- Normal I²S mode: digital filters, digital gains, side tone, some audio resources as tone generator, info tones (e.g. free tone, connection tone, low battery alarm), and ringer are not available

The I²S interface is activated and configured using AT commands, see the u-blox 2G GSM/GPRS AT Commands Manual [2] (AT+UI2S command).

If the I²S interface is used in PCM mode, digital path parameters can be configured and saved as the normal analog paths, using appropriate path index as described in the u-blox 2G GSM/GPRS AT Commands Manual [2]. Analog gain parameters of microphone and speakers are unused when digital path is selected.

☞ Any external signal connected to the digital audio interface must be tri-stated when the module is in power-down mode and must be tri-stated during the module power-on sequence (at least for 1500 ms after the start-up event). If the external signals connected to the digital audio interface cannot be tri-stated, insert a multi channel digital switch (e.g. Texas Instruments SN74CB3Q16244, TS5A3159, or TS5A63157) between the two-circuit connections and set to high impedance when the module is in power down mode and during the module power-on sequence.

☞ If the I²S pins are not used, they can be left floating on the application board.

[1] Check device specifications to ensure compatibility of supported modes to LEON-G100/G200 module. Add a test point to provide access to the pin for debugging.

☞ For debug purposes, include a test point at each I²S pin also if the digital audio interface is not used.

☞ Refer to u-blox 2G GSM/GPRS AT Commands Manual [2], AT+UI2S command for possible combinations of connection and settings.

1.10.2.1 PCM mode

In PCM mode **I2S_TX** and **I2S_RX** are respectively parallel to the analog front end **I2S_RX** and **I2S_TX** as internal connections to the voice processing system (see Figure 40), so resources available for analog path can be shared:

- Digital filters and digital gains are available in both uplink and downlink direction. They can be configured using AT commands; please refer to the u-blox 2G GSM/GPRS AT Commands Manual [2]
- Ringer tone and service tone are mixed on the TX path when active (downlink)
- The HF algorithm acts on I²S path

Main features of the I²S interface in PCM mode:

- I²S runs in PCM - short alignment mode (configurable with AT commands)
- Module functions as I²S master (**I2S_CLK** and **I2S_WA** signals generated by the module)
- **I2S_WA** signal always runs at 8 kHz
- **I2S_WA** toggles high for 1 or 2 CLK cycles of synchronism (configurable), then toggles low for 16 CLK cycles of sample width. Frame length can be 1 + 16 = 17 bits or 2 + 16 = 18 bits
- **I2S_CLK** frequency depends on frame length. Can be 17 x 8 kHz = 136 kHz or 18 x 8 kHz = 144 kHz
- **I2S_TX**, **I2S_RX** data are 16 bit words with 8 kHz sampling rate, mono. Data are in 2's complement notation. MSB is transmitted first
- When **I2S_WA** toggles high, first synchronization bit is always low. Second synchronism bit (present only in case of 2 bit long **I2S_WA** configuration) is MSB of the transmitted word (MSB is transmitted twice in this case)
- **I2S_TX** changes on **I2S_CLK** rising edge, **I2S_RX** changes on **I2S_CLK** falling edge

1.10.2.2 Normal I²S mode

Normal I²S mode supports:

- 16 bits word
- Mono interface
- 8 kHz frequency

Main features of I²S interface in Normal I²S mode:

- **I2S_WA** signal always runs at 8 kHz and the channel can be either high or low
- **I2S_TX** data 16 bit words with 32 bit frame and 2, dual mono (the word can be written on 2 channels). Data are in 2's complement notation. MSB is transmitted first. The MSB is first transmitted; the bits change on **I2S_CLK** rising or falling edge (configurable)
- **I2S_RX** data are read on the **I2S_CLK** edge opposite to **I2S_TX** writing edge
- **I2S_CLK** frequency depends by the number of bits and number of channels so is 16 x 2 x 8 kHz = 256 kHz

The modes are configurable through a specific AT command (refer to u-blox 2G GSM/GPRS AT Commands Manual [2]) and the following parameters can be set:

- **I2S_TX** word can be written while **I2S_WA** is high, low or both
- MSB can be 1 bit delayed or non-delayed on **I2S_WA** edge
- **I2S_TX** data can change on rising or falling edge of **I2S_CLK** signal
- **I2S_RX** data read on the opposite front of **I2S_CLK** signal

1.10.3 Voice-band processing system

The digital voice-band processing on the LEON-G100/G200 is implemented in the DSP core inside the baseband chipset. The analog audio front-end of the chipset is connected to the digital system through 16 bit ADC converters in the uplink path, and through 16 bit DAC converters in the downlink path. The digitized TX and RX voice-band signals are both processed by digital gain stages and decimation filter in TX, interpolation filters in RX path. The processed digital signals of TX and RX are connected to the DSP for various tasks (i.e. speech codec, digital mixing and sidetone, audio filtering) implemented in the firmware modules.

External digital audio devices can be interfaced to the DSP voice-band processing system via the I^2S interface.

The voice-band processing system can be split up into three different blocks:

- Sample-based Voice-band Processing (single sample processed at 8 kHz, every 125 µs)
- Frame-based Voice-band Processing (frames of 160 samples are processed every 20 ms)
- MIDI synthesizer running at 47.6 kHz

These three blocks are connected by buffers and sample rate converters (for 8 to 47.6 kHz conversion)

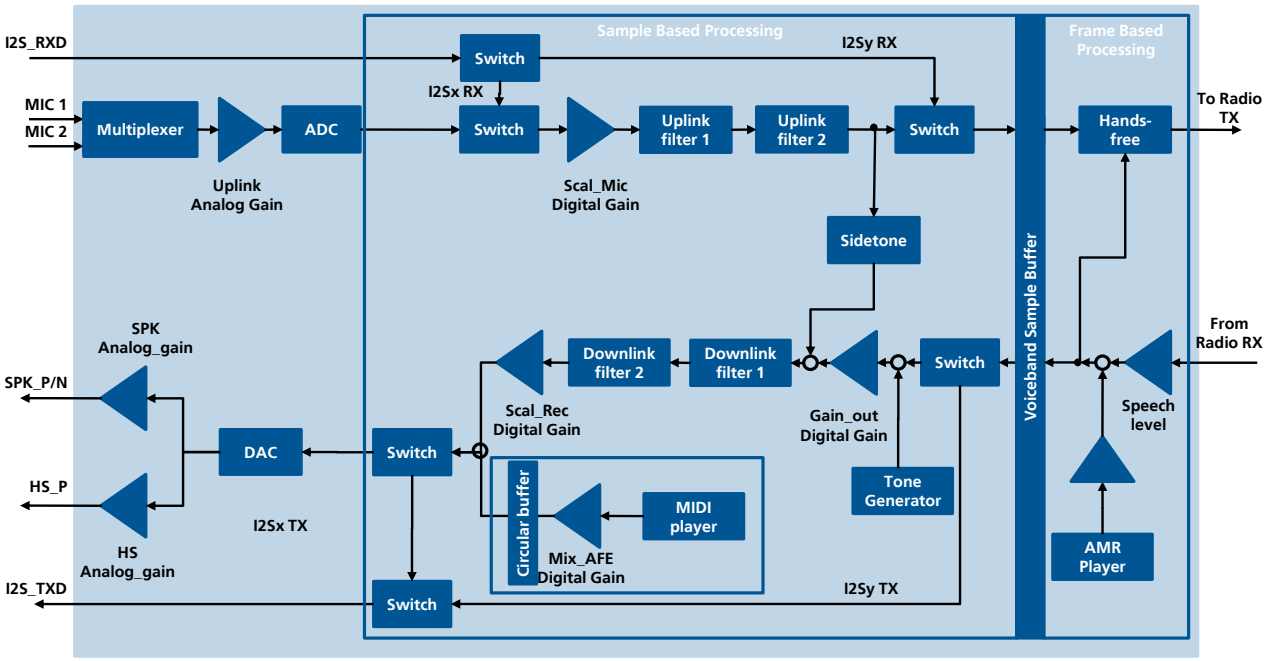

Figure 40: LEON-G100/G200 voice-band processing system block diagram

The sample-based voice-band processing main task is to transfer the voice-band samples from either analog audio front-end TX path or I2Sx RX path to the Voice-band Sample Buffer and from the Voice-band Sample Buffer to the analog audio front-end RX path and/or I2Sx TX path.

While doing this the samples are scaled by digital gains and processed by digital filters both in the uplink and downlink direction. The sidetone is generated mixing scaled uplink samples to the downlink samples. The frame-based voice-band processing implements the Hands Free algorithm. This consists of the Echo Canceller, the Automatic Gain Control and the Noise Suppressor. Hands Free algorithm acts on the uplink signal only. The frame-based voice-band processing also implements an AMR player (according to RFC3267 standard). AMR player supported data rates are: 12.2 – 10.2 – 7.95 – 7.40 – 6.70 – 5.90 – 5.15 – 4.75 kbps. The speech uplink path final block before radio transmission is the speech encoder. Symmetrically, on downlink path, the starting block is the speech decoder which extracts speech signal from the radio receiver.

The circular buffer is a 3000 word buffer to store and mix the voice-band samples from Midi synthesizer. The buffer has a circular structure, so that when the write pointer reaches the end of the buffer, it is wrapped to the begin address of the buffer.

Two different sample-based sample rate converters are used: an interpolator, required to convert the sample-based voice-band processing sampling rate of 8 kHz to the analog audio front-end output rate of 47.6 kHz; a decimator, required to convert the circular buffer sampling rate of 47.6 kHz to the I2Sx TX or the uplink path sample rate of 8 kHz.

1.10.3.1 Audio codecs

The following speech codecs are supported by firmware on the DSP:

- GSM Half Rate (TCH/HS)
- GSM Full Rate (TCH/FS)
- GSM Enhanced Full Rate (TCH/EFR)
- 3GPP Adaptive Multi Rate (AMR) (TCH/AFS+TCH/AHS)

1.10.3.2 Echo cancelation and noise reduction

LEON-G100/G200 support algorithms for echo cancellation, noise suppression and automatic gain control. Algorithms are configurable with AT commands (refer to the u-blox 2G GSM/GPRS AT Commands Manual [2]).

1.10.3.3 Digital filters and gains

Audio parameters such as digital filters, digital gain, Side-tone gain (feedback from uplink to downlink path) and analog gain are available for uplink and downlink audio paths. These parameters can be modified by dedicated AT commands and be saved in 2 customer profiles in the non-volatile memory of the module (refer to the u-blox 2G GSM/GPRS AT Commands Manual [2]).

1.10.3.4 Ringer mode

LEON-G100/G200 modules support polyphonic ring tones. The ringer tones are generated by a built-in generator on the chipset and then amplified by the internal amplifier.

The synthesizer output is only mono and cannot be mixed with TCH voice path (the two are mutually exclusive). To perform in-band alerting during TCH with voice path open, only Tone Generator can be used.

The analog audio path used in ringer mode can be the high power differential audio output (refer to u-blox 2G GSM/GPRS AT Commands Manual [2]; AT+USPM command, <main_downlink> and <alert_sound> parameters for alert sounds routing). In this case the external high power loudspeaker must be connected to the SPK_P/SPK_N output pins of the module as shown in the application circuit (Figure 38) described in section 1.10.1.5.

1.11 ADC input (LEON-G100 only)

One Analog to Digital Converter input is available (**ADC1**) and is configurable using u-blox AT command (see u-blox 2G GSM/GPRS AT Commands Manual [2]). The resolution of this converter is 12-bit with a single ended input range.

Name	Description	Remarks
ADC1	ADC input	Resolution: 12 bits.

Table 27: ADC pin

☞ **ADC1** pin ESD rating is 1 kV (contact discharge). A higher protection level could be required if the line is externally accessible on the application board. A higher protection level can be achieved mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) on the line connected to this pin if it is externally accessible on the application board.

☞ If the **ADC1** pin is not used, it can be left floating on the application board.

The electrical behavior of the measurement circuit in voltage mode can be modeled by a circuit equivalent to that shown in Figure 41. This includes a resistor (R_{eq}), voltage source (U_{eq}), analog preamplifier (with typical gain G=0.5), and a digital amplifier (with typical gain g_{ADC}=2048 LSB/V).

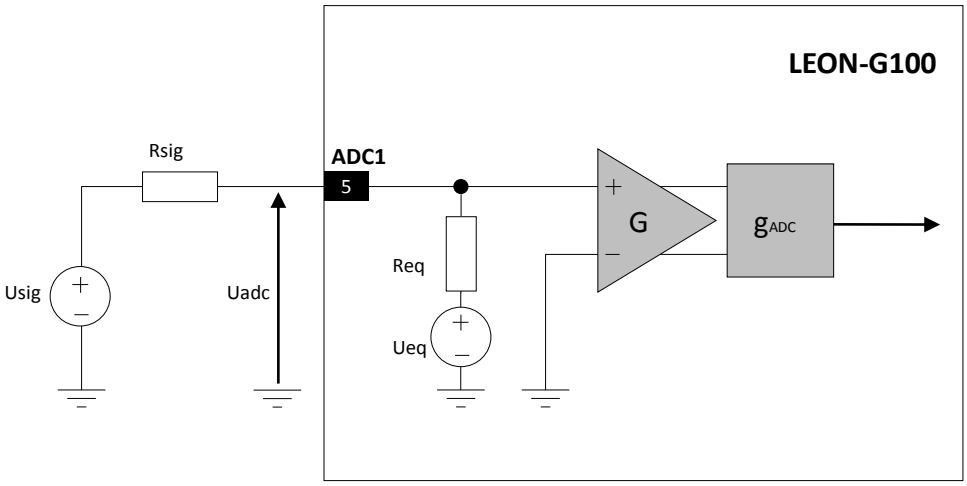

Figure 41: Equivalent network for ADC single-ended measurement

The ADC software driver takes care of the parameters shown in Figure 41 (R_{eq}, U_{eq}, G, g_{ADC}): the voltage measured by **ADC1** is U_{adc} and its value expressed in mV is given by the AT+UADC=0 response (for more details on the AT command please refer to u-blox 2G GSM/GPRS AT Commands Manual [2]).

The detailed electrical specifications of the Analog to Digital Converter input (Input voltage span, Input resistance in measurement mode R_{eq}, Internal voltage U_{eq}): are reported in the LEON-G100/G200 Data Sheet [1].

As described in the ADC equivalent network shown in Figure 41, one part of the whole ADC circuit is outside the module: the (U_{sig}) and the (R_{sig}) are characteristics of the application board because they represent the Thévenin's equivalent of the electrical network developed on the application board.

☞ If an external voltage divider is implemented to increase the voltage range, check the input resistance in measurement mode (R_{eq}) of **ADC1** input and all the electrical characteristics.

If the Thévenin's equivalent of the voltage source (U_{sig}) has a significant internal resistance (R_{sig}) compared to the input resistance in measurement mode (R_{eq}) of the ADC, this should be taken into account and corrected to properly associate the AT+UADC=0 response to the voltage source value, implementing the ADC calibration procedure suggested in the section 1.11.1 below.

If the customer implements the calibration procedure on the developed application board, the influence of the internal series resistance (R_{sig}) of the voltage source (U_{sig}) is taken into account in the measurement: the AT+UADC=0 response can be correctly associated to the value of the voltage source applied on the application board.

1.11.1 ADC Calibration

To improve the absolute accuracy of the 12-bit analog-to-digital converter (ADC), it is suggested to follow the calibration procedure here described.

The calibration aim is to evaluate the relationship between the value, expressed in mV, of the voltage source (V_S, which Thévenin's equivalent is represented by U_{sig} and R_{sig} shown in Figure 41) that has to be measured and the AT+UADC=0 response (ADC_VALUE, that is the U_{adc} value expressed in mV) when V_S is applied, calculating the calibration GAIN and OFFSET parameters value.

Calibration is performed providing two known reference values (V_1 and V_2) instead of the voltage source (V_S) that has to be measured by the ADC.

V_1 and V_2 values should be as different as possible: taking into account of the ADC applicable range, the maximum limit and the minimum limit for the voltage source has to be applied to obtain the best accuracy in calibration.

The following values are involved in the calibration procedure:

- V_1: the first (e.g. maximum) reference known voltage in mV applied in the calibration procedure
- V_2: the second (e.g. minimum) applied reference known voltage in mV applied in the calibration procedure
- ADC_1: the AT+UADC=0 response when V_1 is applied
- ADC_2: the AT+UADC=0 response when V_2 is applied

This is the procedure to calibrate the ADC:

1. Apply V_1
2. Read ADC_1
3. Apply V_2
4. Read ADC_2
5. Evaluate GAIN value with the following formula:

$$GAIN = 16384 * \frac{(V\_1 - V\_2)}{(ADC\_1 - ADC\_2)}$$

6. Evaluate OFFSET value with the following formula:

$$OFFSET = \frac{(V\_2 * ADC\_1 - V\_1 * ADC\_2)}{(V\_1 - V\_2)} + \frac{8192}{GAIN}$$

Now the voltage source (V_S) value expressed in mV can be exactly evaluated from the AT+UADC=0 response (ADC_VALUE) when V_S is applied, with the following formula:

$$V\_S = \frac{(ADC\_VALUE + OFFSET) * GAIN - 8192}{16384}$$

where the parameters are defined as following:

- V_S is the voltage source value expressed in mV
- ADC_VALUE is the AT+UADC=0 response when V_S is applied
- GAIN is calculated in the calibration procedure (see point 5)
- OFFSET is calculated in the calibration procedure (see point 6)

1.12 General Purpose Input/Output (GPIO)

LEON-G100/G200 modules provide two General Purpose Input/Output pins (**GPIO1**, **GPIO2**) which can be configured via u-blox AT commands (more details available in u-blox 2G GSM/GPRS AT Commands Manual [2], AT+UGPIOC, AT+UGPIOR, AT+UGPIOW).

Name	Description	Remarks
GPIO1	GPIO	Add a test point to provide access to the pin for debugging.
GPIO2	GPIO	Dedicated for connection to a u-blox GPS receiver

Table 28: GPIO pins

☞ **GPIO1** and **GPIO2** pins ESD rating is 1 kV (contact discharge). A higher protection level could be required if the lines are externally accessible on the application board. A higher protection level can be achieved mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) on the lines connected to these pins if they are externally accessible on the application board.

GPIO2 is dedicated for connection to a u-blox GPS receiver: **GPIO2** is driven as output by the +UGPS AT command to switch-on or switch-off the u-blox GPS receiver.

If LEON-G100/G200 module is connected to a u-blox GPS receiver by the DDC (I^2C) interface, **GPIO2** must be connected to the active-high enable pin (or the active-low shutdown pin) of the voltage regulator that supplies the u-blox GPS receiver on the application board.

If LEON-G100/G200 module is not connected to a u-blox GPS receiver by the DDC (I^2C) interface, **GPIO2** can be used for general purposes.

☞ To avoid an increase of module power consumption any external signal connected to a GPIO must be set low or tri-stated when the module is in power-down mode. If the external signals in the application circuit connected to a GPIO cannot be set low or tri-stated, mount a multi channel digital switch (e.g. Texas Instruments SN74CB3Q16244) or a single channel analog switch (e.g. Texas Instruments TS5A3159 or TS5A63157) between the two-circuit connections and set to high impedance.

☞ If the **GPIO1** and **GPIO2** pins are not used, they can be left floating on the application board.

☞ For debug purposes, add a test point on the **GPIO1** pin even if this GPIO is not used.

1.13 M2M Setup Schematic Example

Figure 42 is an example of a schematic diagram where the LEON-G200 module is integrated into an application board, using all the interfaces of the module.

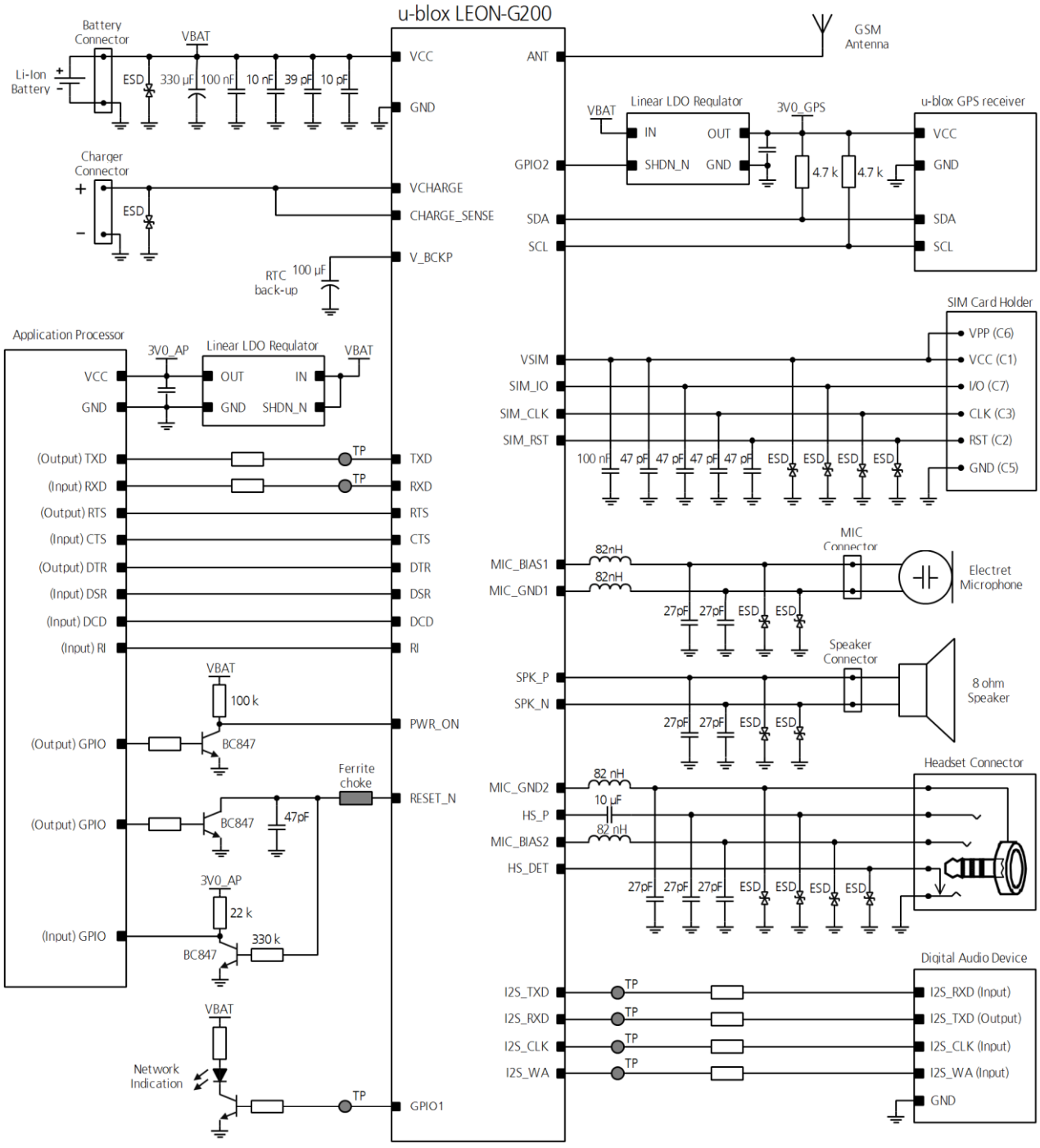

Figure 42: Example of schematic diagram to integrate LEON-G200 module in an application board, using all the interfaces

1.14 Approvals

1.14.1 Compliance with FCC and IC Rules and Regulations

LEON-G100/G200 modules are approved by the following regulatory bodies:

- **European Conformance CE mark**: EC identification number 0682
- **R&TTED** (Radio and Telecommunications Terminal Equipment Directive)
- **PTCRB** (PCS Type Certification Review Board)
- **GCF** (Global Certification Forum), partial compliance
- **AT&T** network compatibility
- **CMIIT** (China Ministry of Information Industry); **SRRC** (State Radio Regulation Center); Approval Code:
  - LEON-G100: CMIIT ID: 2010CJ0053
  - LEON-G200: CMIIT ID: 2010CJ0054
- **FCC** (Federal Communications Commission) Identifier:
  - LEON-G100: XPYLEONG100
  - LEON-G200: XPYLEONG200
- **GOST-R**, **Hygienic**, **DoC**

Radiofrequency radiation exposure Information: this equipment complies with FCC radiation exposure limits prescribed for an uncontrolled environment. This equipment should be installed and operated with a minimum distance of 20 cm between the radiator and your body. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

- **IC** (Industry Canada) Certification Number:
  - LEON-G100: 8595A-LEONG100
  - LEON-G200: 8595A-LEONG200

Manufacturers of mobile or fixed devices incorporating LEON-G100 / LEON-G200 modules are authorized to use the FCC Grants and Industry Canada Certificates of the LEON-G100 / LEON-G200 modules for their own final products according to the conditions referenced in the certificates.

The FCC Label shall in the above case be visible from the outside, or the host device shall bear a second label stating:
"Contains FCC ID: XPYLEONG100" resp. "Contains FCC ID XPYLEONG200".

IMPORTANT: Manufacturers of portable applications incorporating LEON-G100 / LEON-G200 modules are required to have their final product certified and apply for their own FCC Grant and Industry Canada Certificate related to the specific portable device. This is mandatory to meet the SAR requirements for portable devices.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

- **ICASA** (Independent Communications Authority of South Africa)

- **ANATEL** (Brazilian Agency of Telecommunications, in Portuguese, Agência Nacional de Telecomunicações)

2 Design-In

2.1 Design-in checklist

This section provides a design-in checklist.

2.1.1 Schematic checklist

The following are the most important points for a simple schematic check:

- ☑ DC supply must provide a nominal voltage at **VCC** pin above the minimum normal operating range limit.
- ☑ DC supply must be capable to provide 2.5 A current bursts with maximum 400 mV voltage drop at **VCC** pin.
- ☑ **VCC** supply should be clean, with very low ripple/noise: suggested passive filtering parts can be inserted.
- ☑ Connect only one DC supply to **VCC**: different DC supply systems are mutually exclusive.
- ☑ **V_CHARGE** and **CHARGE_SENSE** must be externally shorted (LEON-G200 only).
- ☑ The DC supply used as charger must be voltage and current limited as specified (LEON-G200 only).
- ☑ Do no leave **PWR_ON** floating: add a pull-up resistor to a proper supply (i.e. **V_BCKP** or **VCC**).
- ☑ Check that voltage level of any connected pin does not exceed the relative operating range.
- ☑ Capacitance and series resistance must be limited on each SIM signal to match the SIM specifications.
- ☑ Insert the suggested low capacitance ESD protection and passive filtering parts on each SIM signal.
- ☑ Check UART signals direction, since the signal names follow the ITU-T V.24 Recommendation [4].
- ☑ Add a proper pull-up resistor to a proper supply on each DDC (I^2C) interface line, if the interface is used.
- ☑ Capacitance and series resistance must be limited on each line of the DDC interface.
- ☑ Insert the suggested passive filtering parts on each used analog audio line.
- ☑ Check the digital audio interface specifications to connect a proper device.
- ☑ For debug purposes, add a test point on each I^2S pin and on **GPIO1** also if they are not used.
- ☑ To avoid an increase of module current consumption in power down mode, any external signals connected to the module digital pins (UART interface, **HS_DET**, GPIOs) must be set low or tri-stated when the module is in power down mode.
- ☑ Any external signal connected to the digital audio interface must be tri-stated when the module is in power down mode and must be tri-stated during the module power-on sequence (at least for 1500 ms after the start-up event).
- ☑ Provide proper precautions for ESD immunity as required on the application board.
- ☑ All the not used pins can be left floating on the application board.

2.1.2 Layout checklist

The following are the most important points for a simple layout check:

- ☑ Check 50 Ω impedance of **ANT** line.
- ☑ Follow the recommendations of the antenna producer for correct antenna installation and deployment.
- ☑ Ensure no coupling occurs with other noisy or sensitive signals.
- ☑ **VCC** line should be wide and short.
- ☑ Route **VCC** supply line away from sensitive analog signals.
- ☑ Avoid coupling of any noisy signals to microphone inputs lines.
- ☑ Ensure proper grounding.
- ☑ Consider "No-routing" areas for the Data Module footprint.

☑ Optimize placement for minimum length of RF line and closer path from DC source for **VCC**.

2.1.3 Antenna checklist

☑ Antenna should have 50 Ω impedance, V.S.W.R less then 3:1, recommended 2:1 on operating bands in deployment geographical area.

☑ Antenna should have built in DC resistor to ground to get proper Antenna detection functionality.

2.2 Design Guidelines for Layout

The following design guidelines must be met for optimal integration of LEON-G100/G200 modules on the final application board.

2.2.1 Layout guidelines per pin function

This section groups the LEON-G100/G200 pins by signal function and provides a ranking of importance in layout design.

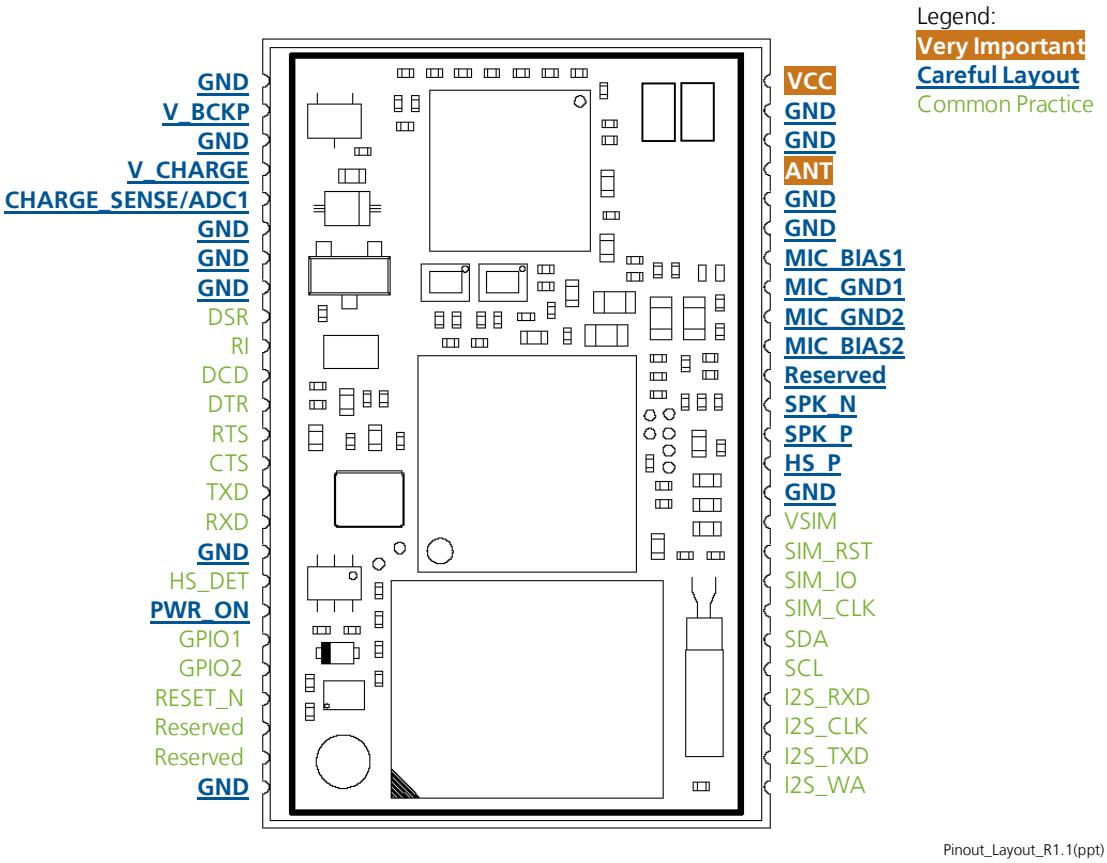

Figure 43: Module pin-out with highlighted functions

Rank	Function	Pin(s)	Layout	Remarks
1st	**RF Antenna In/out**	**ANT**	**Very Important**	Design for 50 Ω characteristic impedance. See section 2.2.1.1
2nd	**DC Supply**	**VCC**	**Very Important**	**VCC** line should be wide and short. Route away from sensitive analog signals. See section 2.2.1.2
3rd	**Analog Audio**		**Careful Layout**	Avoid coupling with noisy signals. See section 2.2.1.3
	Audio Inputs	**MIC_BIAS1, MIC_GND1, MIC_BIAS2, MIC_GND2**		
	Audio Outputs	**SPK_P, SPK_N, HS_P**		
4th	**Ground**	**GND**	**Careful Layout**	Provide proper grounding. See section 2.2.1.4
5th	**Charger**	**V_CHARGE, CHARGE_SENSE**	**Careful Layout**	Check Charger line width. See section 2.2.1.5
6th	**Sensitive Pin:**		**Careful Layout**	Avoid coupling with noisy signals. See section 2.2.1.6
	Backup Voltage	**V_BCKP**		
	A to D Converter (If implemented)	**ADC1**		
	Power On	**PWR_ON**		
7th	**Digital pins:**		Common Practice	Follow common practice rules for digital pin routing See section 2.2.1.7
	SIM Card Interface	VSIM, SIM_CLK, SIM_IO, SIM_RST		
	Digital Audio	I2S_CLK, I2S_RXD, I2S_TXD, I2S_WA		
	DDC	SCL, SDA		
	UART	TXD, RXD, CTS, RTS, DSR, RI, DCD, DTR		
	External Reset	RESET_N		
	General Purpose I/O	GPIO1, GPIO2		

Table 29: Pin list in order of decreasing importance for layout design

2.2.1.1 RF Antenna connection

The RF antenna connection pin **ANT** is very critical in layout design. The PCB line must be designed to provide 50 Ω characteristic impedance and minimum loss up to radiating element.

- Provide proper transition between the **ANT** pad to application board PCB
- Increase GND keep-out (i.e. clearance) for **ANT** pin to at least 250 µm up to adjacent pads metal definition and up to 500 µm on the area below the Data Module, as described in Figure 44
- Add GND keep-out (i.e. clearance) on buried metal layers below **ANT** pad and below any other pad of component present on the RF line, if top-layer to buried layer dielectric thickness is below 200 µm, to reduce parasitic capacitance to ground (see Figure 44 for the description keep-out area below **ANT** pad)
- The transmission line up to antenna connector or pad may be a micro strip or a stripline. In any case must be designed to achieve 50 Ω characteristic impedance
- Microstrip lines are usually easier to implement and the reduced number of layer transitions up to antenna connector simplifies the design and diminishes reflection losses. However, the electromagnetic field extends to the free air interface above the stripline and may interact with other circuitry
- Buried stripline exhibits better shielding to incoming and generated interferences. Therefore are preferred for sensitive application. In case a stripline is implemented, carefully check that the via pad-stack does not couple with other signals on the crossed and adjacent layers
- Minimize the transmission line length; the insertion loss should be minimized as much as possible, in the order of a few tenths of a dB
- The transmission line should not have abrupt change to thickness and spacing to GND, but must be uniform and routed as smoothly as possible

- The transmission line must be routed in a section of the PCB where minimal interference from noise sources can be expected
- Route **ANT** line far from other sensitive circuits as it is a source of electromagnetic interference
- Avoid coupling with **VCC** routing and analog audio lines
- Ensure solid metal connection of the adjacent metal layer on the PCB stack-up to main ground layer
- Add GND vias around transmission line
- Ensure no other signals are routed parallel to transmission line, or that other signals cross on adjacent metal layer
- If the distance between the transmission line and the adjacent GND area (on the same layer) does not exceed 5 times the track width of the micro strip, use the "Coplanar Waveguide" model for 50 Ω characteristic impedance calculation
- Don't route microstrip line below discrete component or other mechanics placed on top layer
- When terminating transmission line on antenna connector (or antenna pad) it is very important to strictly follow the connector manufacturer's recommended layout
- GND layer under RF connectors and close to buried vias should be cut out in order to remove stray capacitance and thus keep the RF line 50 Ω. In most cases the large active pad of the integrated antenna or antenna connector needs to have a GND keep-out (i.e. clearance) at least on first inner layer to reduce parasitic capacitance to ground. Note that the layout recommendation is not always available from connector manufacturer: e.g. the classical SMA Pin-Through-Hole needs to have GND cleared on all the layers around the central pin up to annular pads of the four GND posts. Check 50 Ω impedance of **ANT** line

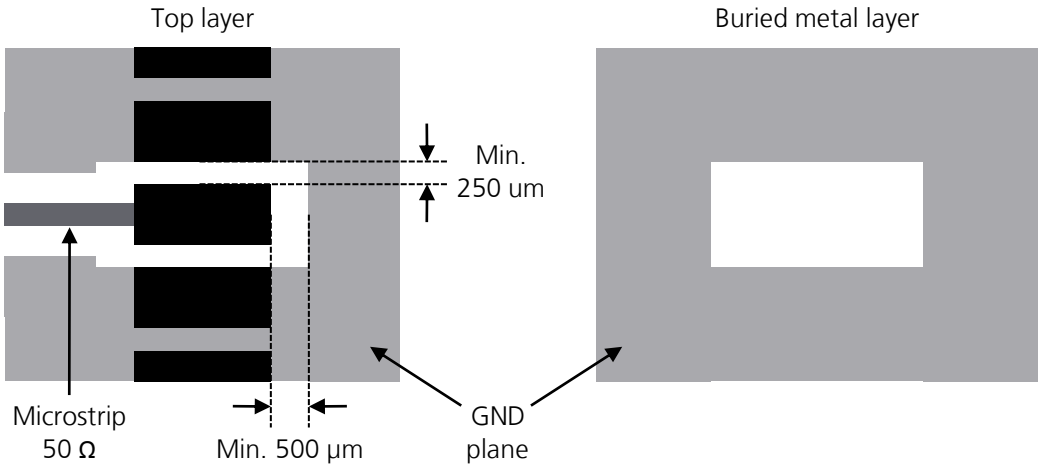

Figure 44: GND keep-out area on the top layer around the ANT pad and on the buried metal layer below the ANT pad

☞ Any RF transmission line on PCB should be designed for 50 Ω characteristic impedance.

☞ Ensure no coupling occurs with other noisy or sensitive signals.

2.2.1.2 Main DC supply connection

The DC supply of LEON-G100/G200 modules is very important for the overall performance and functionality of the integrated product. For detailed description check the design guidelines in section 1.5.2. Some main characteristics are:

- **VCC** connection may carry a maximum burst current in the order of 2.5 A. Therefore, it is typically implemented as a wide PCB line with short routing from DC supply (DC-DC regulator, battery pack, etc)
- The module automatically initiates an emergency shutdown if supply voltage drops below hardware threshold. In addition, reduced supply voltage can set a worst case operation point for RF circuitry that may behave incorrectly. It follows that each voltage drop in the DC supply track will restrict the operating margin at the main DC source output. Therefore, the PCB connection has to exhibit a minimum or zero voltage drop. Avoid any series component with Equivalent Series Resistance (ESR) greater than a few mΩ
- Given the large burst current, **VCC** line is a source of disturbance for other signals. Therefore route **VCC** through a PCB area separated from sensitive analog signals. Typically it is good practice to interpose at least one layer of PCB ground between **VCC** track and other signal routing
- The **VCC** supply current supply flows back to main DC source through GND as ground current: provide adequate return path with suitable uninterrupted ground plane to main DC source
- A tank capacitor with low ESR is often used to smooth current spikes. This is most effective when placed as close as possible to **VCC**. From main DC source, first connect the capacitor and then **VCC**. If the main DC source is a switching DC-DC converter, place the large capacitor close to the DC-DC output and minimize the **VCC** track length. Otherwise consider using separate capacitors for DC-DC converter and LEON-G100/G200 tank capacitor. Note that the capacitor voltage rating may be adequate to withstand the charger over-voltage if battery-pack is used
- **VCC** is directly connected to the RF power amplifier. Add capacitor in the pF range from **VCC** to GND along the supply path
- Since **VCC** is directly connected to RF Power Amplifier, voltage ripple at high frequency may result in unwanted spurious modulation of transmitter RF signal. This is especially seen with switching DC-DC converters, in which case it is better to select the highest operating frequency for the switcher and add a large L-C filter before connecting to LEON-G100/G200 in the worst case
- The large current generates a magnetic field that is not well isolated by PCB ground layers and which may interact with other analog modules (e.g. **VCO**) even if placed on opposite side of PCB. In this case route **VCC** away from other sensitive functional units
- The typical GSM burst has a periodic nature of approx. 217 Hz, which lies in the audible audio range. Avoid coupling between **VCC** and audio lines (especially microphone inputs)
- If **VCC** is protected by transient voltage suppressor / reverse polarity protection diode to ensure that the voltage maximum ratings are not exceeded, place the protecting device along the path from the DC source toward LEON-G100/G200, preferably closer to the DC source (otherwise functionality may be compromised)
- **VCC** pad is longer than other pads, and requires a "No-Routing" area for any other signals on the top layer of the application board PCB, below the LEON-G100/G200

☞ **VCC** line should be wide and short.

☞ Route away from sensitive analog signals.

2.2.1.3 Analog Audio

Accurate analog audio design is very important to obtain clear and high quality audio. The GSM signal burst has a repetition rate of 271 Hz that lies in the audible range. A careful layout is required to reduce the risk of noise pickup from audio lines due to both **VCC** burst noise coupling and RF detection.

Analog audio is separated in the two paths:

1. Audio Input (uplink path): **MIC_BIASx**, **MIC_GNDx**
2. Audio Outputs (downlink path): **SPK_P** / **SPK_N**, **HS_P**

The most sensitive is the uplink path, since the analog input signals are in the µV range. The two microphone inputs have the same electrical characteristics, and it is recommended to implement their layout with the same routing rules.

- Avoid coupling of any noisy signals to microphone inputs lines
- It is strongly recommended to route MIC signals away from battery and RF antenna lines. Try to skip fast switching digital lines as well
- Keep ground separation from other noisy signals. Use an intermediate GND layer or vias wall for coplanar signals
- **MIC_BIAS** and **MIC_GND** carry also the bias for external electret active microphone. Verify that microphone is connected with right polarity, i.e. **MIC_BIAS** to the pin marked "+" and **MIC_GND** (zero Volt) to the chassis of the device
- Despite different DC level, **MIC_BIAS** and **MIC_GND** are sensed differentially within the module. Therefore they should be routed as a differential pair of **MIC_BIAS** up to the active microphone
- Route **MIC_GND** with dedicated line together with **MIC_BIAS** up to active microphone. Note that **MIC_GND** is grounded internally within module and does not need external connection to GND
- Cross other signals lines on adjacent layers with 90° crossing
- Place bypass capacitor for RF very close to active microphone. The preferred microphone should be designed for GSM applications which typically have internal built-in bypass capacitor for RF very close to active device. If the integrated FET detects the RF burst, the resulting DC level will be in the pass-band of the audio circuitry and cannot be filtered by any other device
- If DC decoupling is required, consider that the input impedance of microphone lines is in the kΩ range. Therefore, series capacitors with sufficiently large value to reduce the high-pass cut-off frequency of the equivalent high-pass RC filter

Output audio lines have two separated configurations.

- **SPK_P** / **SPK_N** are high level balanced output. They are DC coupled and must be used with a speaker connected in bridge configuration
- Route **SPK_P** / **SPK_N** as differential pair, to reduce differential noise pick-up. The balanced configuration will help reject the common mode noise
- If audio output is directly connected to speaker transducer, given the low load impedance of its load, then consider enlarging PCB lines to reduce series resistive losses
- **HS_P** is single ended analog audio referenced to GND. Reduce coupling with noisy lines as this Audio output line does not benefit from common mode noise rejection of **SPK_P** / **SPK_N**
- Use twisted pair cable for balanced audio usage, shielded cable for unbalanced connection to speaker
- If DC decoupling is required, a large capacitor needs to be used, typically in the µF range, depending on the load impedance, in order not to increase the lower cut-off frequency due to its High-Pass RC filter response

2.2.1.4 Module grounding

Good connection of the module with application board solid ground layer is required for correct RF performance. It significantly reduces EMC issues and provides a thermal heat sink for the module.

- Connect each **GND** pin with application board solid GND layer. It is strongly recommended that each **GND** pad surrounding **VCC** and **ANT** pins have one or more dedicated via down to application board solid ground layer. The same applies to **GND** pins on the opposite side close to charger pins
- If the application board is a multilayer PCB, then it is required to tight together each GND area with complete via stack down to main board ground layer
- It is recommended to implement one layer of the application board as ground plane
- Good grounding of **GND** pads will also ensure thermal heat sink. This is critical during call connection, when the real network commands the module to transmit at maximum power: proper grounding helps prevent module overheating

2.2.1.5 Charger Layout (for LEON-G200 only)

If battery charger is implemented, **V_CHARGE** must withstand the charge current (typically in the order of several hundred mA) continuous current sink. Voltage drop is not as critical as for **VCC**, but dimension the line width adequately to support the charge current without excessive loss that may lead to increase in PCB temperature.

CHARGE_SENSE senses the charger voltage: it sinks a few µA. Therefore its line width is not critical. Since it is an analog input, it must be connected to **V_CHARGE** away from noisy sources.

2.2.1.6 Other Sensitive pins

A few other pins on the LEON-G100/G200 require careful layout.

- **Backup battery (V_BCKP)**: avoid injecting noise on this voltage domain as it may affect the stability of sleep oscillator
- **Analog-to-Digital Converter (ADC1)**: it is a high impedance analog input; the conversion accuracy will be degraded if noise injected. Low-pass filter may be used to improve noise rejection; typically L-C tuned for RF rejection gives better results
- **Power On (PWR_ON)**: is the digital input for power-on of the LEON-G100/G200. It is implemented as high impedance input. Ensure that the voltage level is well defined during operation and no transient noise is coupled on this line, otherwise the module may detect a spurious power-on request

2.2.1.7 Digital pins

- **External Reset (RESET_N)**: input for external reset, a logic low voltage will reset the module
- **SIM Card Interface (VSIM, SIM_CLK, SIM_IO, SIM_RST)**: the SIM layout may be critical if the SIM card is placed far away from LEON-G100/G200 or in close vicinity of RF antenna. In the first case the long connection may radiate higher harmonic of digital data. In the second case the same harmonics may be picked up and create self-interference that can reduce the sensitivity of GSM Receiver channels whose carrier frequency is coincident with harmonic frequencies. In the later case using RF bypass capacitors on the digital line will mitigate the problem. In addition, since the SIM card typically accesses by the end use, it may be subjected to ESD discharges: add adequate ESD protection to improve the robustness of the digital pins within the module. Remember to add such ESD protection along the path between SIM holder toward the module
- **Digital Audio (I2S_CLK, I2S_RX, I2S_TX, I2S_WA)**: the I^2S interface requires the same consideration regarding electro-magnetic interference as the SIM card. Keep the traces short and avoid coupling with RF line or sensitive analog inputs
- **DDC (SCL, SDA)**: the DDC interface requires the same consideration regarding electro-magnetic interference as for SIM card. Keep the traces short and avoid coupling with RF line or sensitive analog inputs
- **UART (TXD, RXD, CTS, RTS, DSR, RI, DCD, DTR)**: the serial interface require the same consideration regarding electro-magnetic interference as for SIM card. Keep the traces short and avoid coupling with RF line or sensitive analog inputs

2.2.2 Footprint and paste mask

Figure 45 and Figure 46 describe the footprint and provide recommendations for the paste mask for LEON modules. These are recommendations only and not specifications. Note that the copper and solder masks have the same size and position.

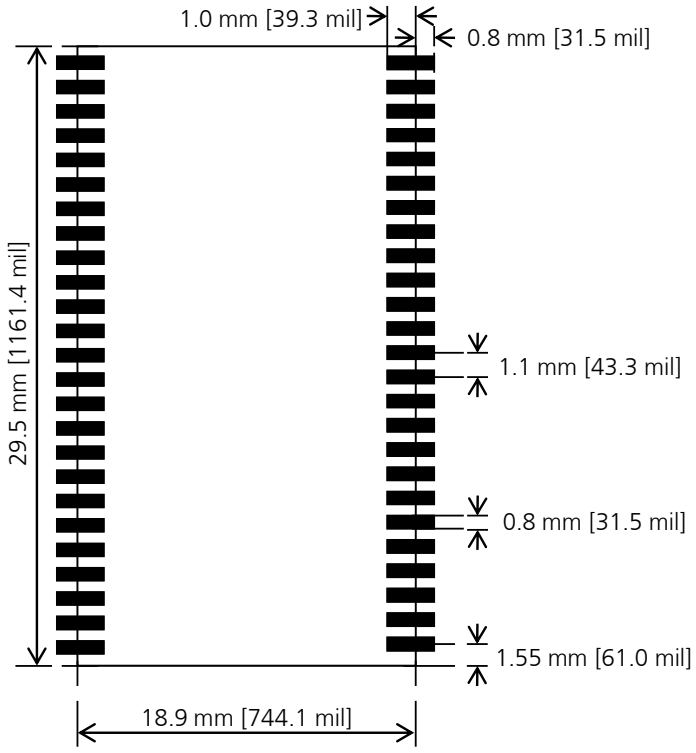

Figure 45: LEON-G100/G200 footprint

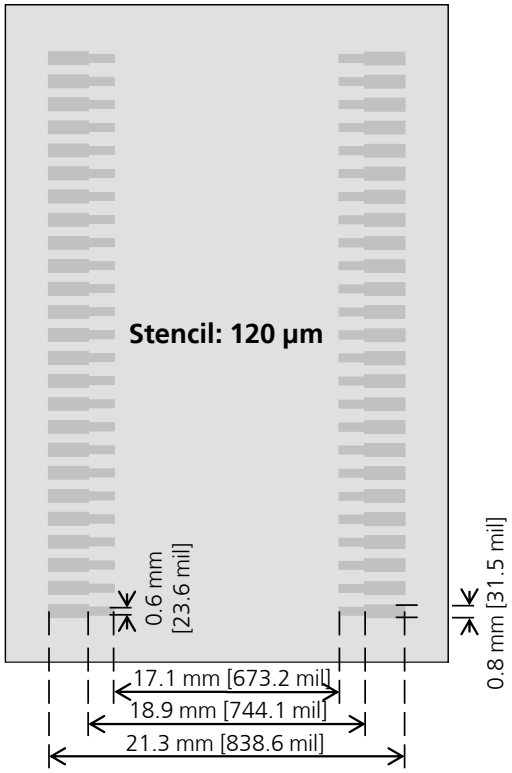

Figure 46: LEON-G100/G200 paste mask

To improve the wetting of the half vias, reduce the amount of solder paste under the module and increase the volume outside of the module by defining the dimensions of the paste mask to form a T-shape (or equivalent) extending beyond the Copper mask. The solder paste should have a total thickness of 120 µm.

☞ The paste mask outline needs to be considered when defining the minimal distance to the next component.

☞ The exact geometry, distances, stencil thicknesses and solder paste volumes must be adapted to the specific production processes (e.g. soldering etc.) of the customer.

The bottom layer of LEON-G100/G200 shows some unprotected copper areas for **GND** and **VCC** signals, plus **GND** keep-out for internal RF signals routing.

☞ Consider "No-routing" areas for the LEON-G100/G200 footprint as follows:

1. Ground copper and signals keep-out below LEON-G100/G200 on Application Motherboard due to **VCC** area, RF **ANT** pin and exposed GND pad on module bottom layer (see Figure 47).
2. Signals Keep-Out below module on Application Motherboard due to GND opening on LEON-G100/G200 bottom layer for internal RF signals (see Figure 48).

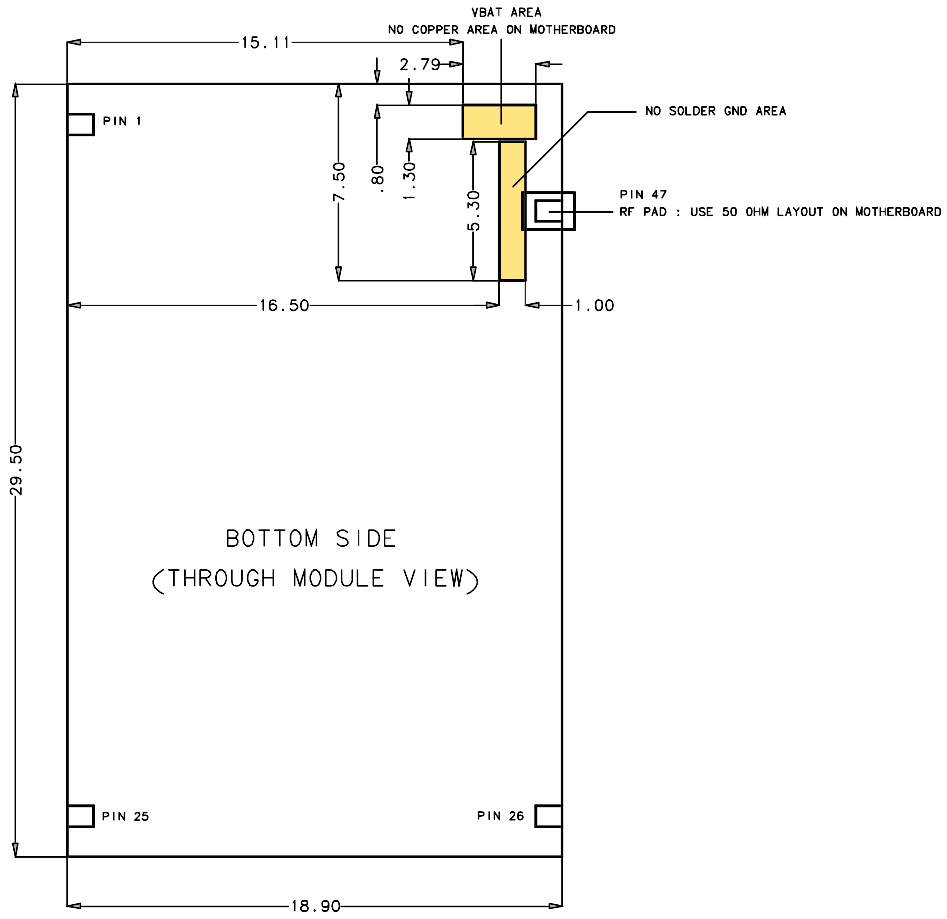

Figure 47: Ground copper and signal keep-out below data module on application motherboard due to due to VCC area, RF ANT pin and exposed GND pad on data module bottom layer

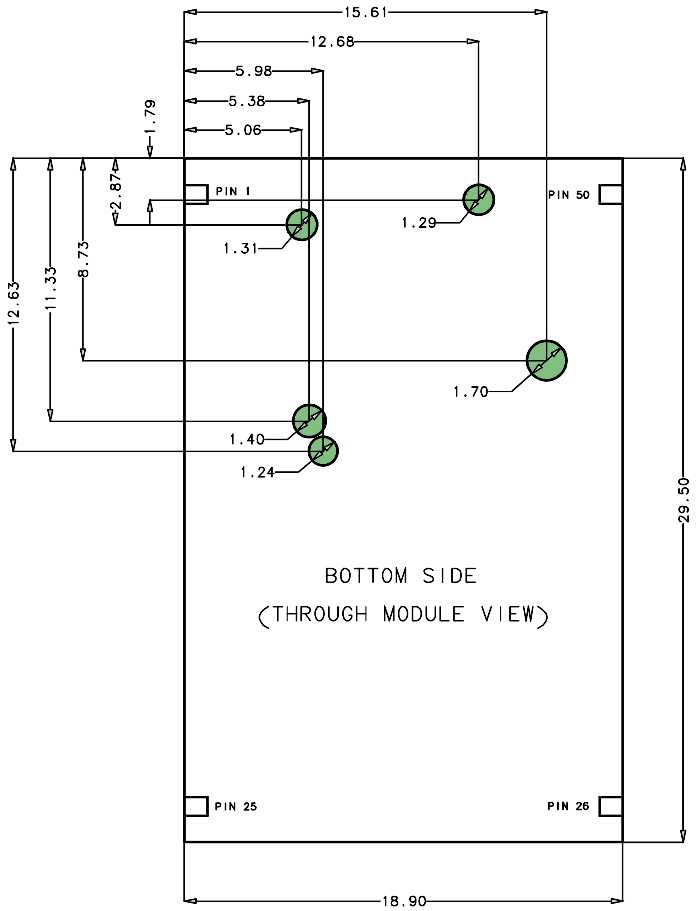

Figure 48: Signals keep-out below data module on application motherboard due to GND opening on data module bottom layer for internal RF signals

Routing below LEON-G100/G200 on application motherboard is generally possible but not recommended: in addition to the required keep-out defined before, consider that the insulation offered by the solder mask painting may be weakened corresponding to micro-vias on LEON-G100/G200 bottom layer, thus increasing the risk of short to GND if the application motherboard has unprotected signal routing on same coordinates.

2.2.3 Placement

Optimize placement for minimum length of RF line and closer path from DC source for **VCC**.

2.3 Module thermal resistance

The Case-to-Ambient thermal resistance (R_{C-A}) of the module, with the LEON-G100/G200 mounted on a 130 x 110 x 1.6 mm FR4 PCB with a high coverage of copper (e.g. the EVK-G25H evaluation kit) in still air conditions is equal to 14°C/W.

With this Case-to-Ambient thermal resistance, the increase of the module temperature is:

- Around 12°C when the module transmits at the maximum power level during a GSM call in the GSM/EGSM bands

- Around 17°C when the module transmits at the maximum power level during a GPRS data transfer (2 Tx + 3 Rx slots) in the GSM/EGSM bands

☞ Case-to-Ambient thermal resistance value will be different than the one provided if the module is mounted on a PCB with different size and characteristics.

2.4 Antenna guidelines

Antenna characteristics are essential for good functionality of the module. The radiating performance of antennas has direct impact on the reliability of connection over the Air Interface. Bad termination of **ANT** can result in poor performance of the module.

The following parameters should be checked:

Item	Recommendations
Impedance	50 Ω nominal characteristic impedance
Frequency Range	Depends on the Mobile Network used. GSM900: 880..960 MHz GSM1800: 1710..1880 MHz GSM850: 824..894 MHz GSM1900: 1850..1990 MHz
Input Power	>2 W peak
V.S.W.R	<2:1 recommended, <3:1 acceptable
Return Loss	S_{11}<-10 dB recommended, S_{11}<-6 dB acceptable
Gain	<3 dBi

Table 30: General recommendation for GSM antenna

GSM antennas are typically available as:

- Linear monopole: typical for fixed application. The antenna extends mostly as a linear element with a dimension comparable to lambda/4 of the lowest frequency of the operating band. Magnetic base may be available. Cable or direct RF connectors are common options. The integration normally requires the fulfillment of some minimum guidelines suggested by antenna manufacturer
- Patch-like antenna: better suited for integration in compact designs (e.g. mobile phone). They are mostly custom designs where the exact definition of the PCB and product mechanical design is fundamental for tuning of antenna characteristics

For integration observe these recommendations:

- Ensure 50 Ω antenna termination, minimize the V.S.W.R. or return loss, as this will optimize the electrical performance of the module. See section 2.4.1
- Select antenna with best radiating performance. See section 2.4.2
- If a cable is used to connect the antenna radiating element to application board, select a short cable with minimum insertion loss. The higher the additional insertion loss due to low quality or long cable, the lower the connectivity
- Follow the recommendations of the antenna manufacturer for correct installation and deployment
- Do not include antenna within closed metal case
- Do not place antenna in close vicinity to end user since the emitted radiation in human tissue is limited by S.A.R. regulatory requirements
- Do not use directivity antenna since the electromagnetic field radiation intensity is limited in some countries
- Take care of interaction between co-located RF systems since the GSM transmitted power may interact or disturb the performance of companion systems
- Place antenna far from sensitive analog systems or employ countermeasures to reduce electromagnetic compatibility issues that may arise

2.4.1 Antenna termination

LEON-G100/G200 modules are designed to work on a 50 Ω load. However, real antennas have no perfect 50 Ω load on all the supported frequency bands. To reduce as much as possible performance degradation due to antenna mismatch, the following requirements should be met:

- Measure the antenna termination with a network analyzer: connect the antenna through a coaxial cable to the measurement device, the $|S_{11}|$ indicates which portion of the power is delivered to antenna and which portion is reflected by the antenna back to the modem output
- A good antenna should have a $|S_{11}|$ below -10 dB over the entire frequency band. Due to miniaturization, mechanical constraints and other design issues, this value will not be achieved. A value of $|S_{11}|$ of about -6 dB - (in the worst case) - is acceptable

Figure 49 shows an example of this measurement:

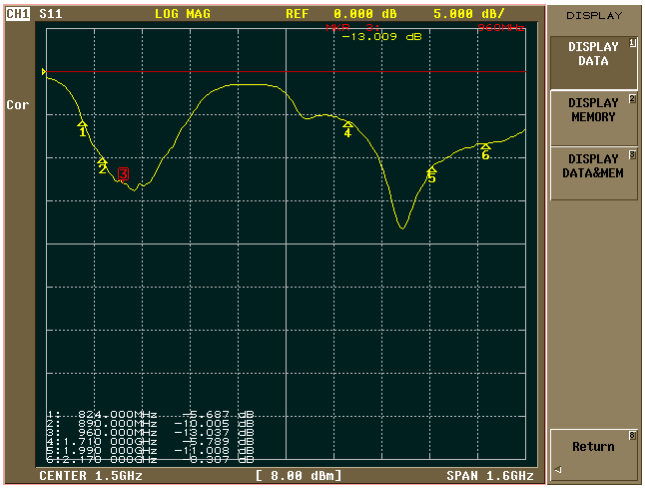

Figure 49: $|S_{11}|$ sample measurement of a penta-band antenna that covers in a small form factor the 4 GSM bands (850 MHz, 900 MHz, 1800 MHz and 1900 MHz) and the UMTS Band I

Figure 50 shows comparable measurements performed on a wideband antenna. The termination is better, but the size of the antenna is considerably larger.

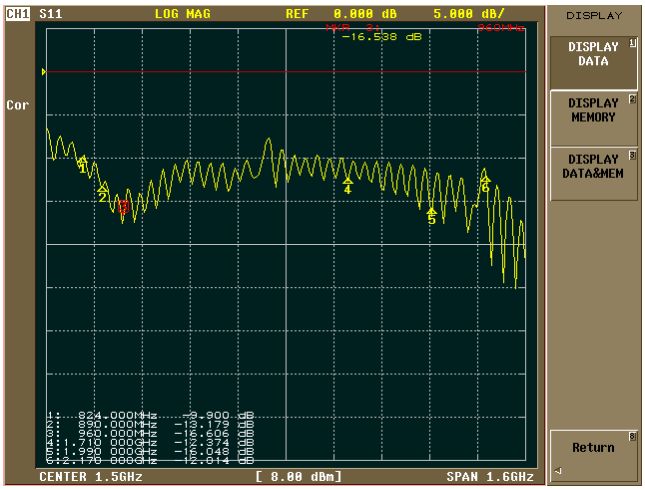

Figure 50: $|S_{11}|$ sample measurement of a wideband antenna

2.4.2 Antenna radiation

An indication of the radiated power by the antenna can be approximated by measuring the $|S_{21}|$ from a target antenna to the measurement antenna, measured with a network analyzer using a wideband antenna. Measurements should be done at a fixed distance and orientation. Compare the results to measurements performed on a known good antenna. Figure 51 through Figure 52 show measurement results. A wideband log periodic-like antenna was used, and the comparison was done with a half lambda dipole tune on 900 MHz frequency. The measurements show both the $|S_{11}|$ and $|S_{21}|$ for penta-band internal antenna and for the wideband antenna.

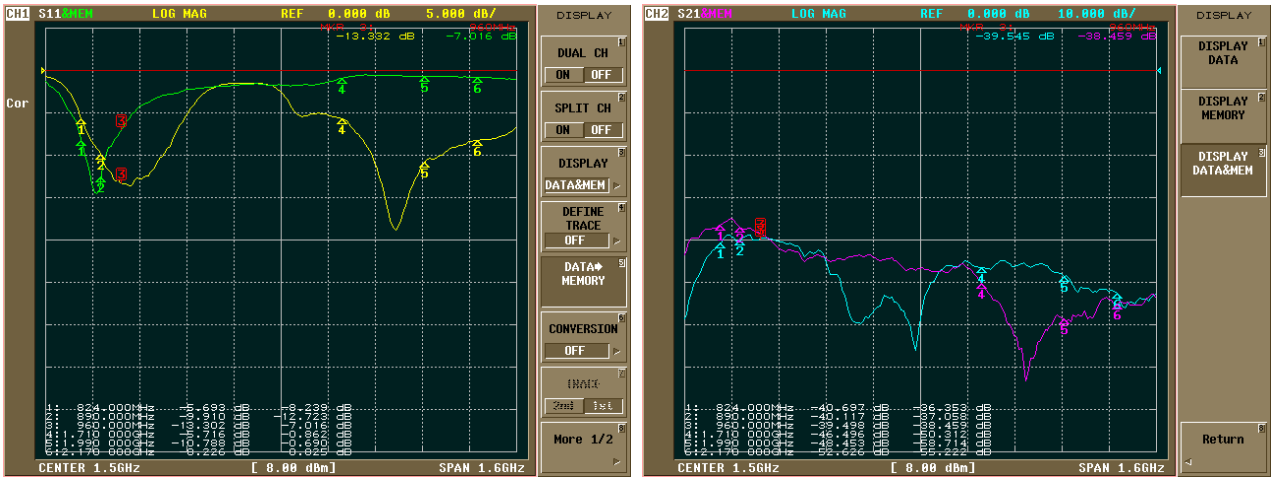

Figure 51: $|S_{11}|$ and $|S_{21}|$ comparison of a 900 MHz tuned half wavelength dipole and a penta-band internal antenna

The half lambda dipole tuned to 900 MHz is known to have good radiation performance (both for gain and directivity). By comparing the $|S_{21}|$ measurement with the antenna under investigation for the frequency for which the half dipole is tuned (e.g. marker 3 in Figure 51) it is possible to rate the antenna being tested. If the performance of the two antennas is similar then the target antenna is good.

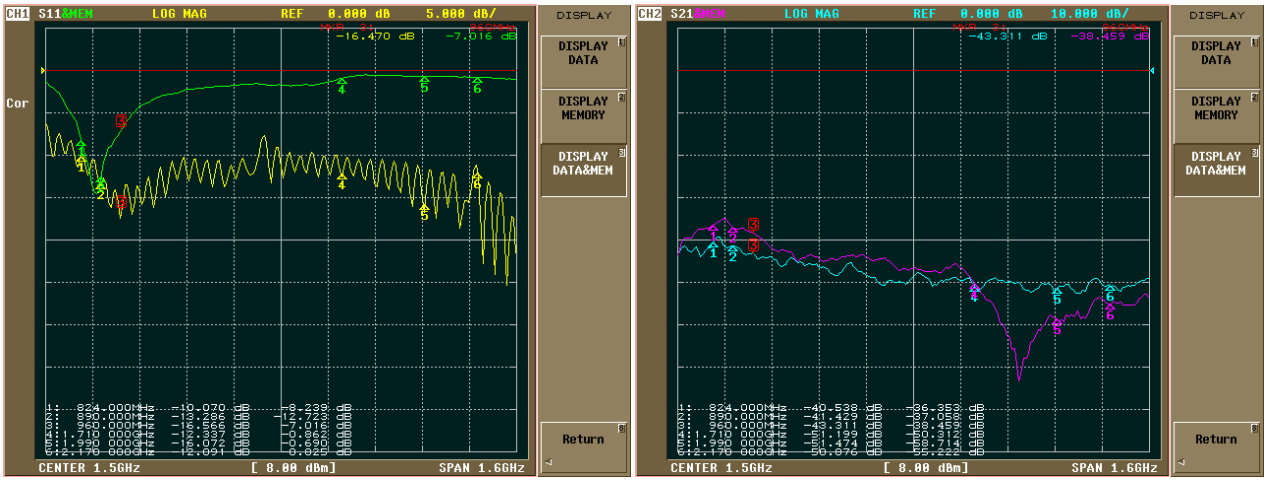

Figure 52: $|S_{11}|$ and $|S_{21}|$ comparison between a 900 MHz tuned half wavelength dipole and a wideband commercial antenna

If $|S_{21}|$ values for the tuned dipole are much better than for the antenna under evaluation (e.g. as seen by markers 1 and 2 of the S21 comparison in Figure 52, where the dipole performance is 5 dB better), then it can be concluded that the radiation of the antenna under evaluation is considerably less.

The same procedure should be repeated for other bands with the half wavelength dipole re-tuned to the band under investigation.

☞ For good antenna radiation performance, antenna dimensions should be comparable to a quarter of the wavelength. Different antenna types can be used for the module, many of them (e.g. patch antennas, monopole) are based on a resonating element that works in combination with a ground plane. The ground plane, ideally infinite, can be reduced down to a minimum size that must be similar to one quarter of the wavelength of the minimum frequency that has to be radiated (transmitted/received). Numerical sample: frequency = 1 GHz → wavelength = 30 cm → minimum ground plane (or antenna size) = 7.5 cm. Below this size, the antenna efficiency is reduced.

2.4.3 Antenna detection functionality

The internal antenna detect circuit is based on ADC measurement at **ANT** pin: the RF port is DC coupled to the ADC unit in the baseband chip which injects a DC current (30 µA) on **ANT** and measures the resulting DC voltage to evaluate the resistance from **ANT** pad to GND.

The antenna detection is performed by the measurement of the resistance from **ANT** pad to GND (DC element of the GSM antenna), that is forced by the +UANTR AT command: refer to u-blox 2G GSM/GPRS AT Commands Manual [2] for more details on how to access to this feature.

To achieve good antenna detection functionality, use an RF antenna with built-in resistor from **ANT** signal to GND, or implement an equivalent solution with a circuit between the antenna cable connection and the radiating element as shown in Figure 53.

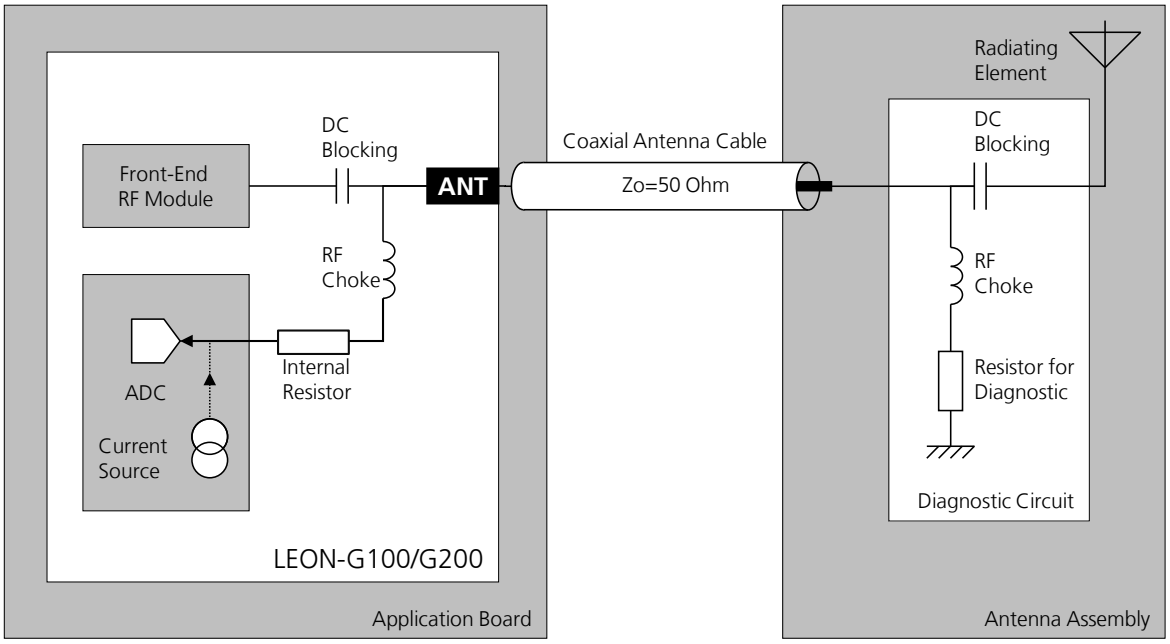

Figure 53: Module Antenna Detection circuit and antenna with diagnostic resistor

Examples of components for the antenna detection diagnostic circuit are reported in the following table:

Description	Part Number - Manufacturer
DC Blocking Capacitor	Murata GRM1555C1H220JA01 or equivalent
RF Choke Inductor	Murata LQG15HS68NJ02, LQG15HH68NJ02 or equivalent
Resistor for Diagnostic	15kΩ 5%, various Manufacturers

Table 31: Example of components for the antenna detection diagnostic circuit

Please note that the DC impedance at RF port for some antennas may be a DC open (e.g. linear monopole) or a DC short to reference GND (e.g. PIFA antenna). For those antennas, without the diagnostic circuit Figure 53, the measured DC resistance will be always on the extreme of measurement range (respectively open or short), and there will be no mean to distinguish from defect on antenna path with similar characteristic (respectively: removal of linear antenna or RF cable shorted to GND for PIFA antenna).

Furthermore, any other DC signal injected to the RF connection from **ANT** connector to radiating element will alter the measurement and produce invalid results for antenna detection.

It is recommended to use an antenna with a built-in diagnostic resistor in the range from 5 kΩ to 30 kΩ to assure good antenna detection functionality and to avoid a reduction of module RF performances.

For example: consider GSM antennas with built-in DC load resistor of 15 kΩ.

Using the +UANTR AT command, the module reports the resistance value evaluated from **ANT** pad to GND:

- Reported values close to the used diagnostic resistor nominal value (i.e. values from 10 kΩ to 20 kΩ if a 15 kΩ diagnostic resistor is used) indicate that the antenna is connected
- Values above the maximum measurement range limit (about 53 kΩ) indicate that the antenna is not connected
- Reported values below the minimum measurement range limit (about 1 kΩ) indicate that the antenna is shorted to GND
- Measurement inside the valid measurement range and outside the expected range may indicate an improper connection, damaged antenna or wrong value of antenna load resistor for diagnostic

2.5 ESD Immunity Test Precautions

The immunity to EMS phenomenon Electrostatic Discharge of the device (i.e. the application board where the module is mounted) must be certified complying the testing requirements standard [9] and the requirements for radio and digital cellular radio telecommunications system equipments standards [10] [11].

The ESD test is performed at the enclosure port [10] referred as the physical boundary through which EM field radiates. If the device implements an integral antenna [10] the enclosure is intended as all insulating surfaces housing the device. If the device implements a removable antenna [10] the enclosure port is limited to the antenna port [10] hence the enclosure port comprises the antenna element and its interconnecting cable surfaces.

The applicability of the ESD test depends to the device classification [10], as well the test on other ports [10] or on interconnecting cables to auxiliary equipments depends to the device accessible interfaces and manufacturer requirements.

Contact discharges [9] are performed at conductive surfaces whereas air discharges [9] are performed at insulating surfaces. Indirect contact discharges are performed to the measurement setup horizontal and vertical coupling planes [9].

In order to satisfy ESD immunity test requirements [9] [10] [11] performed at device enclosure complying the category level [10] shown in the following table, some precautions should be implemented as described in the following sections.

Category	Immunity Level
Contact Discharge to coupling planes (indirect contact discharge)	+2 kV / -2 kV
	+4 kV / -4 kV
Contact Discharges to conducted surfaces (direct contact discharge)	Not Applicable[2]*
Air Discharge at insulating surfaces	+2 kV / -2 kV
	+4 kV / -4 kV
	+8 kV / -8 kV

Table 32: Enclosure ESD immunity level, standards "EN 61000-4-2, EN 301 489-1 V1.8.1, EN 301 489-7 V1.3.1"

2.5.1 General Precautions

The following module interfaces could be involved in the ESD immunity test criticalness depending on the application board handling. Some precautions are herein suggested.

A series Schottky diode is integrated in LEON-G100/G200 modules as protection on the **RESET_N** pin. The external circuit must be able to cause a current flow through the series diode to determine the RESET_N state.

Sensitive interface is the reset line (**RESET_N** pin):

- A 47 pF bypass capacitor (e.g. Murata GRM1555C1H470JA01) have to be mounted on the line termination connected to the **RESET_N** pin to avoid a module reset caused by an electrostatic discharge applied to the application board

[2] LEON mounted on application reference design:

Applicability -> EUT with insulating surfaces, air discharges on interconnecting cables between EUT and antenna and auxiliary equipments

Not Applicability -> EUT with conductive surface, direct contact discharge

- A series ferrite bead (e.g. Murata BLM15HD182SN1) must be added on the line connected to the **RESET_N** pin to avoid a module reset caused by an electrostatic discharge applied to the application board
- It is recommended to keep the connection line to **RESET_N** as short as possible

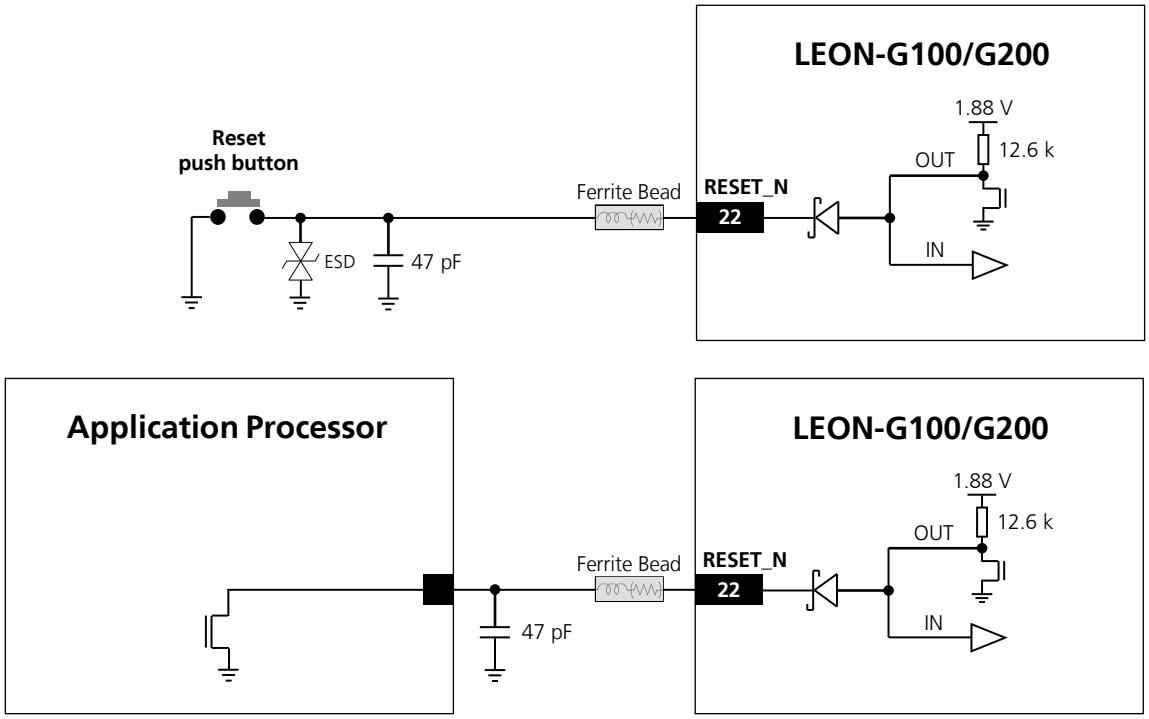

Figure 54: Application circuits to reset line for ESD immunity test

Sensitive interface is the SIM interface (**VSIM** pin, **SIM_RST** pin, **SIM_IO** pin, **SIM_CLK** pin):

- A 47 pF bypass capacitor (e.g. Murata GRM1555C1H470J) have to be mounted on the lines connected to **VSIM**, **SIM_RST**, **SIM_IO** and **SIM_CLK** to assure SIM interface functionality when an electrostatic discharge is applied to the application board
- It is suggested to use as short as possible connection lines at SIM pins

2.5.2 Antenna Interface Precautions

The antenna interface **ANT** pin could be involved in the ESD immunity test criticalness depending on the application board handling. Antenna port precaution is herein suggested.

- If the device implements an embedded antenna and the device insulating enclosure avoid air discharge up to +8 kV / -8 kV to the antenna interface, no further precautions to ESD immunity test should be needed
- If the device implements an external antenna and the antenna and its connecting cable are provided with completely insulating enclosure to avoid air discharge up to +8 kV / -8 kV to the whole antenna and cable surfaces, no further precautions to ESD immunity test should be needed
- If the device implements an external antenna and the antenna or its connecting cable are not provided with completely insulating enclosure to avoid air discharge up to +8 kV / -8 kV to the whole antenna and cable surfaces, the following precautions to ESD immunity test should be implemented on the application board

ANT port ESD rating is 4 kV (contact discharge according to IEC 61000-4-2). A higher protection level is required if the line is externally accessible on the application board.

A higher protection level can be achieved with an external high pass filter, consists of a series 15 pF capacitor (e.g. Murata GRM1555C1H150JA01) and a shunt 39 nH coil (e.g. Murata LQG15HN39NJ102) connected to the **ANT** port.

Note that antenna detection functionality will be not provided implementing this high pass filter for ESD protection on the **ANT** port.

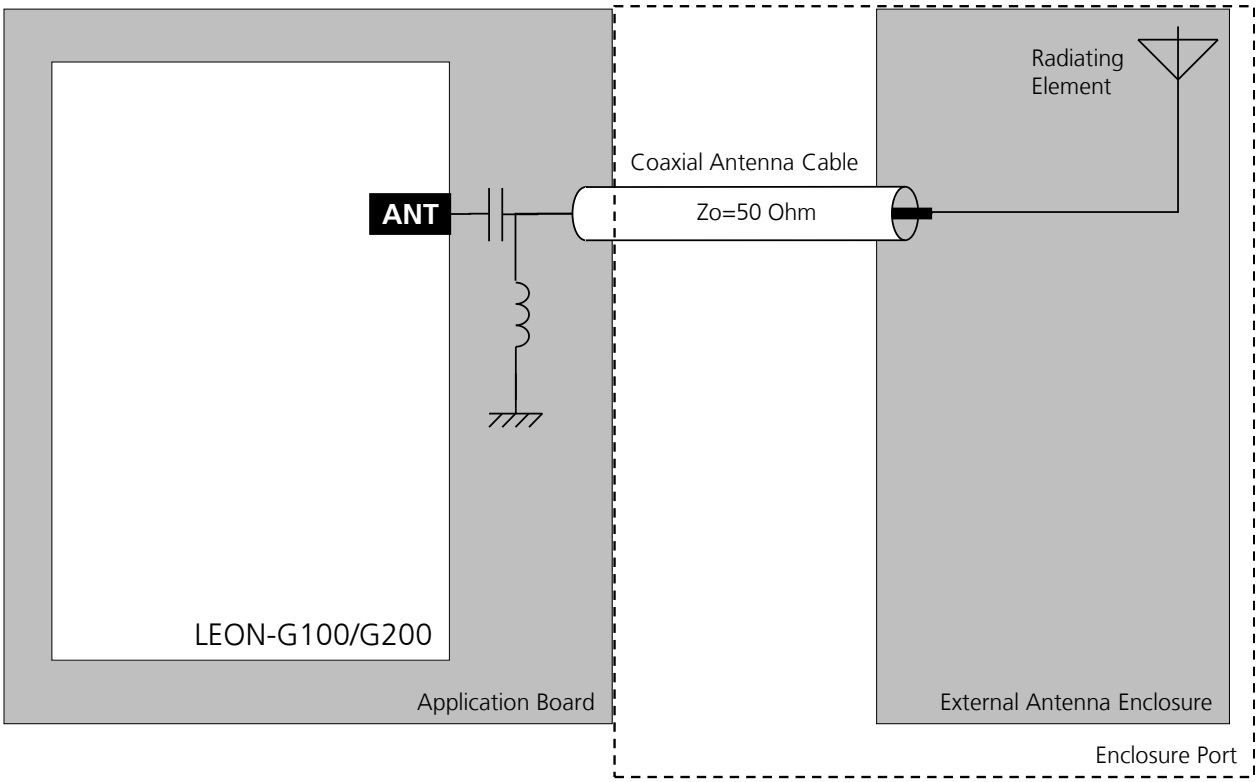

Figure 55: Antenna high pass filter circuit for ESD protection and external antenna

2.5.3 Module Interfaces Precautions

Any module pins that are externally accessible, should be included in the ESD immunity test since they are considered to be a port [10]. Depending on applicability, and in order to satisfy ESD immunity test requirements and ESD category level, pins connected to the port should be protected up to +4 kV / -4 kV for direct Contact Discharge, and up to +8 kV / -8 kV for Air Discharge applied to the enclosure.

The maximum ESD rating of all the pins of the module, except the ANT pin, is 1 kV (HBM according MIL-Std 883D, method 3015.7, EOS/ESD Standard S5.1-1993). A higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array).

3 Handling and soldering

☞ No natural rubbers, no hygroscopic materials nor materials containing asbestos are employed.

3.1 Packaging, shipping, storage and moisture preconditioning

For information pertaining to reels and tapes, Moisture Sensitivity levels (MSD), shipment and storage information, as well as drying for preconditioning see the LEON-G100/G200 Data Sheet [1]. LEON-G100/G200 modules are Electro-Static Discharge (ESD) sensitive devices.

⚠ **Ensure ESD precautions are implemented during handling of the module.**

3.2 Soldering

3.2.1 Soldering paste

Use of "No Clean" soldering paste is strongly recommended, as it does not require cleaning after the soldering process has taken place. The paste listed in the example below meets these criteria.

Soldering Paste:	OM338 SAC405 / Nr.143714 (Cookson Electronics)
Alloy specification:	Sn 95.5 / Ag 3.9 / Cu 0.6 (95.5% Tin / 0.6 % Silver / 0.6% Copper)
	95.5% Sn / 4.0% Ag / 0.5% Cu (95.5% Tin / 4.0 % Silver / 0.5% Copper)
Melting Temperature:	217°C
Stencil Thickness:	120 µm for base boards

The final choice of the soldering paste depends on the approved manufacturing procedures.

The paste-mask geometry for applying soldering paste should meet the recommendations in section 2.2.2

☞ The quality of the solder joints on the connectors ('half vias') should meet the appropriate IPC specification.

3.2.2 Reflow soldering

A convection type-soldering oven is strongly recommended over the infrared type radiation oven. Convection heated ovens allow precise control of the temperature and all parts will be heated up evenly, regardless of material properties, thickness of components and surface color.

Consider the "IPC-7530 Guidelines for temperature profiling for mass soldering (reflow and wave) processes, published 2001".

Preheat phase

Initial heating of component leads and balls. Residual humidity will be dried out. Please note that this preheat phase will not replace prior baking procedures.

- Temperature rise rate: max 3°C/s — If the temperature rise is too rapid in the preheat phase it may cause excessive slumping.

- Time: 60 – 120 s — If the preheat is insufficient, rather large solder balls tend to be generated. Conversely, if performed excessively, fine balls and large balls will be generated in clusters.
- End Temperature: 150 - 200°C — If the temperature is too low, non-melting tends to be caused in areas containing large heat capacity.

Heating/ reflow phase

The temperature rises above the liquidus temperature of 217°C. Avoid a sudden rise in temperature as the slump of the paste could become worse.

- Limit time above 217°C liquidus temperature: 40 - 60 s
- Peak reflow temperature: 245°C

Cooling phase

A controlled cooling avoids negative metallurgical effects (solder becomes more brittle) of the solder and possible mechanical tensions in the products. Controlled cooling helps to achieve bright solder fillets with a good shape and low contact angle.

- Temperature fall rate: max 4°C / s

☞ To avoid falling off, modules should be placed on the topside of the motherboard during soldering.

The final soldering temperature chosen at the factory depends on additional external factors like choice of soldering paste, size, thickness and properties of the base board, etc. Exceeding the maximum soldering temperature in the recommended soldering profile may permanently damage the module.

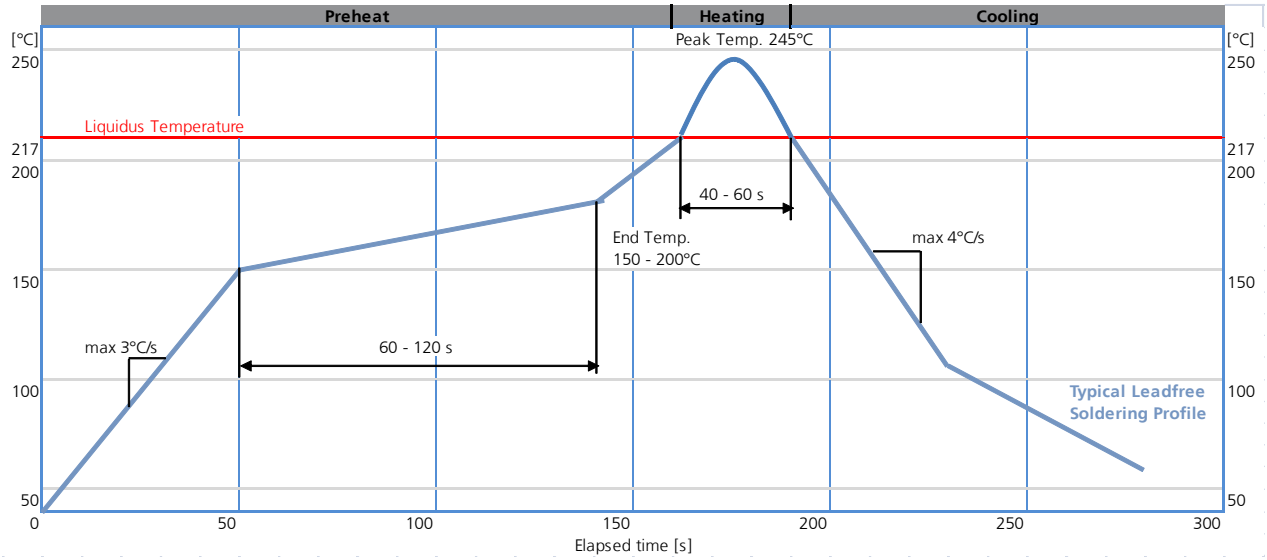

Figure 56: Recommended soldering profile

☞ When soldering lead-free LEON-G100/G200 modules in a leaded process, check the following temperatures:

PB- Technology Soaktime: 40-80 s
Time above Liquidus: 40-90 s
Peak temperature: 225-235°C

☞ LEON-G100/G200 modules must not be soldered with a damp heat process.

3.2.3 Optical inspection

After soldering the LEON-G100/G200 module, inspect the modules optically to verify that he module is properly aligned and centered.

3.2.4 Cleaning

Cleaning the soldered modules is not recommended. Residues underneath the modules cannot be easily removed with a washing process.

- Cleaning with water will lead to capillary effects where water is absorbed in the gap between the baseboard and the module. The combination of residues of soldering flux and encapsulated water leads to short circuits or resistor-like interconnections between neighboring pads. Water will also damage the sticker and the ink-jet printed text.
- Cleaning with alcohol or other organic solvents can result in soldering flux residues flooding into the two housings, areas that are not accessible for post-wash inspections. The solvent will also damage the sticker and the ink-jet printed text.
- Ultrasonic cleaning will permanently damage the module, in particular the quartz oscillators.

For best results use a "no clean" soldering paste and eliminate the cleaning step after the soldering.

3.2.5 Repeated reflow soldering

Only a single reflow soldering process is encouraged for boards with a LEON-G100/G200 module populated on it. The reason for this is the risk of the module falling off due to high weight in relation to the adhesive properties of the solder.

3.2.6 Wave soldering

Boards with combined through-hole technology (THT) components and surface-mount technology (SMT) devices require wave soldering to solder the THT components. Only a single wave soldering process is encouraged for boards populated with LEON-G100/G200 modules.

3.2.7 Hand soldering

Hand soldering is not recommended.

3.2.8 Rework

The LEON-G100/G200 module can be unsoldered from the baseboard using a hot air gun.

Avoid overheating the module.

After the module is removed, clean the pads before placing.

Never attempt a rework on the module itself, e.g. replacing individual components. Such actions immediately terminate the warranty.

3.2.9 Conformal coating

Certain applications employ a conformal coating of the PCB using HumiSeal® or other related coating products.

These materials affect the HF properties of the LEON-G100/G200 modules and it is important to prevent them from flowing into the module.

The RF shields do not provide 100% protection for the module from coating liquids with low viscosity, therefore care is required in applying the coating.

Conformal Coating of the module will void the warranty.

3.2.10 Casting

If casting is required, use viscose or another type of silicon pottant. The OEM is strongly advised to qualify such processes in combination with the LEON-G100/G200 module before implementing this in the production.

☞ Casting will void the warranty.

3.2.11 Grounding metal covers

Attempts to improve grounding by soldering ground cables, wick or other forms of metal strips directly onto the EMI covers is done at the customer's own risk. The numerous ground pins should be sufficient to provide optimum immunity to interferences and noise.

☞ u-blox gives no warranty for damages to the LEON-G100/G200 module caused by soldering metal cables or any other forms of metal strips directly onto the EMI covers.

3.2.12 Use of ultrasonic processes

Some components on the LEON-G100/G200 module are sensitive to Ultrasonic Waves. Use of any Ultrasonic Processes (cleaning, welding etc.) may cause damage to the module.

☞ u-blox gives no warranty against damages to the LEON-G100/G200 module caused by any Ultrasonic Processes.

4 Product Testing

4.1 u-blox in-series production test

u-blox focuses on high quality for its products. All units produced are fully tested. Defective units are analyzed in detail to improve the production quality.

This is achieved with automatic test equipment, which delivers a detailed test report for each unit. The following measurements are done:

- Digital self-test (software download, verification of Flash firmware, etc.)
- Measurement of voltages and currents
- Measurement of RF characteristics

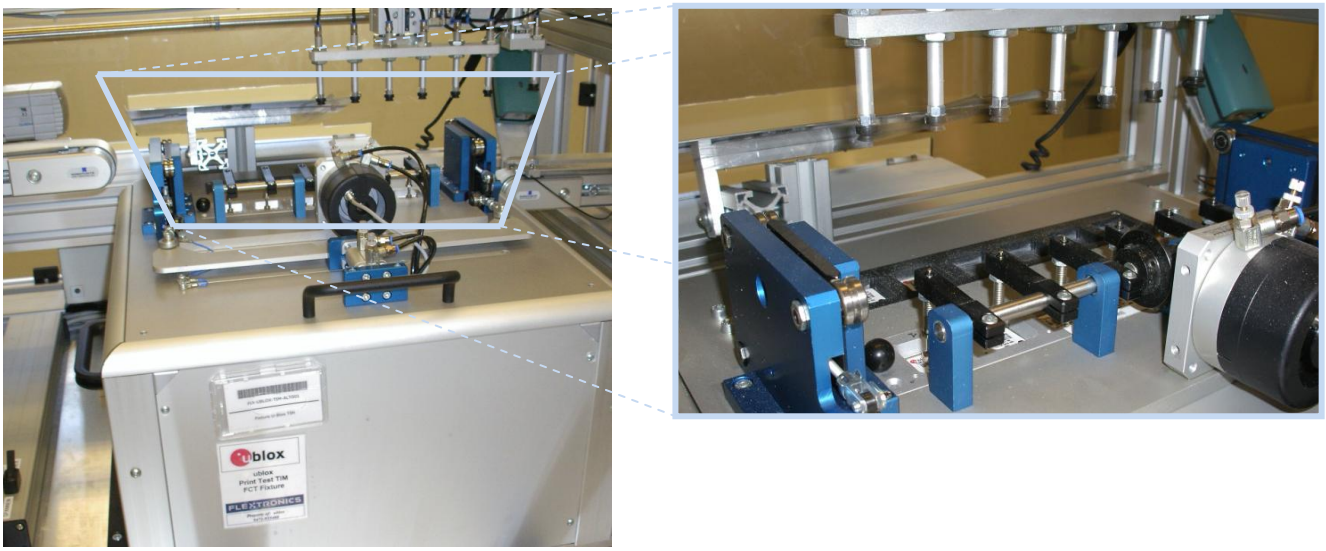

Figure 57: Automatic test equipment for module tests

Appendix

A Extra Features

A.1 Firmware (upgrade) Over The Air (FOTA) (LEON-G200 only)

LEON-G100/G200 Firmware can be updated Over The Air. The main idea is that Firmware can be updated over the air reducing the amount of data transmitted. This is achieved by downloading into LEON not the full Firmware, only the "delta file" which contains only the differences between the two firmware versions (old and new), and compressing the "delta file".

To perform the update over the air of LEON FW, a 3rd party library from RedBend has been integrated into the FW. This library allows to download into the module just a "delta" between the 2 FW versions (the one on the module and the upgrade); in this way it is possible to transfer less data and use less space on the flash for storing it.

For more details please refer to Firmware Update Application Note [13].

A.2 Firmware (upgrade) Over AT (FOAT)

Firmware upgrade is available with LEON-G100/G200 modules using AT commands.

A.2.1 Overview

This feature allows upgrade the module Firmware over UART, using AT Commands.

- AT Command AT+UFWUPD triggers a reboot and followed by upgrade procedure at specified baud rate (refer to u-blox 2G GSM/GPRS AT Commands Manual [2] for more details)
- The Xmodem-1k protocol is used for downloading the new Firmware image via a terminal application
- A special boot loader on the module performs Firmware installation, security verifications and module reboot
- Firmware authenticity verification is performed via a security signature during the download. Firmware is then installed, overwriting the current version. In case of power loss during this phase, the boot loader detects a fault at the next wake-up, and restarts the Firmware download from the Xmodem-1k handshake. After completing the upgrade, the module is reset again and wakes-up in normal boot

A.2.2 FOAT procedure

The application processor must proceed in the following way:

- send through the UART the AT+UFWUPD command, specifying the file type and the desired baud rate
- reconfigure the serial communication at the selected baud rate, without flow control with the Xmodem-1k protocol
- send the new FW image via Xmodem-1k

A.3 Firewall

The feature allows the LEON-G100/G200 user to reject incoming connections originated from IP addresses different from the specified list and inserted in a black list.

A.4 TCP/IP

Via the AT commands it's possible to access the TCP/IP functionalities over the GPRS connection. For more details about AT commands see the u-blox 2G GSM/GPRS AT Commands Manual [2].

A.4.1 Multiple IP addresses and sockets

Using LEON's embedded TCP/IP or UDP/IP stack, only 1 IP instance (address) is supported. The IP instance supports up to 16 sockets. Using an external TCP/IP stack (on the application processor), it is possible to have 2 IP instances (addresses).

A.5 FTP

LEON-G100/G200 modules support the File Transfer Protocol functionalities via AT commands. Files are read and stored in the local file system of the module. For more details about AT commands see the u-blox 2G GSM/GPRS AT Commands Manual [2].

A.6 HTTP

HTTP client is implemented in LEON. HEAD, GET, POST, DELETE and PUT operations are available. The file size to be uploaded / downloaded depends on the free space available in the local file system (FFS) at the moment of the operation. Up to 4 HTTP client contexts to be used simultaneously.

For more details about AT commands see the u-blox 2G GSM/GPRS AT Commands Manual [2].

A.7 SMTP

LEON supports SMTP client functionalities. It is possible to specify the common parameters (e.g. server data, authentication method, etc.) can be specified, to send an email to a SMTP server. Emails can be send with or without attachment. Attachments are store in the local file system of LEON.

For more details about AT commands see the u-blox 2G GSM/GPRS AT Commands Manual [2].

A.8 GPS

The LEON-G100/G200 modules allow a simple and fast connection with the u-blox GPS modules (u-blox 5 family and above). Via the DDC bus it's possible to communicate and exchange data, while the available GPIOs can handle the GPS device power on/off.

For information about implementing u-blox GPS with LEON-G100/G200 modules, including using u-blox' AssistNow Assisted GPS (A-GPS) service see the GPS Integration Application Note [3].

B Glossary

3GPP	3rd Generation Partnership Project
AC	Alternating Current
ADC	Analog to Digital Converter
ADN	Abbreviated Dialing Numbers
AMR	Adaptive Multi Rate
ASIC	Application Specific Integrated Circuit
AT	AT Command Interpreter Software Subsystem, or attention
BB	Baseband
CBCH	Cell Broadcast Channel
CBS	Cell Broadcast Services
CLK	Clock
CMOS	Complementary Metal Oxide Semiconductor
CS	Coding Scheme or Chip Select
CTS	Clear To Send
DAC	Digital Analog Converter
DC	Direct Current
DCD	Data Carrier Detect
DCE	Data Communication Equipment
DCS	Digital Cellular System
DDC	Display Data Channel
DL	Down Link (Reception)
DRX	Discontinuous Reception
DSP	Digital Signal Processing
DSR	Data Set Ready
DTE	Data Terminal Equipment
DTR	Data Terminal Ready
EBU	External Bus Interface Unit
EEP	EEPROM Emulation Parameters
EGSM	Extended GSM
EM	ElectroMagnetic
EMC	Electromagnetic Compatibility
EMI	ElectroMagnetic Interference
EMS	ElectroMagnetic Static
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
EUT	Equipment Under Test
FAQ	Frequently Asked Questions
FDN	Fixed Dialing Numbers
FET	Field Effect Transistor
FFS	Flash File System
FIR	Finite Impulse Response
FOAT	Firmware (upgrade) Over AT
FOTA	Firmware Over The Air
FTP	File Transfer Protocol
FW	Firmware
GND	Ground
GPIO	General Purpose Input Output
GPRS	General Packet Radio Service
GPS	Global Positioning System
GSM	Global System for Mobile Communications
HDLC	High Level Data Link Control
HTTP	HyperText Transfer Protocol
I/O	Input / Output
I/Q	In phase and Quadrature
I^2C	Inter-Integrated Circuit
I^2S	Inter IC Sound
IIR	Infinite Impulse Response

IP	Internet Protocol
ISO	International Organization for Standardization
ITU	International Telecomunication Union
LDN	Last Dialed Numbers
LDO	Low-Dropout
LED	Light Emitting Diode
LNA	Low Noise Amplifier
M2M	Machine to Machine
ME	Mobile Equipment
MIDI	Musical Instrument Digital Interface
MSB	Most Significant Bit
MSD	Moisture Sensitive Devices
MSL	Moisture Sensitivity Level
MUX	Multiplexer or Multiplexed
NOM	Network Operating Mode
NTC	Negative Temperature Coefficient
OSI	Open Systems Interconnection
PA	Power Amplifier
PBCCH	Packet Broadcast Control Channel
PCCCH	Packet Common Control Channel
PC	Personal Computer
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PCS	Personal Communications Service
PICS	Protocol Implementation Conformance Statement
PIXIT	Protocol Implementation Extra Information for Testing
PMU	Power Management Unit
PPS	Protocol and Parameter Selection
PSRAM	Pseudo Static Random Access Memory
RF	Radio Frequency
RI	Ring Indicator
RoHS	Restriction of Hazardous Substances Directive
RTC	Real Time Clock
RTS	Ready To Send
RX	Receiver
RXD	RX Data
SAR	Specific Absorption Rate
SAW	Surface Acoustic Wave
SCL	Serial Clock
SDA	Serial Data
SDN	Service Dialing Numbers
SIM	Subscriber Identity Module
SMA	SubMiniature version A connector
SMS	Short Message Service
SMTP	Simple Mail Transfer Protocol
STK	SIM Toolkit
SW	Software
TCH	Traffic Channel
TCP	Transmission Control Protocol
TDMA	Time Division Multiple Access
TS	Technical Specification
TX	Transmitter
TXD	TX Data
UART	Universal Asynchronous Receiver Transmitter
UDP	User Datagram Protocol
UL	Up Link (Transmission)
VCO	Voltage Controlled Oscillator
VSWR	Voltage Standing Wave Ratio
WA	Word Alignment

Related documents

[1] u-blox LEON-G100/G200 Data Sheet, Document No GSM.G1-HW-09001

[2] u-blox 2G GSM/GPRS AT Commands Manual, Document No GSM.G1-SW-09002

[3] GPS Implementation Application Note, Document No GSM.G1-CS-09007

[4] ITU-T Recommendation V.24, 02-2000. List of definitions for interchange circuits between data terminal equipment (DTE) and data circuit-terminating equipment (DCE). http://www.itu.int/rec/T-REC-V.24-200002-I/en

[5] 3GPP TS 27.007 - AT command set for User Equipment (UE) (Release 1999)

[6] 3GPP TS 27.005 - Use of Data Terminal Equipment - Data Circuit terminating; Equipment (DTE - DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS) (Release 1999)

[7] 3GPP TS 27.010 - Terminal Equipment to User Equipment (TE-UE) multiplexer protocol (Release 1999)

[8] The I2C-bus specification, Version 2.1, Jan 2000, http://www.nxp.com/acrobat_download/literature/9398/39340011_21.pdf

[9] CENELEC EN 61000-4-2 (2001): "Electromagnetic compatibility (EMC) - Part 4-2: Testing and measurement techniques - Electrostatic discharge immunity test".

[10] ETSI EN 301 489-1 V1.8.1: "Electromagnetic compatibility and Radio spectrum Matters (ERM); ElectroMagnetic Compatibility (EMC) standard for radio equipment and services; Part 1: Common technical requirements"

[11] ETSI EN 301 489-7 V1.3.1 "Electromagnetic compatibility and Radio spectrum Matters (ERM); ElectroMagnetic Compatibility (EMC) standard for radio equipment and services; Part 7: Specific conditions for mobile and portable radio and ancillary equipment of digital cellular radio telecommunications systems (GSM and DCS)"

[12] LEON Audio Application Note, Document No. GSM.G1-CS-10005

[13] Firmware Update Application Note, Document No GSM.G1-CS-09006

[14] GSM Mux Implementation Application Note for LEON-G100/G200 Document No GSM.G1-CS-10002

Part of the documents mentioned above can be downloaded from u-blox web-site (http://www.u-blox.com).

Revision history

Revision	Date	Name	Status / Comments
-	30/04/2009	tgri	Initial release. Objective specification
A	22/06/2009	lpah	New CI
A1	16/07/2009	tgr	Change of document status to advance information
B	20/08/2009	lpah	Figure 1.1 and Figure 1.2: corrected the LEON block diagram Figure 1.17: corrected the SIM Application circuit
			Document updated for serial port handling Table 1: renamed pins and description
			Chapter 1.9.1: added the figures related to DSR behavior at power-on, RI behavior at SMS Arrival, RI behavior at incoming call and CTS handling in power saving mode
C	4/11/2009	tgri/lpah/ssesteste/fves	Change of document status to Preliminary. Revision of 2.2.2 footprint and paste mask, 2.2.3 paste mask removed
			Section 1.5.2completely revised. Added Table 3, updated section 1.5.3.1 Section 1.5.4: added charging temperature range values with clarification Section 1.5.5: added clarification regarding V_BCKP current consumption; added formula to evaluate external capacitor capacitance requirement as function of the buffering time; updated application circuits. Updated Figure 17 Section 1.6.1: added Figure 19: Power on sequence description Section 1.6.2: added clarification regarding the application circuit to avoid an increase of the module current consumption in power down mode and added the power off sequence diagram Added Figure 20: Power off sequence description Section 1.6.3: added RESET_N equivalent circuit description Updated Figure 21: Application circuits to reset the module using a push button or using an application processor Section 1.10.1.3: clarified and updated application circuit description to connect a handset; added application circuit description to connect an external audio device with analog input/outputs; clarified and updated application circuit description to connect a headset. Added Figure 20. Section 1.10.1.5: clarified and updated application circuit description in hands free mode Section1.10.2: added clarification regarding the application circuit to avoid an increase of the module current consumption in power down mode. Section 1.8: clarified and updated application circuit description for the SIM card. Section 1.9.1: corrected MAX3237 description; added clarification regarding the application circuit to avoid an increase of the module current consumption in power down mode. Section 1.10: clarified as the measured value is input impedance dependent Section 1.12: added clarification regarding the application circuit to avoid an increase of the module current consumption in power down mode. Updated section 2.1: Check UART signals direction, since the signal names follow the ITU-T V.24 Recommendation. Added section 2.3 to explain module thermal resistance. Section 1.9.1: corrected supported UART frame format. Corrected and improved description Updated and improved Figure 3: Power supply concept Added VCC extended and normal operating ranges description and clarified DC power supply requirements in section 1.5.2 Updated and improved Figure 7 content and caption Clarified current profile description in section 1.5.3.2 Updated and improved content and caption Clarified charger requirements in section 1.5.4 Grouped sections Module power on, Module power off, Module reset into the 1.6 System functions chapter Updated and improved Figure 19: Power on sequence description Updated and improved Figure 20: Power off sequence description Updated Figure 37: Headset mode application circuit content Clarified I2S PCM mode path in section 1.10.2.1 Updated section 1.9.1: clarified, added and corrected UART features, UART signal behavior,. Updated and improved UART signal behavior (AT commands interface case) content and caption Updated Figure 25: UART default frame format (8N1) description caption Deleted the double repeated point in the Design-in checklist Clarified pins arrangement in section 2.2.1 Clarified ground plane requirements in section 2.2.1.4 Renumbered sections Antenna termination, Antenna radiation, Antenna detection functionality Corrected AT Commands Manual code in Related documents section Removed “System Configuration” chapter
D	01/29/2010	lpah	Improved audio interfaces and updated approvals chapter
E	22/04/2010	lpah	Aligned the document to LEON-G100-04S-00 and LEON-G200-04S-00 Digital Audio Interface supported by LEON-G100
F	08/07/2010	lpah	Aligned the document to LEON-G100-05S-00 and LEON-G200-05S-00
F1	30/07/2010	lpah	Added more details on Additional hints for the VCC supply application circuits

Revision	Date	Name	Status / Comments
F2	13/08/2010	lpah	Updated soldering profile information
F3	20/01/2011	lpah	Updated stencil information and inserted the application circuit for LEON-x00-06x UART Power saving description added; improved the description of serial line handling

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