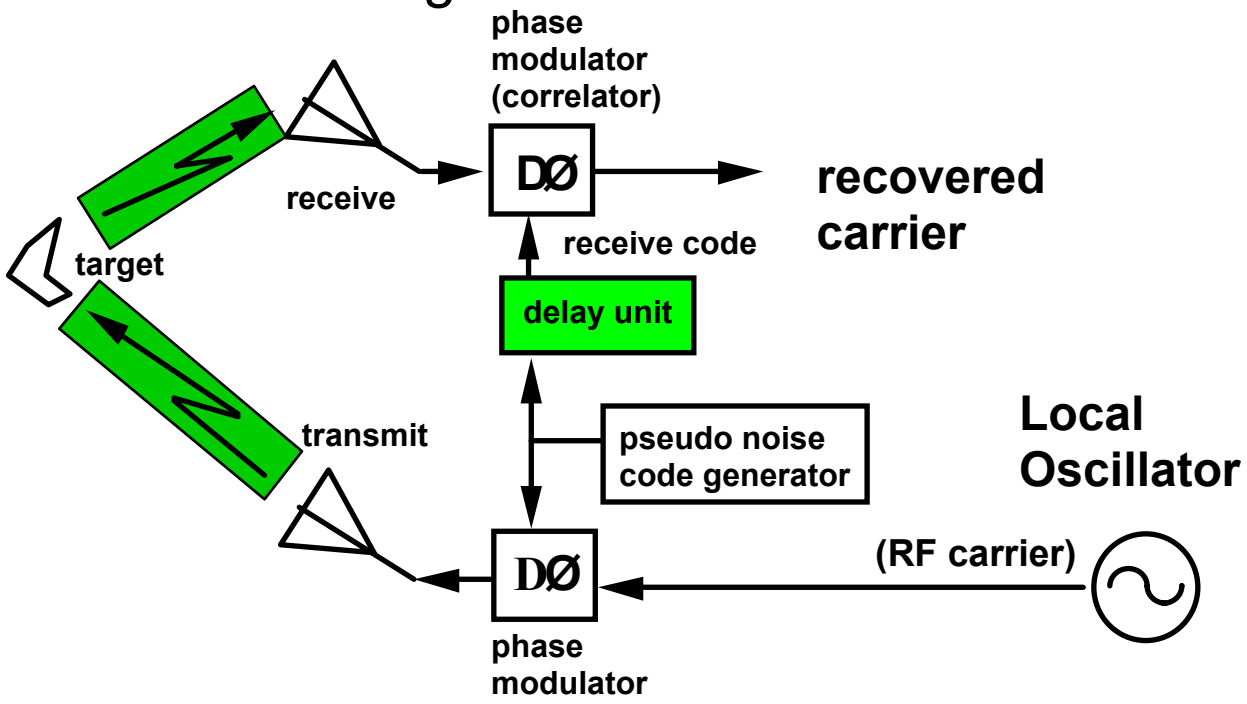
Principles of Operation

- Architecture & Block Diagrams



When the internal delay of the receive code matches the time of flight to target and back, receiver output is at a maximum as governed by return target signal power

Microwave Oscillator/Multiplier Frequencies Block Diagram

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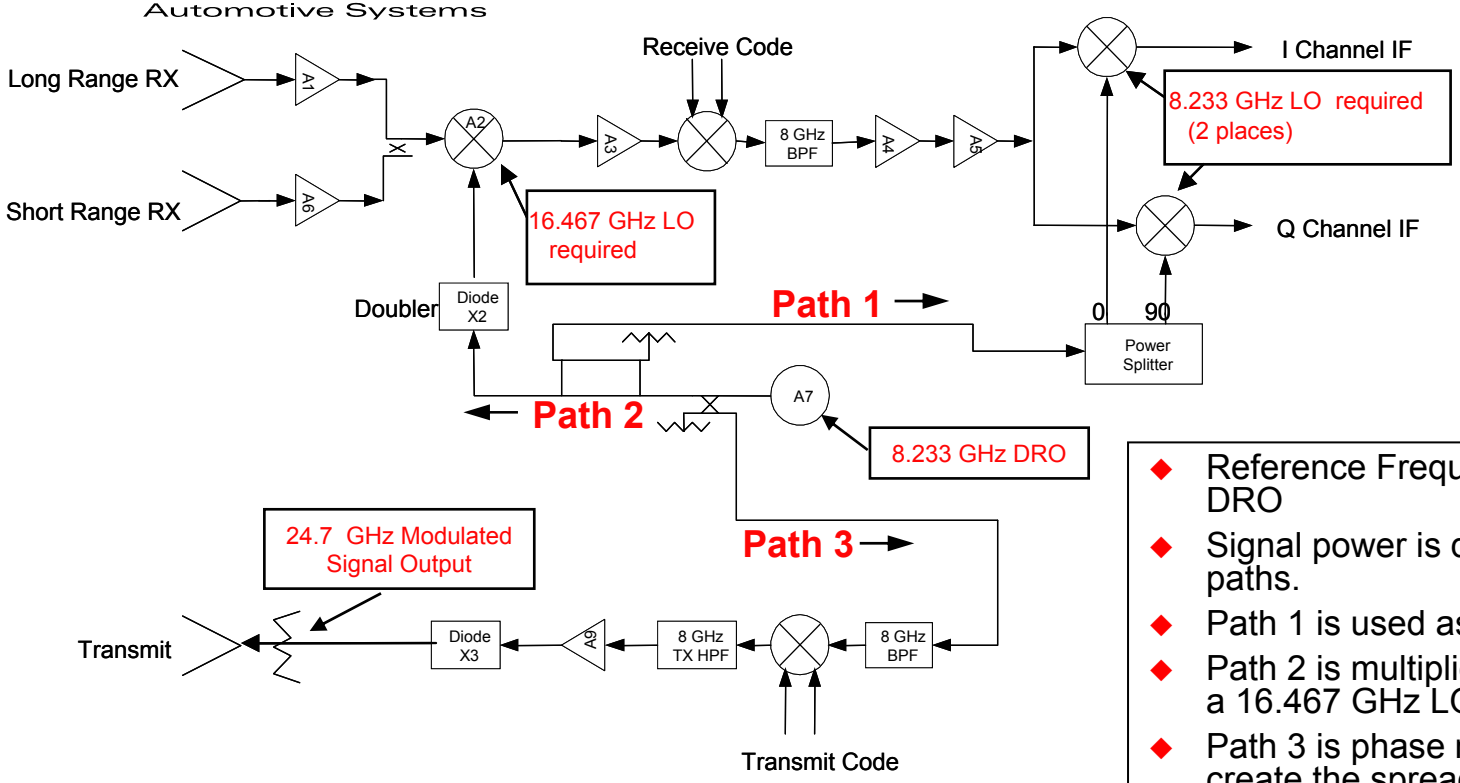

- Reference Frequency is 8.233 GHz DRO
- Signal power is divided into three paths.
- Path 1 is used as an 8.233 GHz LO
- Path 2 is multiplied x2 and used as a 16.467 GHz LO
- Path 3 is phase modulated to create the spread spectrum signal
  - phase modulation suppresses the carrier to zero amplitude with theoretically perfect diodes
- Path 3 spread spectrum signal is then amplified and multiplied x3 to create the transmitted 24.7 Ghz spread spectrum signal

Digital Circuitry Oscillator/Multiplier Frequencies Block Diagram

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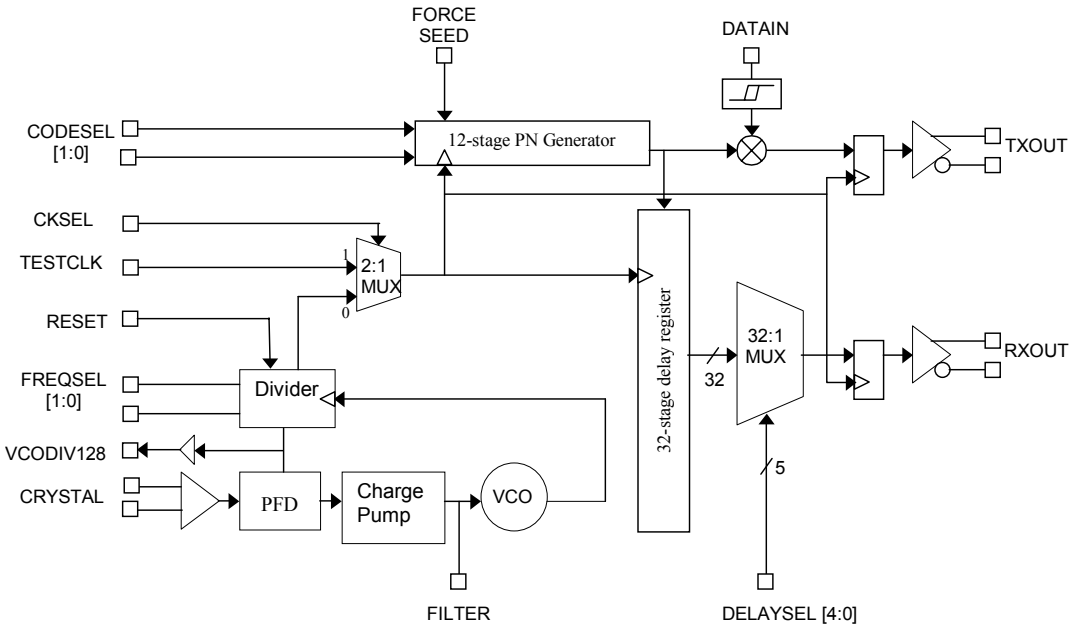

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Operating frequency range (internal CLOCK)	F_{clock}	1230	1250	1270	MHz
CLOCK jitter (RMS)	J_{ck}		20	50	ps
DATA input frequency	F_{data}	.001		20	Mhz
TRANSMIT/RECEIVE output skew (nominal)	T_{skew}	-320		320	ps
Output skew variation	T_{var}	-200		200	ps
Output rise time	T_{rise}		10	150	ps
Output fall time	T_{fall}		10	150	ps
TRANSMIT output leakage (RMS)	L_{TC}		tbd		dbV
RECEIVE output leakage (RMS)	L_{RC}		tbd		dbV

- The pseudo noise code generator ASIC has an onboard oscillator referenced to an external crystal.
- Internal clock frequencies used in the PN codes are x8, x16, x32, x64 multiples of the crystal reference (all multiplication circuits are on ASIC)
- External 19.53125MHz crystal is required