DUTY CYCLE CORRECTION FACTOR, CALCULATIONS COPIED FROM REPORT:

For a graphical presentation of the data bursts being transmitted from the transmitter, refer to Appendix C. for a zero span picture of the modulation burst from one representative unit. Plots are provided that show the repeating burst of data that occurs when a key is held down continuously, and also over a 250 millisecond (worst case) period and a 20 millisecond period, to display the individual pulses in detail.. The Data is Pulse Position modulated. When the total On-time is computed over a100 millisecond window, according to FCC Part 15.35(c), where the packet duration exceeds 100 milliseconds, a total of 22.87 milliseconds is obtained. This results in a relaxation factor of 12.8 dB, which is under the allowable cap of 20 dB, as stated in FCC Part 15.35(b)

The construction of the entire data packet is as follows:

Portion	duration	max on-time
Preamble:	175 ms.	29.167 ms
Header :	8 ms.	1.67 ms.
Data:	70.4ms	17.6 ms
Total	253.4ms	48.43ms

Selecting the worst case, 100 millisecond window, which is found to be the end of the packet:

Portion	duration	max on-time
Preamble:	21.6 ms.	3.6 ms
Header :	8 ms.	1.67 ms.
Data:	70.4ms	17.6 ms
Total	100 ms	22.87 ms

Relaxation Factor= 20 log (22.87/100)

= 12.8 dB

ADDITIONAL INFORMATION REGARDING DUTY CYCLE CORRECTION FACTOR:

For the pulse position modulation scheme:

A logic "0" is defined by a 0.2 millisecond wide pulse, followed by a 0.6 millisecond dead time. (25% on)
A logic "1" is defined by a 0.2 millisecond wide pulse, followed by a 1.0 millisecond dead time. (16.6% on)

The Preamble consists of 146 bits, all of the bits are logic "1"s, for a total length of 175.2 ms
The Header consists of 8 bits, 4 are logic "1" and 4 are logic "0", for a length of 8 ms.
The Data consists of 88 bits, which are mixed "0"s and "1"s. All "0"s results in 70.4 ms length.

Since this is a pulse position modulation scheme, and because the third section of the packet can vary in composition, the total length can vary from about 250 ms. to 288 ms. For the calculation presented in the report, and reiterated above, the worst case packet, where the bits in the data section are all set to be a logic "0", was utilized.

On the following pages can be found a number of oscilloscope traces, showing greater detail of the data packet construction of a sample keyfob. These were created by connecting the oscilloscope input to the video (baseband, or detected) output of a spectrum analyzer. The transmit signal from the sample was picked up by a near field probe, (Emco H-field loop) and coupled into the spectrum analyzer input. The keyfob transmitter button was then depressed, and the resulting data packet was captured in the oscilloscope memory, and resultant close-up scans were directly transferred to disc, and imported as .TIF files to this document.

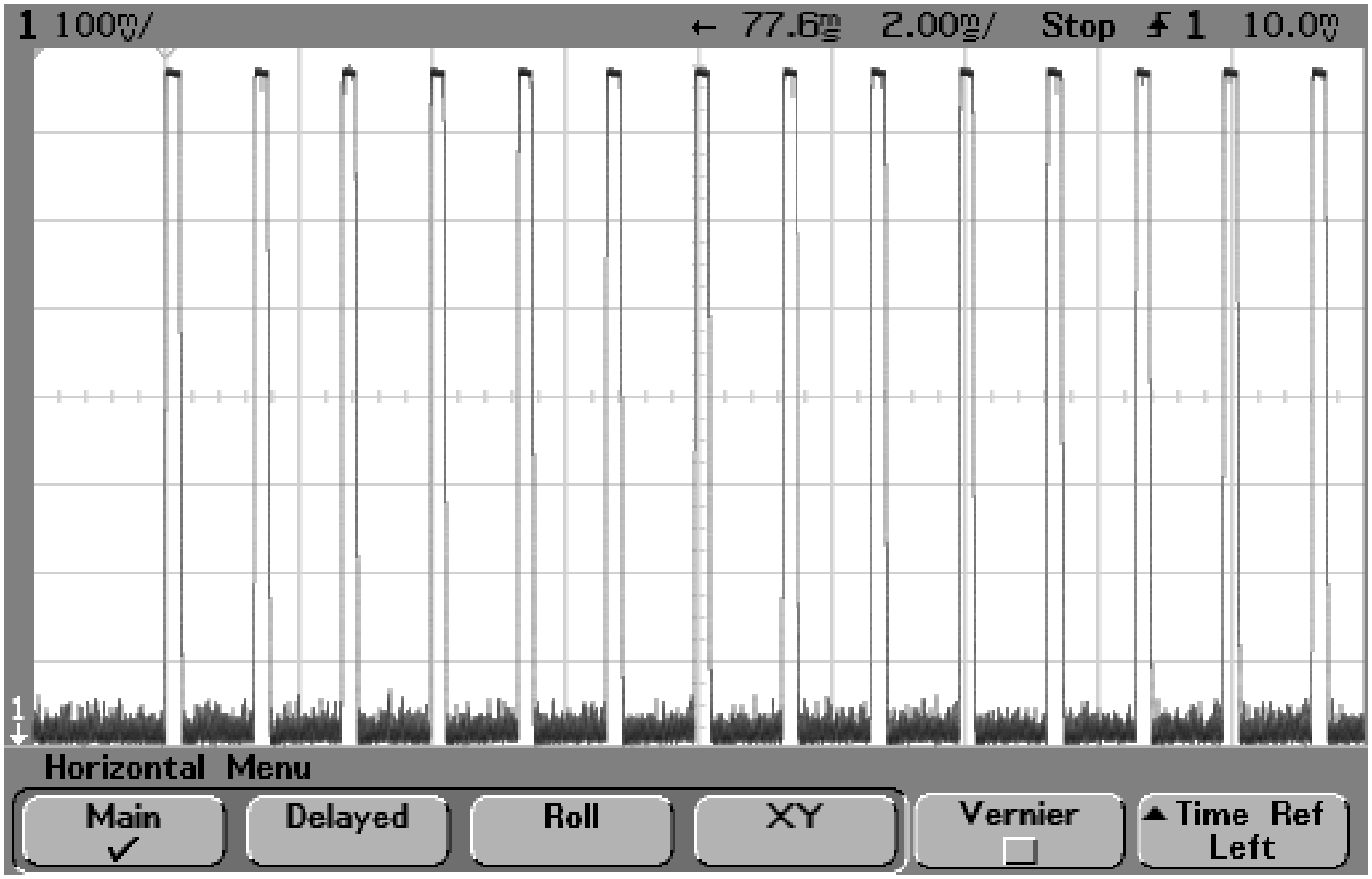
There are two things to keep in mind:

1. The timing, or clock in the transmitter is RC based, and is not exact, and can drift, which will effect the on-times and off times.
2. The packet details shown are for a typical sample, and do not represent the worst case. This means that the data section, which is the last 88 bits, are a combination of logic "0"s and logic "1"s, which will cause the length of this section to increase beyond 70.4 ms.

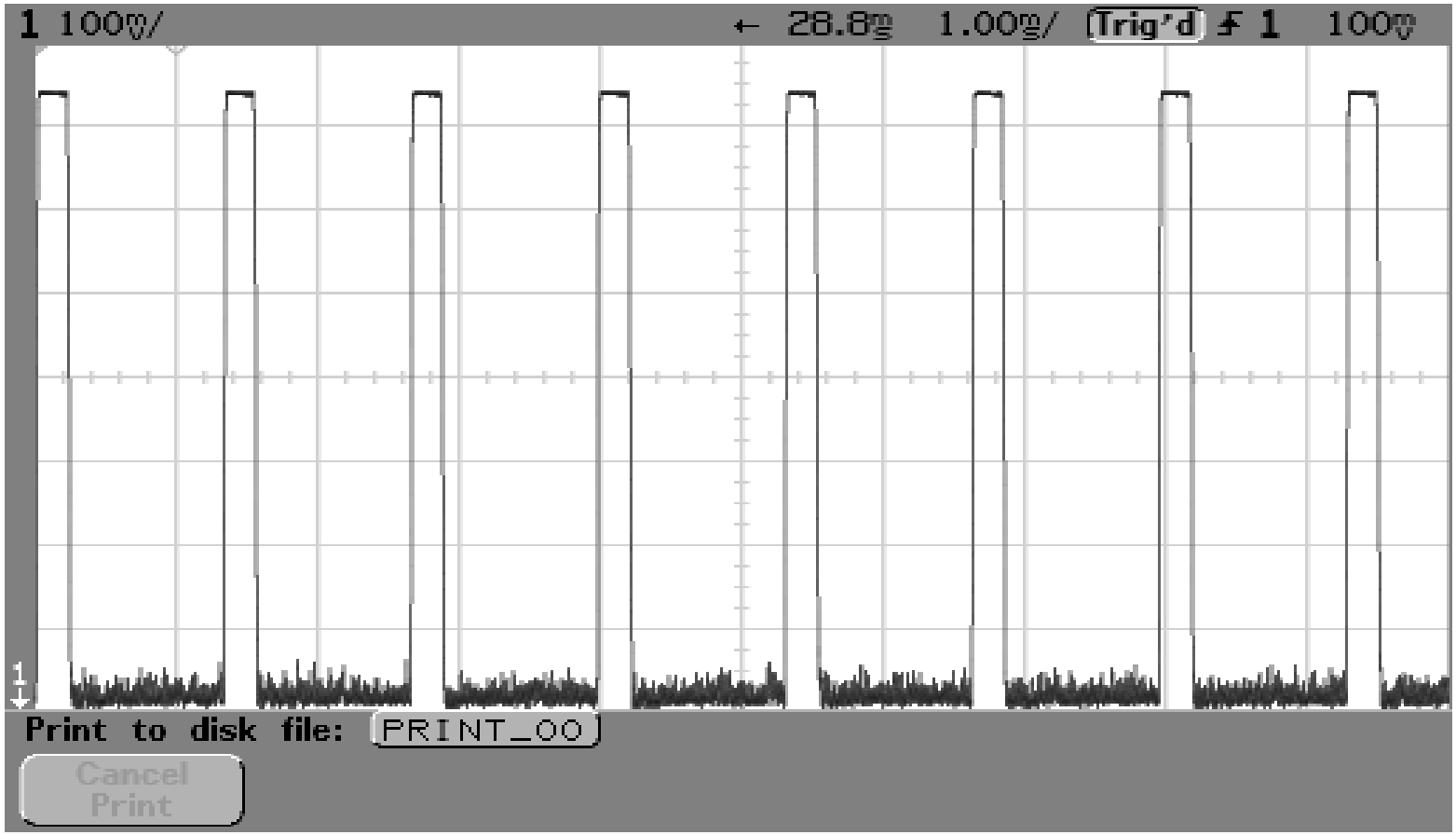
The general effect of this is to cause the duty cycle to vary by a few percent, but in the general direction of a lower duty cycle than that derived in the calculations. The packet shown in detail in the following graphs is about 290 milliseconds long, which illustrates the effect of both of the above mentioned variable parameters.

View of the Agilent (HP) model 54624A 100 MHz digital oscilloscope; HP 8591EM spectrum analyzer; and EMCO 7405-901 6 centimeter H field probe, used to create the data packet detail plots.

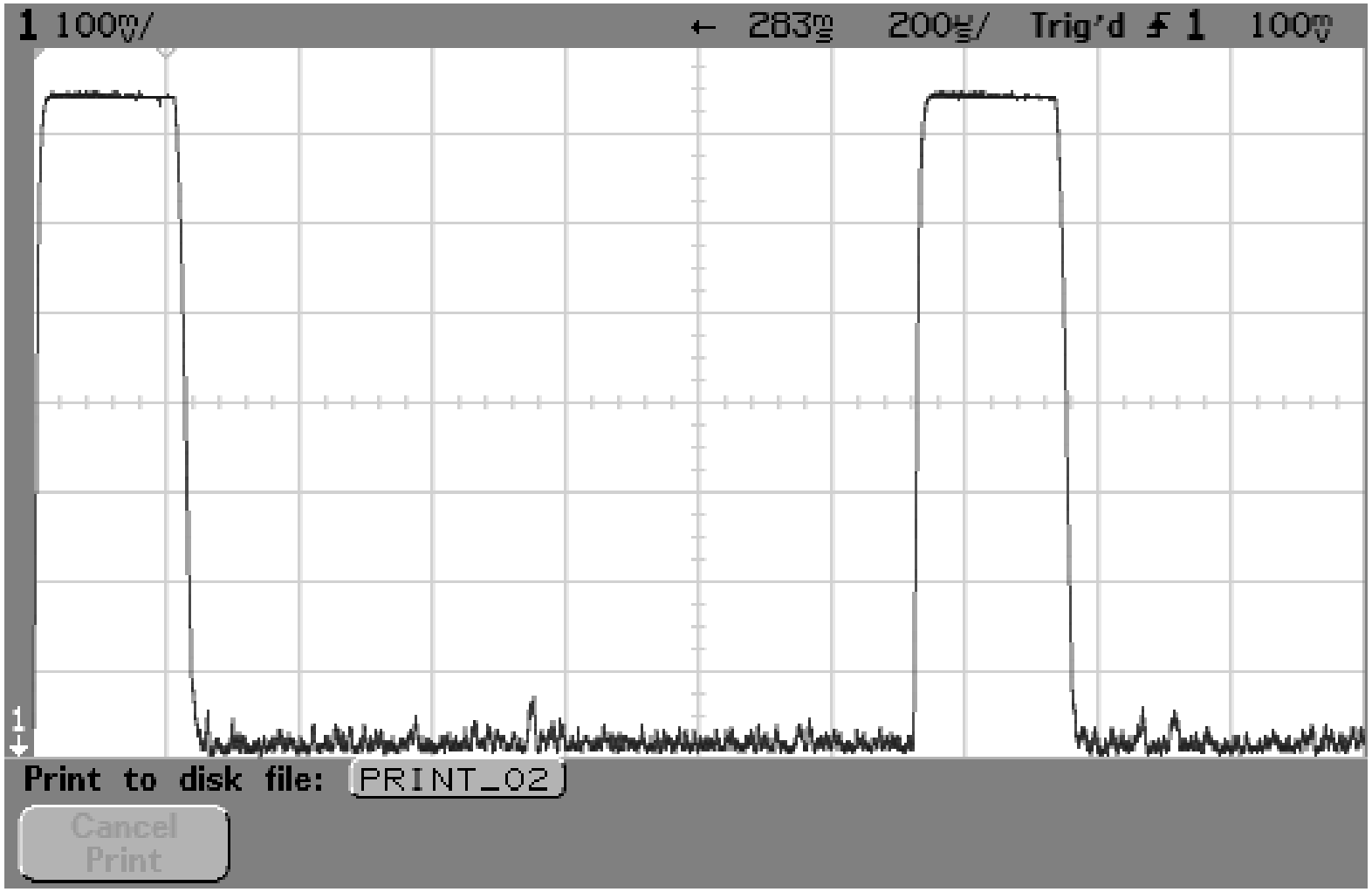
20 millisecond window, showing detail at front of the packet transmission, (start of packet occurs 1 cm from left)



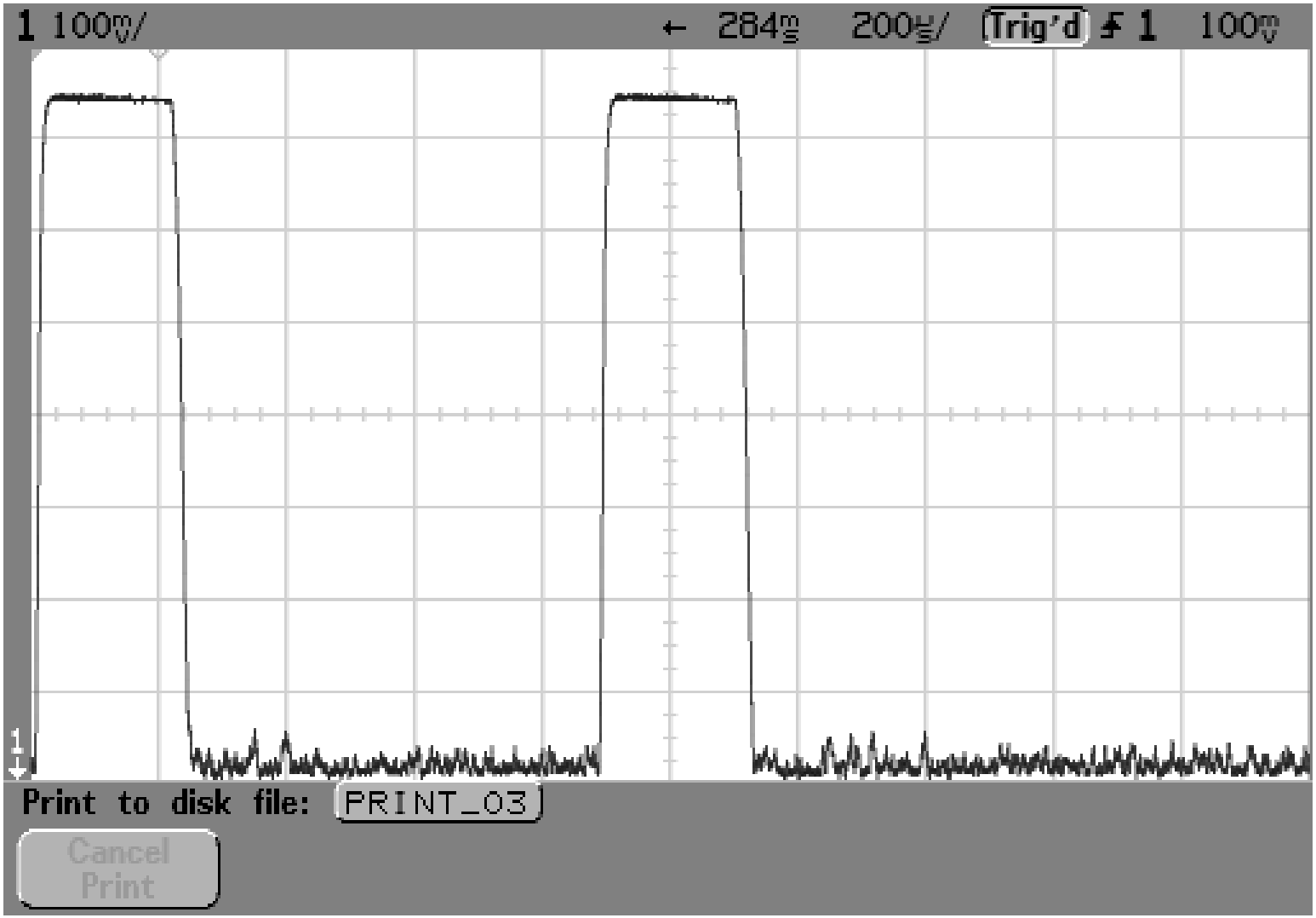
10 millisecond window, showing detail at front of the packet transmission



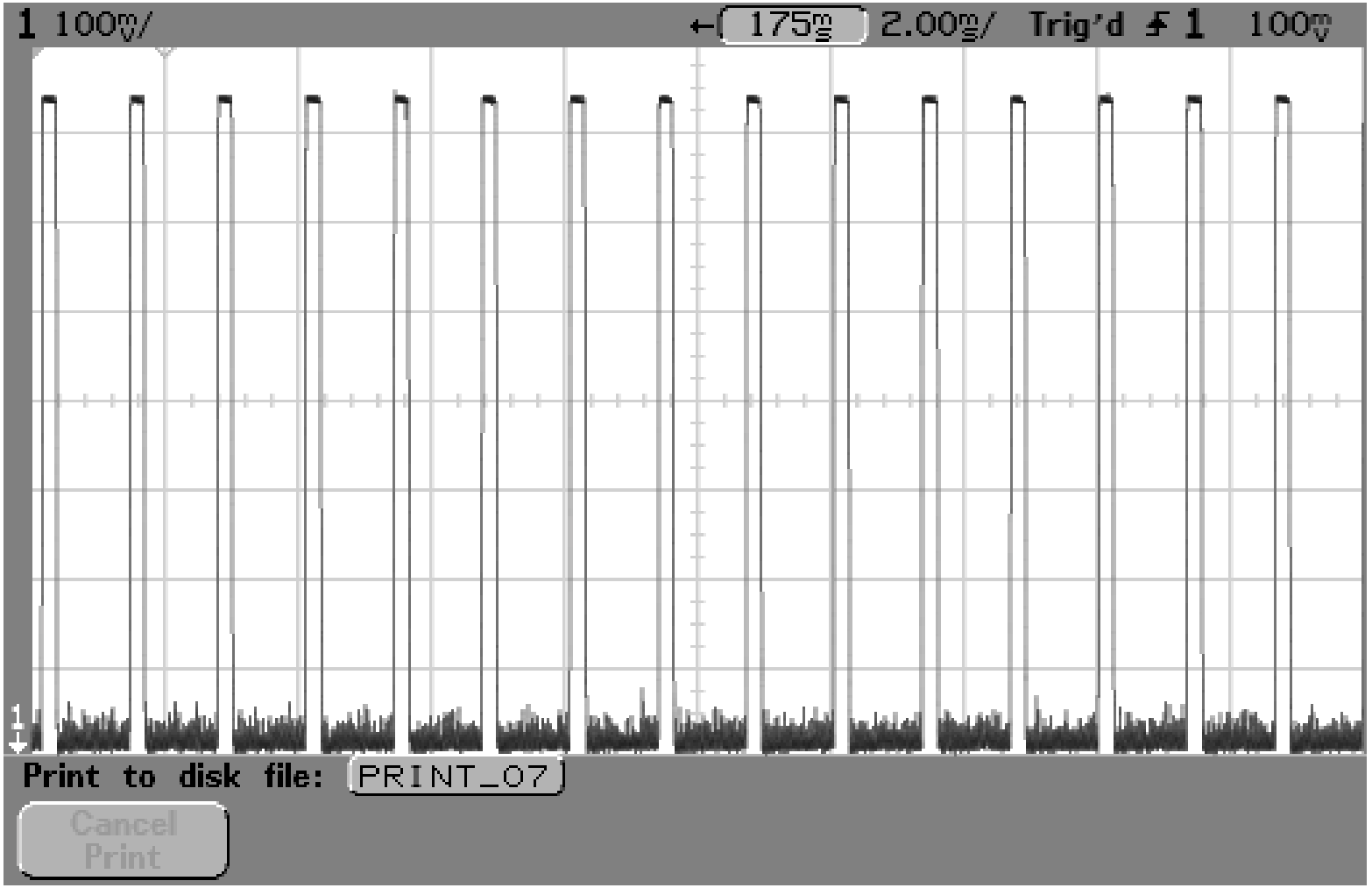
2 millisecond window, showing detail from near back end of the packet transmission, logic "1" detail



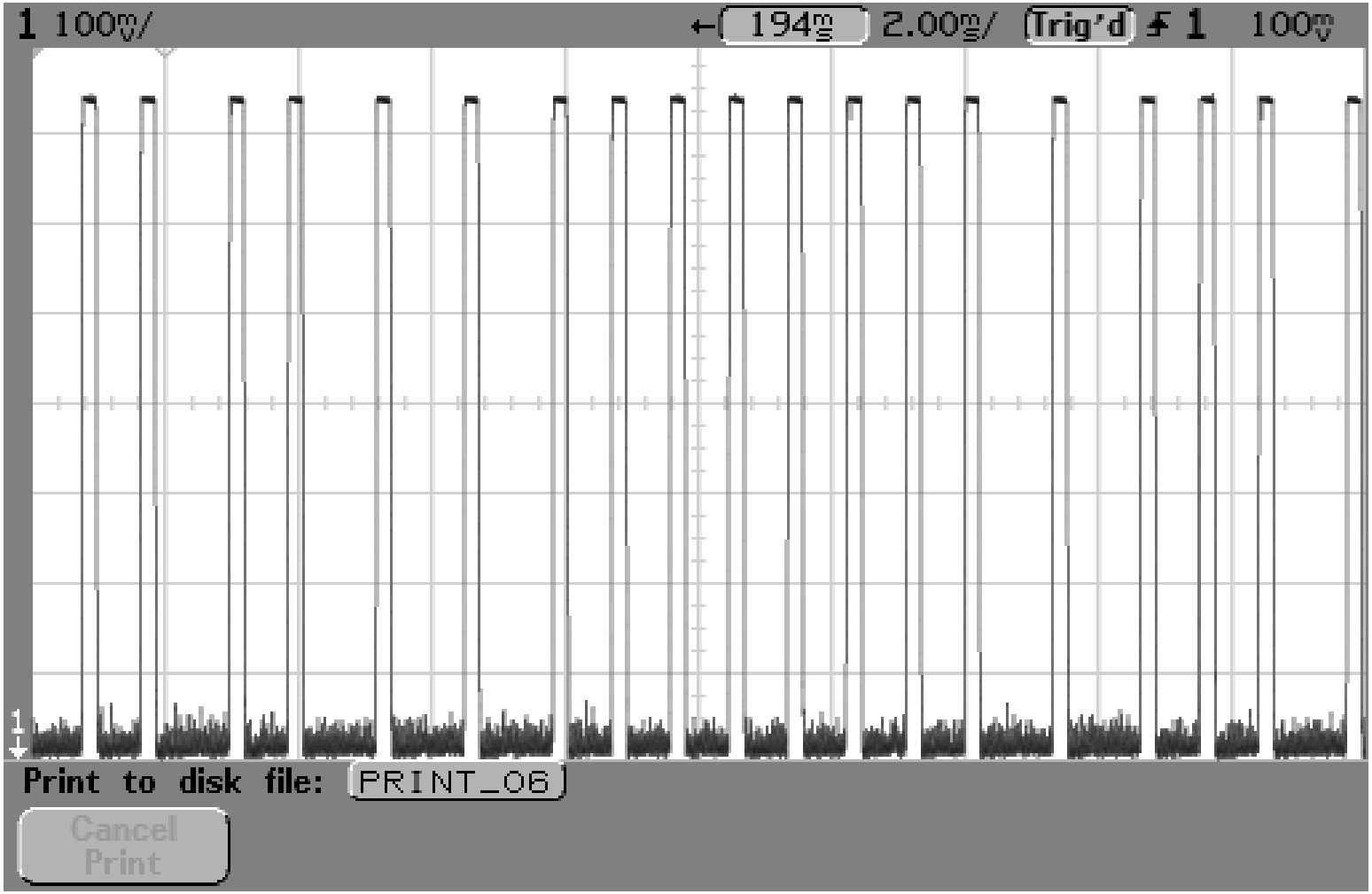
2 millisecond window, showing detail from near the back end of the packet transmission, logic "0" detail



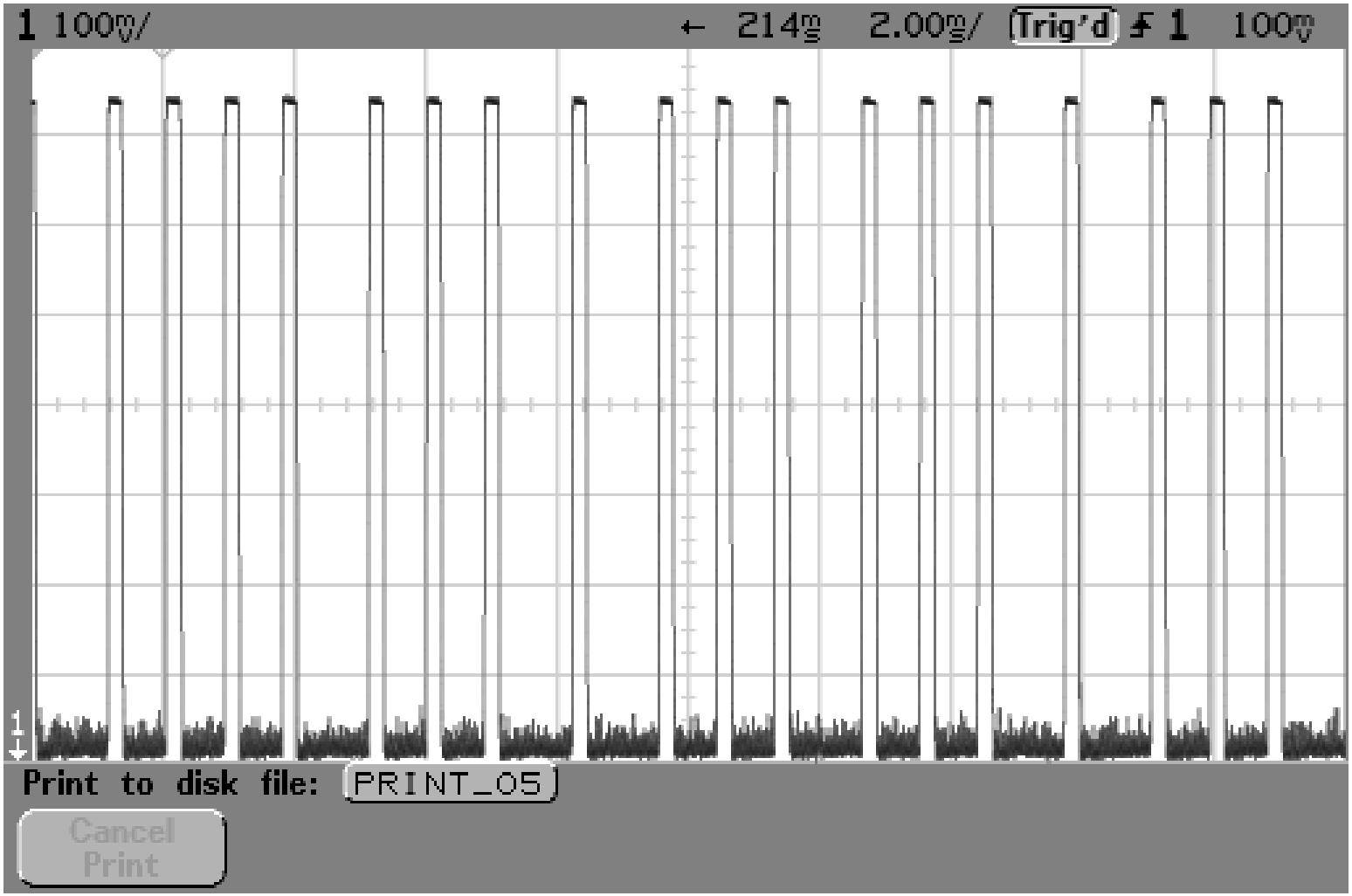
20 millisecond window, showing detail at middle of the packet transmission, 120ms to 100ms from the back end.
All pulses here and ahead of this point in the packet are identical and are part of the preamble. (logic 1)



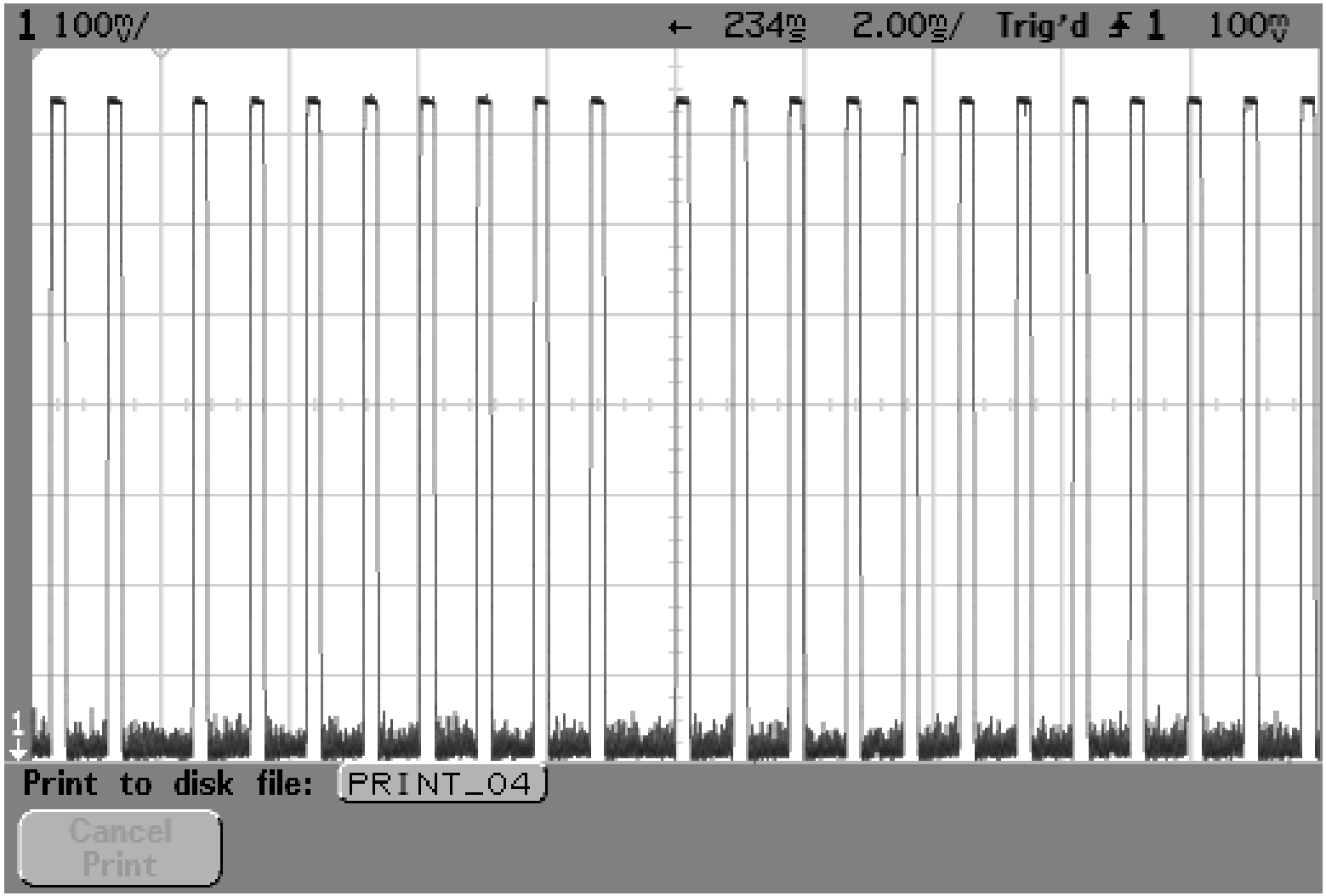
20 millisecond window, showing detail at middle of the packet transmission, 100ms to 80ms from the back end.
The first eight pulses on the left of this screen are the header, all subsequent pulses comprise the data.



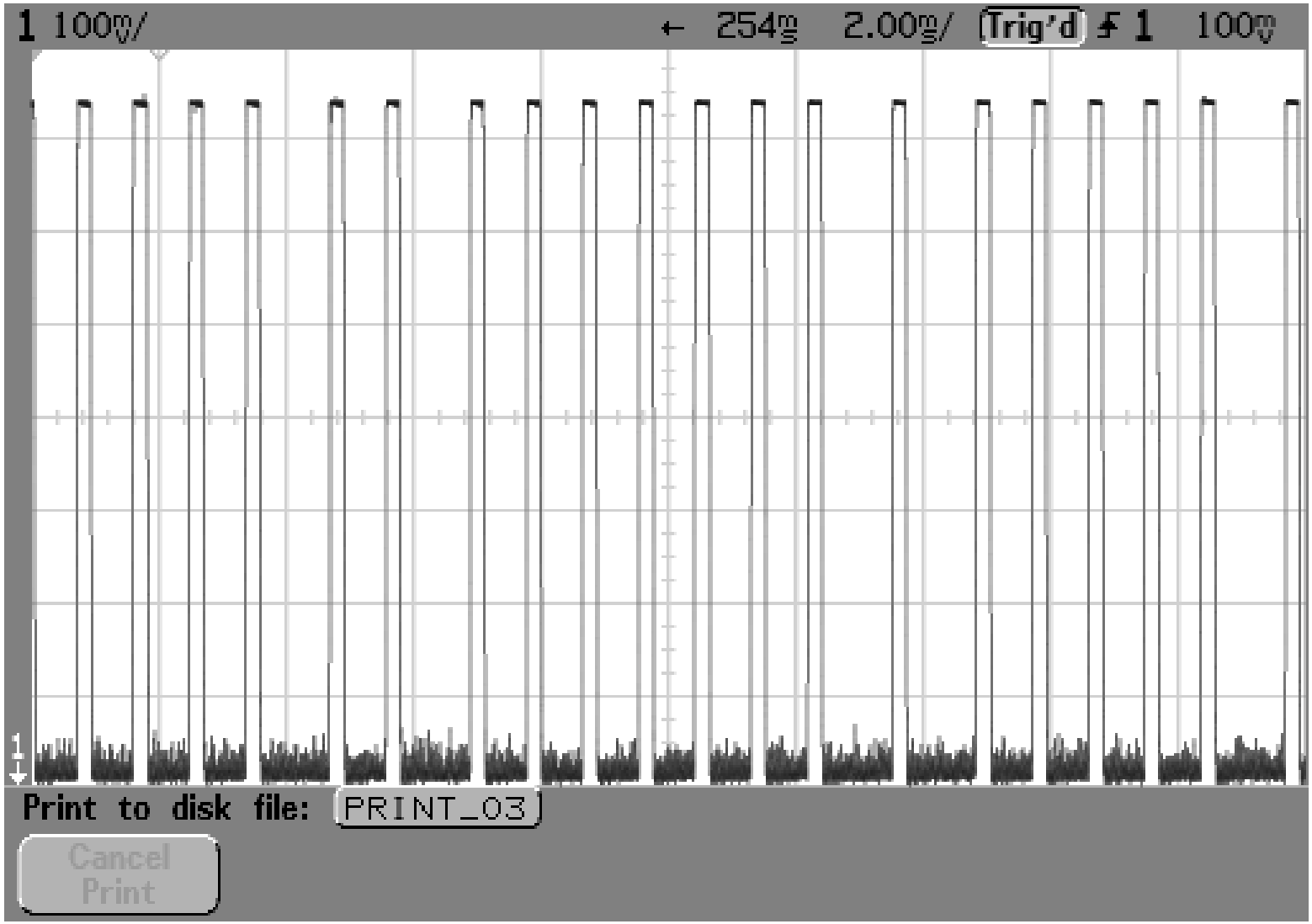
20 millisecond window, showing detail near the end of the packet transmission, 80ms to 60ms from the back end.



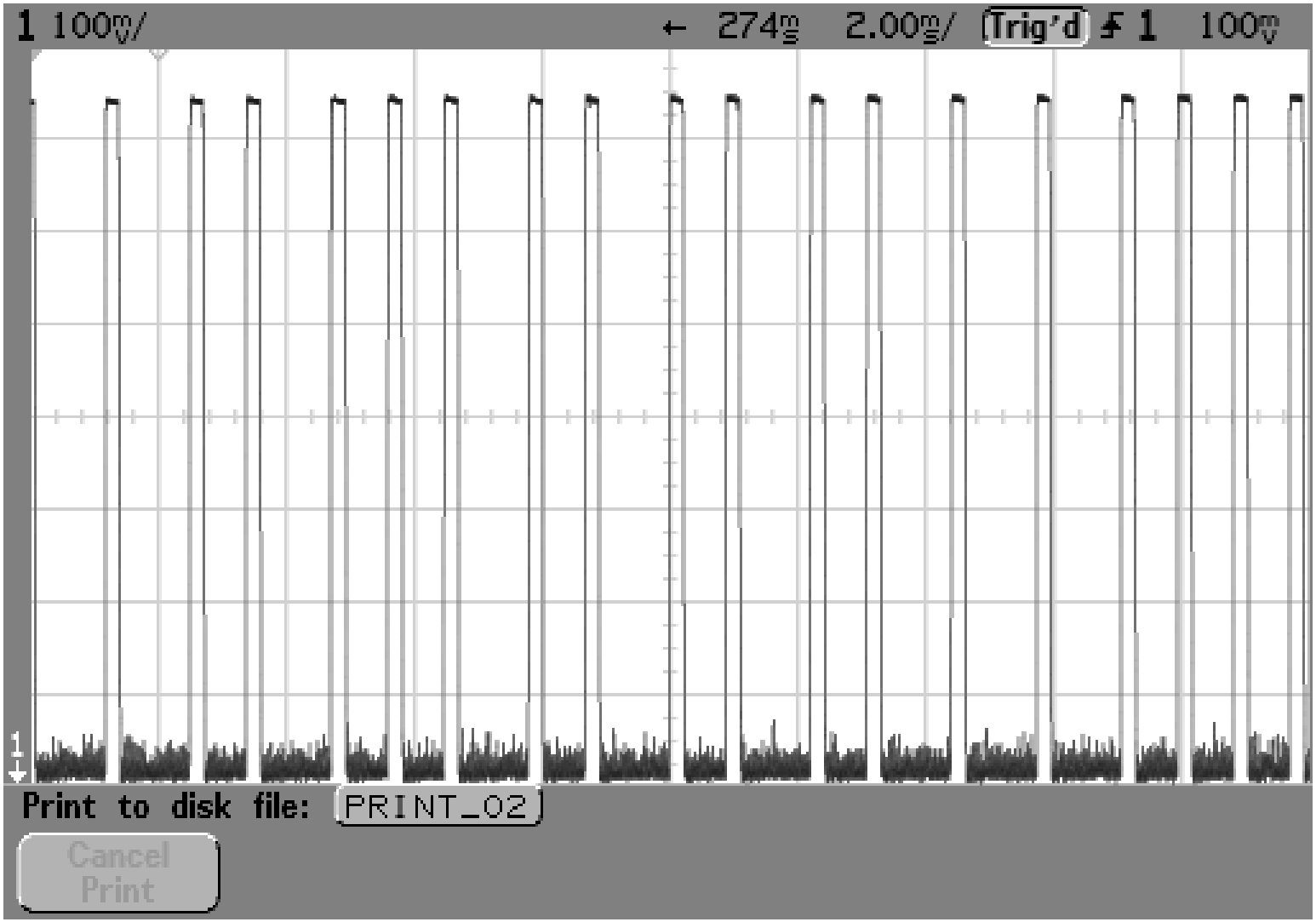
20 millisecond window, showing detail near the end of the packet transmission, 60ms to 40ms from the back end.



20 millisecond window, showing detail near the end of the packet transmission, 40ms to 20ms from the back end.



20 millisecond window, showing detail at the end of the packet transmission, 20ms to 0ms from the back end.



50 millisecond window, showing detail near the end of the packet transmission, 50ms to 0ms from the back end.