Operational Description - Z100S1 – Aerocomm's Family of High Power Zigbee Radios

Overview

The Z100S1 is an IEEE compliant 802.15.4 Zigbee transceiver. It operates at +18dBm conducted transmit power and has the option to use either an integral chip antenna or an external dipole connected by a u.fl RF connector. The module is solderable and is meant to be integrated into our OEM customers equipment as a reliable low power 2.4Ghz mesh network option.

The Texas Insrtruments CC2430 is the RF engine and processor for **Z100S1** and uses the ZigBee protocol stack, a network layer protocol which uses small, low power digital transceivers based on the IEEE 802.15.4 hardware standard. The ZigBee layer is the software layer that sits atop the 802.15.4 PHY/MAC layer and performs all packet routing and mesh networking.

The Z100S1 can be as a Coordinator, Router, or End Device in a Zigbee mesh network. The Coordinator is the first device to be powered up; when powered up the Coordinator scans to find an available channel and establishes a network. Routers/End Devices which are powered up after the Coordinator establish the network, and periodically send beacons looking for a Coordinator, which subsequently assigns them a unique 16-bit Network Address.

Receiver Hardware

TI's CC2430 is an IEEE 802.15.4 compliant radio. The CC2430 features a low-IF receiver. The 2.4Ghz RF signal comes into the Z100S1 from the antenna and is received by the front-end module which passes it through a low noise amplifier and out the receive port. Data then reaches a balun which introduces the data to the differential input / outputs of the CC2430. It is amplified again and down converted in quadrature (I and Q) to the intermediate frequency (IF). At IF (2MHz), the complex I/Q signal is filtered and amplified, and digitized by the RF receiver ADCs. Automatic gain control, final channel filtering, de-spreading, symbol correlation and byte synchronization are performed digitally. An interrupt indicates that a start of frame delimiter has been detected. CC2430 buffers the received data in a 128 byte receive FIFO.

Transmitter Hardware

The CC2430 transmitter is based on direct up-conversion. Data is buffered in a 128 byte transmit FIFO (separate from the receive FIFO). The preamble and start of frame delimiter are generated in hardware. Each symbol (4 bits) is spread using the IEEE 802.15.4 spreading sequence to 32 chips and output to the digital-to-analog converters. An analog low pass filter passes the signal to the quadrature (I and Q) up conversion mixers. The RF signal is amplified internally by the CC2430's power amplifier and fed out to the balun and passed to the front-end module where it is amplified again. It passes out the transmit port and is fed through a low pass filter to reduce the 2^{nd} and 3^{rd} harmonics and passed out through a 2.4GHz antenna.