TECHNICAL DESCRIPTION FOR MP16 224 MHz VERSION

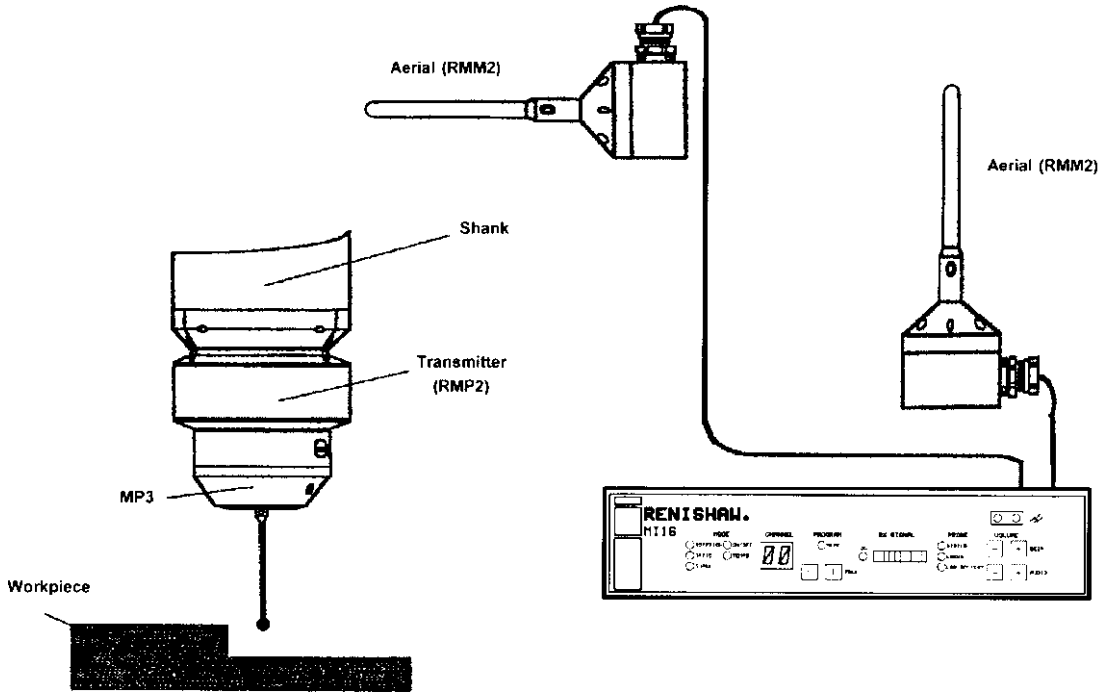
Part Number
H/2137/0131

RENISHAW

FCC codes:
KQG RMP2-224
KQG MI16-224

I. GENERAL DESCRIPTION

The radio probe MP16 made by RENISHAW is a non line-of-sight probing system designed to equip numerical controlled machine tools with in cycle measuring equipment.The installation comprises a probe (RMP2), two antennas (RMM2) and an interface (MI16).



II. RADIO PROBE DESCRIPTION

A. ANTENNA (RMM2)

The antennas are ¼ wavelength tuned and earth plane units with about 0.5 MHz bandwidth and a good VSWR of 1.2. The base is insulated and the grounding is made by capacitance to the machine body. A common problem has been seen of sympathetic radiators in machines, which lead to signal nulls. Sympathetic radiators are parts of machines which are also ¼ wavelength long or thereabouts; these receive and re-radiate the RF signal which can cause field cancellation and loss of signal.The use of two antennas and corresponding circuitry will correct this problem.

B. PROBE (RMP2)

1. GENERAL DESCRIPTION

The probe is assembled as a series of 3 PCB's, one with a RF transmitter module. The other boards contain the reference clock, the tracking probe interface, the set-up module, the switch and the power supply.

The method of operation is as follows. Two frequencies are derived from a 4 MHz crystal oscillator at nominally 500 and 1000 Hz, the 500 Hz is transmitted as a time reference to the modulation on the 1000 Hz. In the receiver the 500 Hz is used to synchronise a clock and regenerate a 1000 Hz for demodulation of the signal. On a probe change of state the time since the last 1000 Hz pulse is latched as an 8 bit word giving a resolution of 256. A start bit, a parity bit and a stop bit are added, and the information is sent as phase modulation on each cycle of the 1000 Hz carrier over the next 11 ms to the receiver. This decodes the time interval and adds it to the transmission frame time to give a precise delay from probe change of state to interface output change with an accuracy of around 4µs. The probe status (trigger or reseat) is carried by the fundamental modulation of the 1000 Hz carrier : in phase or antiphase. The low battery status information is sent as a 125 Hz signal.

An infrared link exists to set-up the probe channel and its mode. It operates in the following modes:

- Start by rotation and stop by rotation
- Start by rotation and stop by time out
- Start and stop by a shank switch
- Optical start and stop
- Optical start and stop by time out

2. POWER SUPPLY PCB

Six AA batteries supply a voltage of 9V to the input of a step-down switching regulator.

3. LOGIC AND INTERFACE PCB

This unit has a probe contact tracking interface and a high voltage generator, which together enhance the reseat performance of the probe.

A FPGA (Field Programmable Gate Arrays) contains the following logic:

- Probe contact debounce
- Clock divider
- 8 bits counter
- Parity generator
- Shift register
- Phase inverter generator.

The modulation frequencies are generated from a Walsh generator (stepped sine wave synthesis, using the shift register as ring counters). The 1000 Hz is phase modulated by inverting the output of the ring counter. In the same way a 125 Hz sine wave is generated when the batteries are below 6.5 V. The sine waves are combined in a low pass filter and sent to the transmitter. A PIC (Programmable controller) is used to control the programming of the mode and the channel by the infrared link.

4. TRANSMITTER 224 MHz

The transmitter operates at a nominal 224 MHz, the precise frequency set by 40 synthesised channels, spaced at 25 KHz intervals. The first channel is set to 224,5 MHz and the last to 225,475 MHz.
The reference clock for the synthesiser (UMA 1017) is 8 MHz. The output of the internal phase comparator controls the frequency of a voltage-controlled oscillator (VCO) with a varicap diode.

C. INTERFACE (MI16)

1. DESCRIPTION

The interface comprises a double receiver allowing diversity reception. Each receiver uses a double conversion system with a common local oscillator. The logic selects the strongest signal automatically.
Three switched capacitor filters are used to separate the frequencies of the demodulated signal, a highpass for the 1000 Hz, and bandpass for the 500 Hz and 125 Hz.
The 500 Hz is used in a phase locked loop (PLL) frequency multiplier to generate a 250 KHz reference clock. The VCO voltage in the PLL is held during the reception of a word to reduce the residual FM, and hence the timing errors.

A FPGA (Field Programmable Gate Arrays) contains the following logic:

- Clock divider to generate a second 500 Hz frequency for the PLL phase comparator
- 1000 Hz decoder

- Down counter to generate the additional part of the delay
- Parity check
- Error detection
- Status bit generation

The IF detector has a signal strength output which is fed to a bar graph driver to give a visual indication of signal strength. An error output is created if the received RF is too low.
An amplitude comparator detects the 125 Hz presence and generates a low battery bit.

The front panel displays:

- The channel number
- The probe mode
- The status mode
- The received signal strength
- The low battery information

2. RECEIVER MODULE

- A circuit SA601 includes a low noise amplifier (LNA) and a mixer. The output of the LNA is mixed with a synthesised signal around 204 MHz to deliver an IF signal at 21.4 MHz.
- The synthesiser used is a UMA 1017. The first local oscillator delivers a frequency of 203,1MHz for the first channel and 204,075 MHz for the last.
- A second frequency change is made using a built in detector (MC3371 Motorola). The RF portion is tuned to 21.4 MHz with a standard 21.4 MHz crystal filter. This frequency is converted to 455 KHz by a local oscillator, and passes through a narrow band pass ceramic filter for the spacing channel.

3. Filters

The following switched capacitor filters are used: 500 and 125 Hz bandpass and 1000 Hz highpass. The centre frequencies and relative phase shifts are set by a 50 KHz oscillator which is tuned by a trim pot.

4. RX VCO

This generates the 250 KHz clock for the precision time delay. The circuit is a conventional PLL frequency multiplier with the addition of special sample and hold circuitry to reduce the phase jitter during decoding. This improves the delay variation from 25µS to 10 µS.

5. FPGA

Inside the FPGA the 250 KHz is divided to generate a 500 Hz signal for the VCO phase comparator and a 1000 Hz to latch the received 1000 Hz signal into a serial to parallel shift register. The shift register loads data continuously, and the word reception sequence is triggered by a change of state in the MSB, which is the probe status, the word is loaded into a down counter to create the additional delay. If the parity check detected is bad, the logic is inhibited, the probe output forced to an open state, and an error signal set.

6. FRONT PANEL

The front panel is equipped with:

- A channel display
- Two programmation buttons "+" and "-"
- Five LED's indicating the type of start and stop method.
- Two infrared LED's for an optical link to set-up the probe channel and its mode.
- An LED « MEMO » used during the set-up.
- A bargraph to display the RX signal strength.
- Three LED's for probe status, error detection and low battery information.
- Four switch buttons to adjust the volume of the loudspeaker. Two for the received audio signal and two for the probe status beep.

The two switch buttons "+" and "-" are used for programming:

- Push "+" or "-" to select a higher or lower channel (1 to 40)
- Push the two together to change the probe mode.

Five probe modes are selectable:

- « ROTATION-ON/OFF » Start and stop by rotation which is detected inside the probe by a centrifugal switch.
- « ROTATION-TEMPO » Start by rotation and stop after a 3 mn time out.
- « SHANK-ON/OFF » Start and stop by a shank switch.
- « OPTIC-ON/OFF » Start and stop by an optical signal.
- « OPTIC-TEMPO » Optical starts and stops after a 3 mn time out.