DATA SHEET

CD1536X
Television tuner for analog and digital cable applications

1999 Jan 18

Preliminary specification
File under Tuners, DC03

Philips
Components

PHILIPS

Television tuner for analog and digital cable applications

CD1536X

FEATURES

- UHF/VHF tuner for analog and digital cable applications
- Passive diplexer
- Systems RTMA M
- Digitally-controlled phase-locked loop (PLL) tuning programmed via I²C-bus
- Compact size, design incorporates a single-chip synthesizer mixer-oscillator IC
- Single 5 V power supply
- Complies with FCC, DOC Canada and CISPR13
- MCNS compliant
- Suitable for horizontal or vertical mounting.

DESCRIPTION

The CD1536X tuner combines a three-band tuner with a passive diplexer to accept RF and data inputs. It is specially designed to have the flat frequency response essential in digital cable applications and is also suited to standard analog applications.

CD1536X tuners are suitable for RTMA M systems.

Selectivity is provided by a tuned antenna circuit and a double-tuned bandpass filter separated by a MOSFET RF amplifier. IF amplification is provided by the mixer-oscillator IC.

The built-in PLL tuning system is digitally programmable via the I²C-bus. The system has multiple addressability and a minimum tuning step size of 62.5 kHz. The frequency range is continuously covered and is divided into three bands that include a tuning margin.

CHANNEL COVERAGE

BAND	FREQUENCY RANGE[1] (MHz)
Low band	57.0 to 159.0
Mid band	165.0 to 453.0
High band	459.0 to 863.0

Note

1. Frequency data refers to the IF centre frequency (43.75 MHz).

MARKING

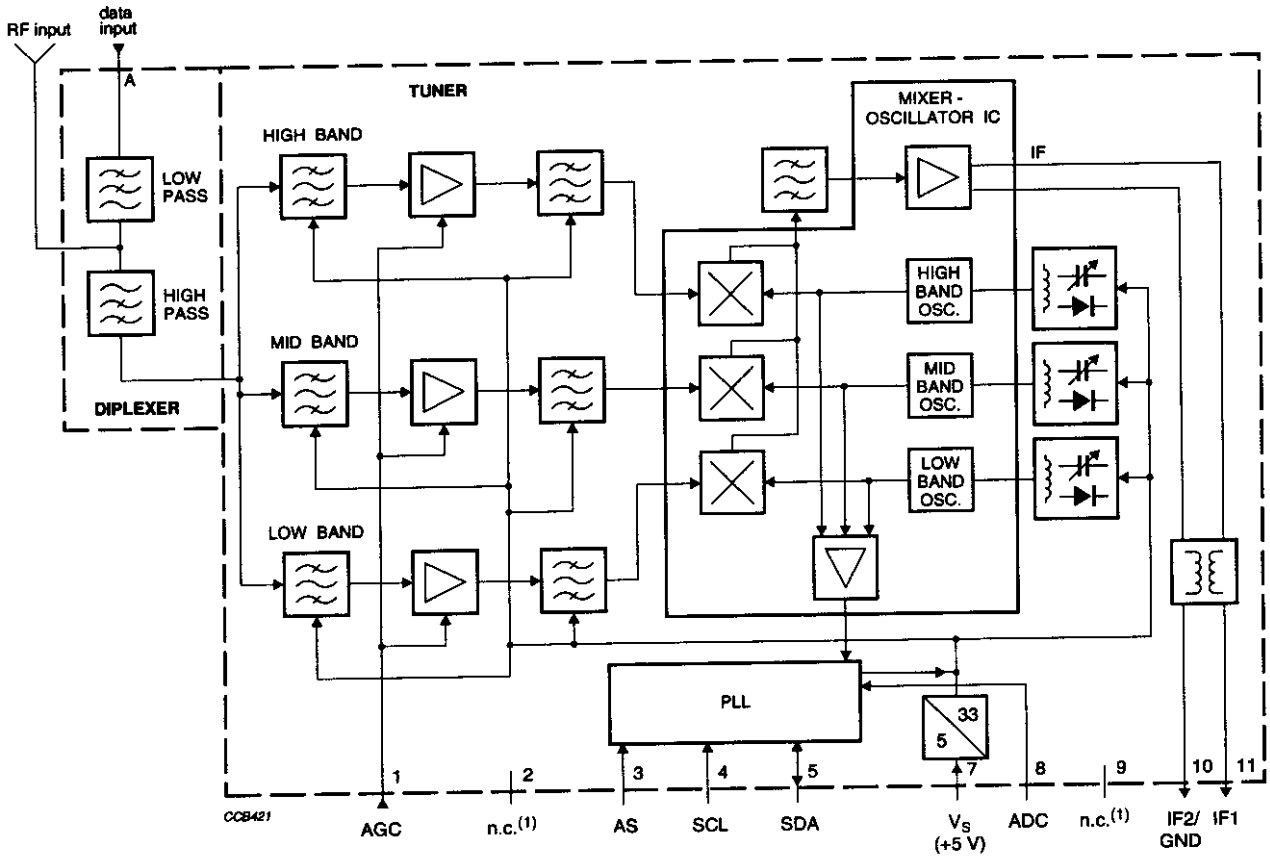
The following items of information are printed on a sticker that is on the top cover of the tuner:

- Type number
- Code number
- Origin letter of factory
- Change code
- Year and week code.

ORDERING INFORMATION

TYPE	CONNECTOR	DESCRIPTION	ORDER NUMBER
CD1536X/F H	F-type	horizontal version	3112 297 12241

BLOCK DIAGRAM



(1) For factory alignment and testing purposes only. Pin must be left open circuit in normal use.

Fig.1 Electrical block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
DATA	A	data input terminal
AGC	1	gain control voltage input
n.c.	2	do not connect; leave terminal open
AS	3	address selection input
SCL	4	I²C-bus clock input
SDA	5	I²C-bus data input/output
V_S	7	supply voltage (+5 V)
ADC	8	analog-to-digital converter input
n.c.	9	do not connect; leave terminal open
IF2/GND	10	IF output/ground
IF1	11	IF output
GND	TH1, TH2, TH3 and TH4	mounting tags (ground)

LIMITING VALUES

Limiting values under operational conditions

The tuner can be guaranteed to function properly under the following conditions.

SYMBOL	PARAMETER	PIN	MIN.	MAX.	UNIT
V_S	supply voltage	7	4.75	5.25	V
I_S	supply current		–	140	mA
V_{AGC}	AGC input voltage	1	–	5.0	V
ΔV_{AGC}	AGC input voltage range		0.6	4.75	V
I_{AGC}	AGC input current		–	16.0	µA
$Z_{S(AGC)}$	AGC source impedance		–	5.0	kΩ
V_{AS}	address select voltage	3	–	6.0	V
V_{SCL}	serial clock input voltage	4	–0.3	+5.5	V
V_{SDA}	serial data input voltage	5	–0.3	+5.5	V

Environmental conditions

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Non-operational conditions					
T_{amb}	ambient temperature		−25	+85	°C
RH	relative humidity		–	100	%
g_B	bump acceleration	25 g	–	245	m/s^2
g_S	shock acceleration	50 g	–	490	m/s^2
	vibration amplitude	10 to 55 Hz	–	0.35	mm
Operational conditions					
T_{amb}	ambient temperature		−10	+60	°C
RH	relative humidity		–	95	%

ELECTRICAL DATA

Conditional data

Unless otherwise specified, all electrical values apply at the following conditions. A proper function is guaranteed within the specified operational conditions but a certain deterioration of performance parameters may occur at the limits of the operational conditions.

SYMBOL	PARAMETER	VALUE	UNIT
T_{amb}	ambient temperature	25 ±2	°C
RH	relative humidity	60 ±10	%
V_S	supply voltage	5.0 ±0.1	V
V_{AGC}	AGC input voltage	5.0 ±0.1	V
f_{IF}	IF frequency	43.75	MHz

General characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_b	frequency range:					
	low band		57.0	–	159.0	MHz
	mid band		165.0	–	453.0	MHz
	high band		459.0	–	863.0	MHz
B_{-3dB}	–3 dB bandwidth:					
	low band		–	11	–	MHz
	mid band		–	16	–	MHz
	high band		–	18	–	MHz
G_V	voltage gain	Z_{IF} = 1.2 kΩ; 24 pF	37	42	47	dB
ΔG_V	AGC range:					
	low band		40	–	–	dB
	mid band		40	–	–	dB
	high band		30	–	–	dB
m_x	cross modulation	note 1	–	0.3	1	%
F	noise factor		–	9	11	dB
N_{osc}	oscillator phase noise:	frequency distance = 10 kHz				
	low band		–	–94	–88	dBc/Hz
	mid band		–	–84	–80	dBc/Hz
	high band		–	–85	–82	dBc/Hz
	oscillator phase noise:	frequency distance = 100 kHz				
	low band		–	–	–104	dBc/Hz
	mid band		–	–	–100	dBc/Hz
	high band		–	–	–102	dBc/Hz
α_i	image rejection:					
	low band		70	–	–	dB
	mid band		70	–	–	dB
	high band		60	–	–	dB
	return loss:					
	at centre frequency ±2.5 MHz		>10	–	–	dB
	out of channel		6	–	–	dB
$V_{I(max)}$	maximum voltage at aerial input		–	–	100	dBμV
$V_{I(osc)}$	oscillator voltage at aerial input	Z_I = 75 Ω; f ≤ 860 MHz	–	<22	–	dBμV
V_{ESD}	ESD protection; all pins	note 2	2	–	–	kV

Notes

1. Cross modulation: transfer of unwanted carrier modulation (f_{unw}) from an adjacent channel to the wanted carrier (f_w). Measurement conditions: $f_{unw} = f_w \pm 6$ MHz; level of all carriers = 70 dBμV; modulation = AM, 50%, 15 kHz; IF output load = 1.2 kΩ + 24 pF in parallel (tuned to f_{IF}); IF level limited to 106 dBμV (set by V_{AGC}).
2. All the pins of the tuner are protected against electrostatic discharge (ESD) up to 2 kV. The product is classified in category B *("MIL-STD-883C")*.

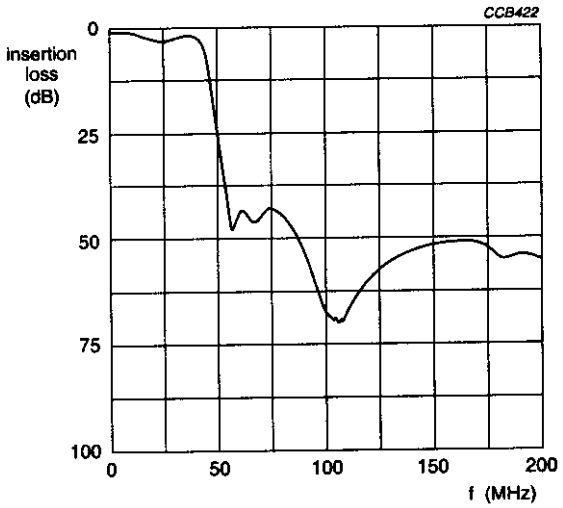
Diplexer input characteristics

RF input terminated in 75 Ω.

SYMBOL	PARAMETER	TYP.	UNIT
$f_{LPcutoff}$	low-pass filter cutoff frequency	43	MHz
$f_{HPcutoff}$	high-pass filter cutoff frequency	48	MHz
	return loss at data input terminal	>10	dB
	insertion loss from data input to RF input; see Fig.2	3	dB

Disturbance radiation and immunity

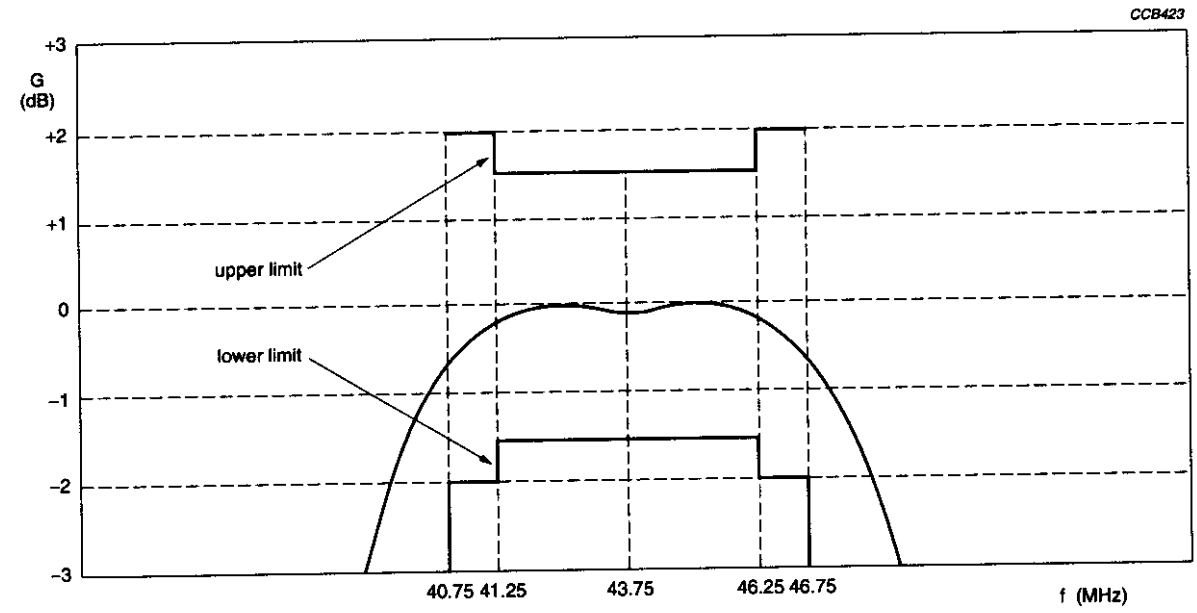
The tuners comply with part 15 of the FCC rules regarding oscillator radiation, signal handling and immunity from radiated fields.



RF input terminated with 75 Ω.

Fig.2 Typical data input frequency characteristic.

Amplitude response



The tilt of the overall response curve is defined as the absolute value between minimum and maximum levels within a bandwidth of 6 MHz.

Fig.3 Tilt of curve; typical values.

APPLICATION INFORMATION

A detailed description of the I²C-bus specification, with applications, is given in brochure *"The I²C-bus and how to use it."* This brochure may be ordered using the code number 9398 393 40011.

WRITE mode

BYTE	BITS								
	7 (MSB)	6	5	4	3	2	1	0 (LSB)	A[1]
Address byte (ADB)	1	1	0	0	0	CA1[2]	CA0[2]	R/W = 0[3]	A
Programmable divider byte 1 (DB1)	0	n14	n13	n12	n11	n10	n9	n8	A
Programmable divider byte 2 (DB2)	n7	n6	n5	n4	n3	n2	n1	n0	A
Control information byte (CB1)	1	CP[4]	0	0	1	1	1	0	A
Control information byte (CB2)	P7	P6	P5	P4	P3	P2	P1	P0	A

Notes

1. A = acknowledge.
2. CA = chip address select bits.
3. R/W = 0 for WRITE mode.
4. CP = charge pump setting bit.

CHIP ADDRESS

V_S = supply voltage at pin 7.

CA1	CA0	VOLTAGE AT PIN 3
0	0	0 to 0.1V_S
0	1	don't care (general address)
1	0	0.4 to 0.6V_S
1	1	0.9 to 1.1V_S

CHARGE PUMP SETTINGS

During search tuning, the charge pump high setting should be selected. After channel selection or during fine tuning, the low charge pump setting should be selected.

CP = 1 for charge pump high

CP = 0 for charge pump low.

PROGRAMMABLE DIVIDER SETTINGS (BYTES 1 AND 2)

Divider ratio:

$$N = \frac{f_{osc}}{8 \times f_{ref}}$$

f_{osc} = oscillator frequency

f_{ref} = reference frequency = 7.8125 kHz

$N = (2^{14} \times n14) + (2^{13} \times n13) + (2^{12} \times n12) + (2^{11} \times n11) + (2^{10} \times n10) + (2^9 \times n9) + (2^8 \times n8) + (2^7 \times n7) + (2^6 \times n6) + (2^5 \times n5) + (2^4 \times n4) + (2^3 \times n3) + (2^2 \times n2) + (2 \times n1) + n0$

Divider ratios below 256 are not allowed.

Minimum step size is 62.5 kHz.

BAND SWITCHING

BAND	BIT							
	P7 (MSB)	P6	P5	P4	P3	P2	P1	P0 (LSB)
Low	1	0	1	0	0	0	0	1
Mid	1	0	0	1	0	0	1	0
High	0	0	1	1	0	1	0	0

TELEGRAM EXAMPLES (WRITE MODE)

Start - ADB - Ack - DB1 - Ack - DB2 - Ack - CB1 - Ack - CB2 - Ack - Stop.

Start - ADB - Ack - CB1 - Ack - CB2 - Ack - DB1 - Ack - DB2 - Ack - Stop.

Start - ADB - Ack - DB1 - Ack - DB2 - Ack - CB1 - Ack - Stop.

Start - ADB - Ack - DB1 - Ack - DB2 - Ack - Stop.

Where:

Start = start condition

ADB = address byte

Ack = acknowledge

DB1 = divider byte 1

DB2 = divider byte 2

CB1 = control byte 1

CB2 = control byte 2

Stop = stop condition.

READ mode

The in-lock flag and the analog-to-digital converter value can be read out by setting the R/W bit to 1.

BYTE	BITS								
	7 (MSB)	6	5	4	3	2	1	0 (LSB)	A[1]
Address byte	1	1	0	0	0	CA1[2]	CA0[2]	R/W = 1[3]	A
Status byte	0	LB[4]	X[5]	X[5]	X[5]	AD2	AD1	AD0	–

Notes

1. A = acknowledge.
2. CA = chip address select bits (see "WRITE mode").
3. R/W bit = 1 for READ mode.
4. LB = 1 indicates loop is phase locked.
5. X = don't care.

ANALOG-TO-DIGITAL CONVERTER INFORMATION (AD BITS)

V_S = supply voltage at pin 7.

ADC INPUT VOLTAGE (PIN 8)	AD2	AD1	AD0
0.00 to 0.15V_S	0	0	0
0.15 to 0.30V_S	0	0	1
0.30 to 0.45V_S	0	1	0
0.45 to 0.60V_S	0	1	1
0.60 to 1.00V_S	1	0	0

IF output

IF OUTPUT LEVEL

To avoid driving the tuner into extreme signal handling conditions, adjust the RF gain control loop to obtain an IF output level of 105 dBμV ≤ V_{IF} ≤ 107 dBμV.

IF LOAD

The maximum permissible load at the IF output (pins 10 and 11): $Z_{IF(max)}$ = 1 kΩ (min.); 30 pF (max.).

Signal handling is optimized by tuning-out the reactive part of the IF load (C_{ext}) to the IF centre frequency using coil (L) connected in parallel to pins 10 and 11.

$$L = \frac{1}{(2\pi f_{IF})^2 \times (C_{ext} + C_{int})}$$

C_{int} = 4 pF

The IF amplifier output circuit is shown in Fig.4. This can be approximated to a floating source due to the coupling inductors and small capacitance to ground.

The tuner load can be symmetrical, or asymmetrical if the unused IF output pin is connected to ground.

Three load configurations are shown in Fig.5. Tracks on the main PCB to the tuner output pins should be as short as possible to prevent oscillator radiation and provide immunity from radiated fields.

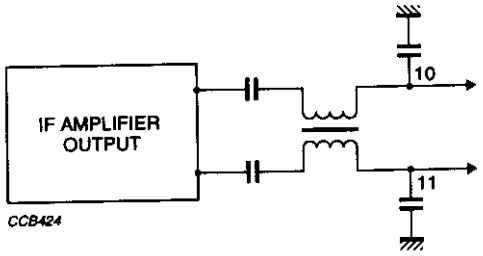
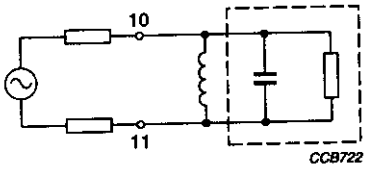
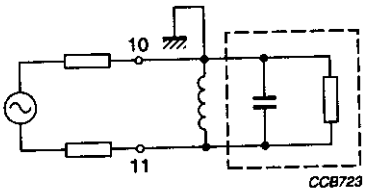


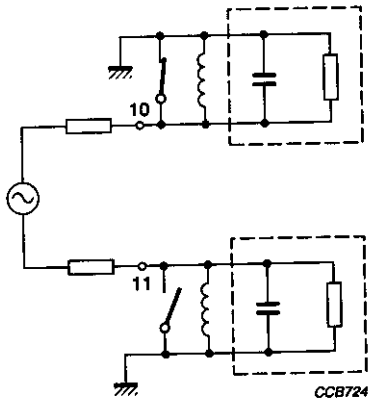
Fig.4 IF amplifier output circuit.



a. Symmetrical.



b. Asymmetrical.



c. Asymmetrical with switchable polarity.

Fig.5 IF loading using SAW filters.

TYPICAL AGC CURVES

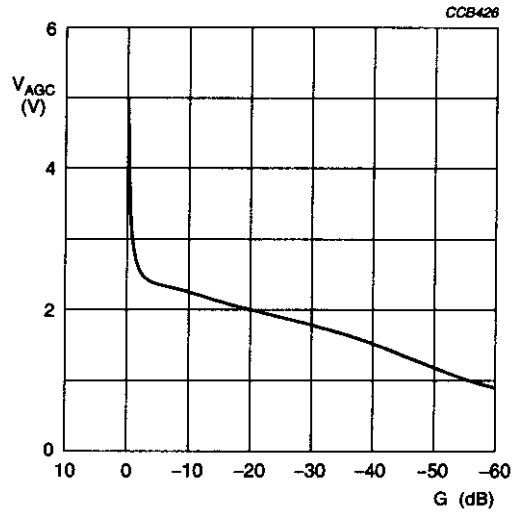


Fig.6 Low band AGC characteristic at 57 MHz.

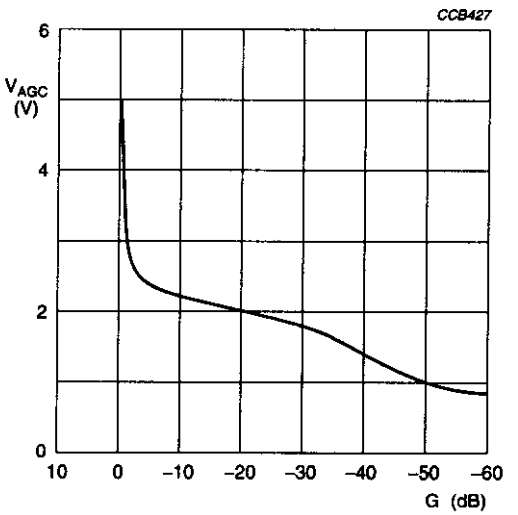


Fig.7 Low band AGC characteristic at 159 MHz.

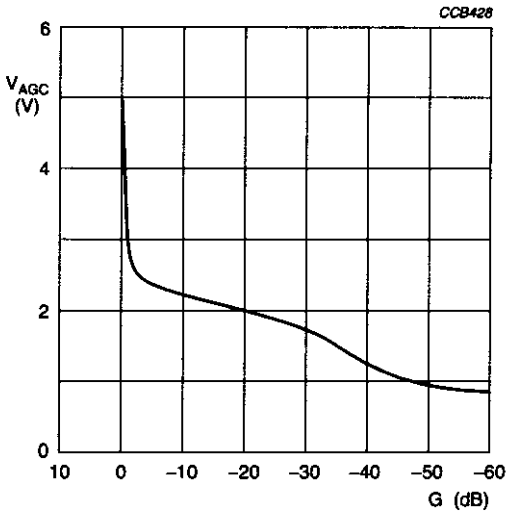


Fig.8 Mid band AGC characteristic at 165 MHz.

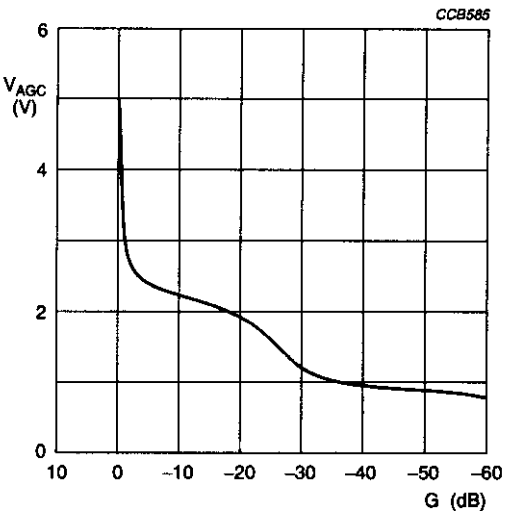


Fig.9 Mid band AGC characteristic at 453.5 MHz.

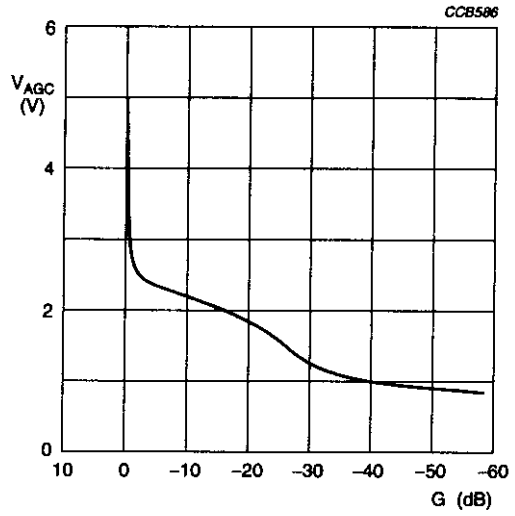


Fig.10 High band AGC characteristic at 459 MHz.

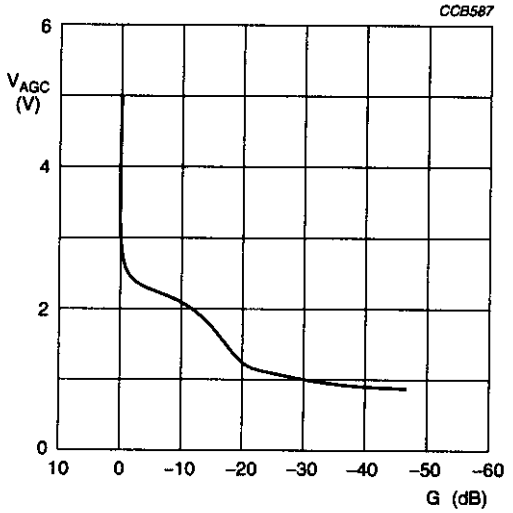
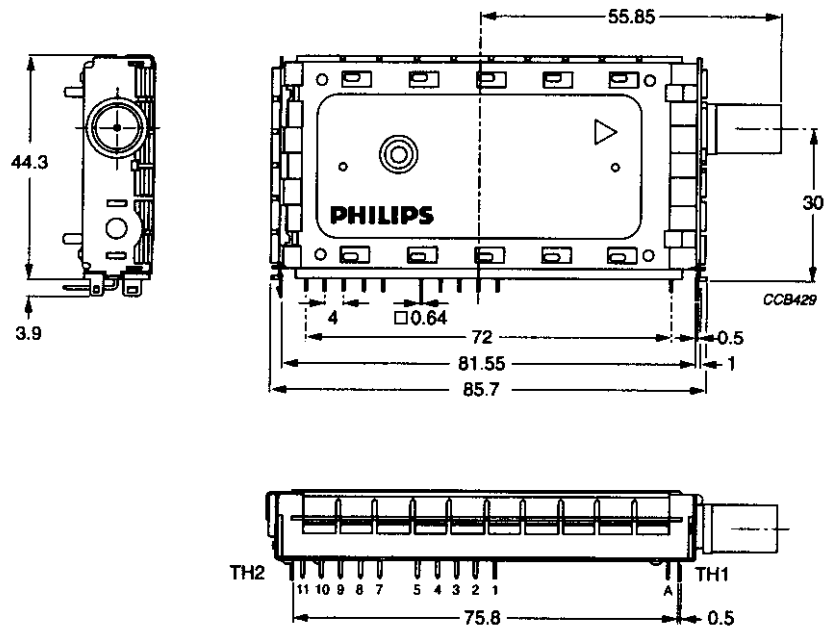


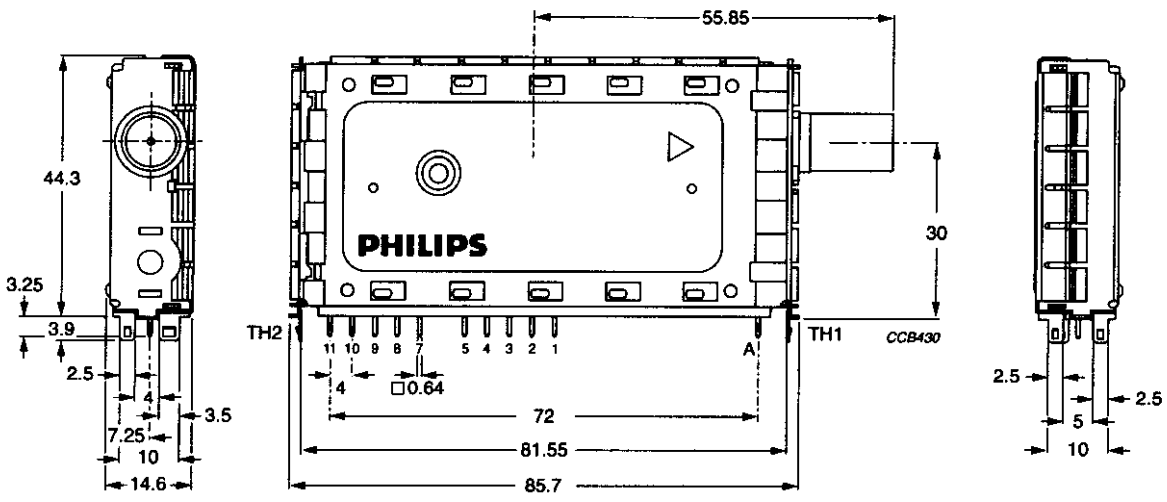
Fig.11 High band AGC characteristic at 863.5 MHz.

MECHANICAL DATA



Dimensions in mm.

Fig.12 Mechanical outline, horizontal version.



Dimensions in mm.

Fig.13 Mechanical outline, vertical version.

Aerial connection

Female F-type connector.

Solderability

The solderability of pins and mounting tags when tested initially and after 16 hours steam ageing in accordance with *"IEC 60068-2-20"*, test Ta, method 1 (solder bath 235 °C for 2 s), results in a wetted area of 95%. No de-wetting will occur when soldered at 260 °C for 5 s.

Resistance to soldering heat

The product will not be damaged when tested in accordance with *"IEC 60068-2-20"*, test Tb, method 1A (solder bath 260 °C for 10 ±1 s).

Mass

Approximately 57 g.

Robustness of pins

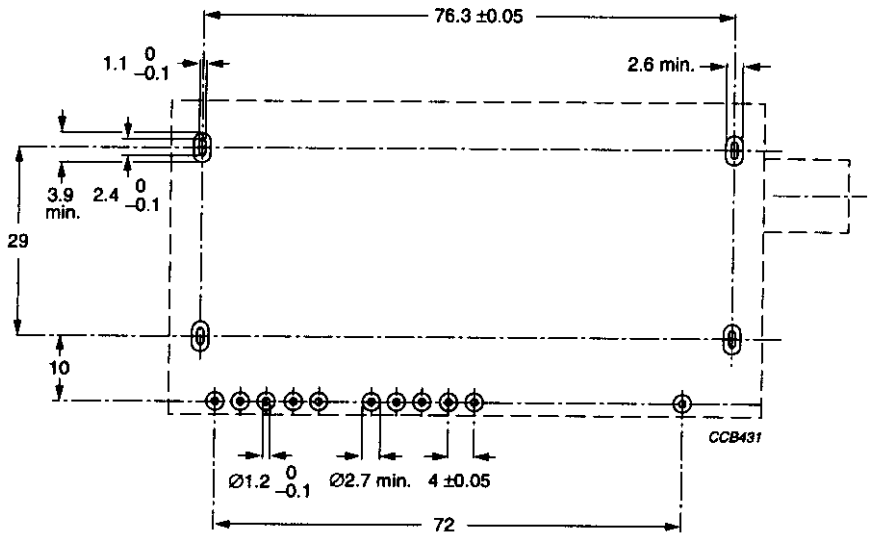
The pins will not be damaged when tested in accordance with *"IEC 60068-2-21"*:

- Test Ua1, tensile of 10 N in axial direction
- Test Ua2, thrust of 4 N in axial direction.

Punching pattern of chassis PCB

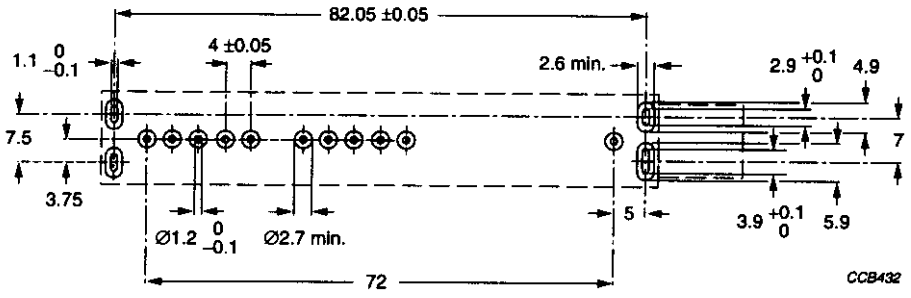
For mounting the tuner on a printed-circuit board (PCB), the recommended punching patterns are shown in Fig.14 for the horizontal version and Fig.15 for the vertical version.

The tuner must be mounted without clearance between the tuner supporting surface and the PCB. When mounted in this way, the tuner must be soldered to the PCB. This can be achieved by pressing the unit vertically on the PCB during soldering.



Dimensions in mm.

Fig.14 Punching pattern seen from solder side, horizontal version.



Dimensions in mm.

Fig.15 Punching pattern seen from solder side, vertical version.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

NOTES

NOTES

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