THEORY OF OPERATION FOR MODEL PDL4535

FCC ID: KEAPDL4535

1. GENERAL INFORMATION

The PDL4535 is a half duplex, UHF Radio Modem Transceiver with a built-in RF amplifier. It takes incoming serial data from a data terminal, modulates it with either 4-Level FSK or GMSK, and transmits it at RF power output levels of 2W or 35W. The carrier frequency is the UHF commercial band of 450MHz to 470MHz. Channel spacings at both 25 kHz and 12.5kHz are supported. The transceiver is also capable of receiving RF signals through a 50 Ohm impedance external antenna port. These signals are demodulated and passed out through the RS-232 port to the data terminal. The RF baud rate is selectable to be 4800, 9600 or 19,200 bits per second and is dependant on the selected modulation method. The modem requires a DC voltage power supply from +9V to +16V with a maximum current draw of 10 Amps. This product contains four printed circuit boards as described below.

2. I/O CIRCUIT BOARD

Incoming data is brought into two RS-232 interface chips (U5 and U6, ADM208EAR and ADM207EAR). The signals are received asynchronously and converted to CMOS levels. There are a total of 4 UART ports avaialable. Three of the ports are not currently used and the fourth is used to communicate with the microcontroller on the RFMOD. User accessible switches SW1 and SW2 provide on/off and channel control, respectively. A seven segment, LED, digital display is provided with DISP1. This display is driven by two serial to parallel data latches U3 and U4 (74HC164). These latches are connected in parallel and loaded with input from the 3 wire SPI interface from the controller on the RFMOD board. Additional status information is provided with discrete LED indicators D5, D6, D7 and D8. These provide indications for HI/LOW, TX, RX, and PWR activity.

Incoming voltage from an external supply is specified from 9V to 16V. This voltage enters voltage regulator U1 (LM2940T-8.0) and produces a regulated 8V supply which is used on the RFMOD board. This voltage is further regulated with U2 (MIC5200-5BM) which supplies the local 5V requirements for the I/O board. The external connections are ESD protected with Varistors RV1 through RV12.

3. VCO CIRCUIT BOARD

The VCO is a small daughter board that is soldered directly on the RFMOD circuit board. The VCO for the transceiver will vary in frequency from 450 MHz to 470 MHz for the transmitter and from 504.45 MHz to 524.45 MHz for the receiver. When the transceiver is in the transmitter state, the +5TX supply will provide power to the transmitter VCO circuitry. When the transceiver is in its receiver state, +5TX will turn off and +5RX will supply power to receiver VCO circuitry. The VCO tuning from the synthesizer IC on the RFMOD pcb steers varactor diodes D2 (SMV1104-36) for transmitting and D3 (SMV1104-36) for receiving. When transmitting, the MOD signal steers varactor diode D1 (MMBV3102L) to provide data modulation. The transmit oscillator is formed with Q1 (NE85633) and the receive oscillator uses Q2 (NE85633).

4. RFMOD CIRCUIT BOARD

4.1 Digital Section:

The microcontroller for this product is an 8 bit microprocessor (U1,MC68HC11FN). It is driven by Y1, a 9.8304 MHz crystal. The microprocessor stores its operating firmware in non-volatile memory using an 1M x 8 FLASH (U10, CAT28C64B-20J). RAM storage is provided by U5 (HY62256ALJ-120), a 32K x 8 SRAM. A Quad UART (U9, STC16C454IJ68) provides buffering for the three unused RS-232 interfaces on the I/O board in addition to providing many control

signals for the AMPLIER board. A local 5V supply for this section is provided by U4 (LP2951ACM) which runs from the 8V supply from the I/O board. This regulator also has a low voltage dectect which is used to reset the microcontroller.

4.2 Modem Section:

This product has two modulation methods, GMSK and 4-Level FSK. The user must select which form of modulation the modem will use. GMSK modulation and demodulation is provided by U3 (MX589DW). The timing reference for this device is a 2.4576 MHz clock which is produced from Y1 with an internal divide-by-4 circuit in the microcontroller. Output signals from the microprocessor determine whether the baud rate will be 4800 or 9600 baud. If 4-Level-FSK is selected then U27 (MX919) will provide the modulation and demodulation. Parallel commands sent from the microcontroller determine if the baud rate will be 19,200 or 9,600 bits per second.

4.3 Base Band Filtering Section:

The analog voltages which exit or enter the modem chips are DC coupled, nominally biased at 2.5 V, with peak to peak amplitudes of 1 Volt. Filtering of the analog signal to be transmitted is controlled by multiplexer U6 (74HC4052), which selects passive components to form the appropriate filtering as a function of the selected RF baud rate and modulation method. All received analog voltages pass through a two pole Sallen-Key low pass filter, which has a 3dB roll off at 12 kHz. Quad operational amplifier U7 (LMC658AI) provides the filtering and level adjustment . The bias voltage for the TX signal is firmware controlled by one half of a Dual 8 bit DAC U13 (MAX549AEUA). This DAC channel also provides final frequency adjustment to the radio as a function of sensed radio temperature from sensor U20 (LM50C). The amplitude of the TXA signal can be changed using variable resistor R34 to provide adjustment of frequency deviation to the radio. A two pole Sallen-Key low pass filter is incorporated at the next stage with poles at 32 kHz and 58 kHz.

4.4 Radio Section

4.4.1 Synthesizer:

A single PLL synthesizer (U17, LMX2315) is employed. Serial data from the microcontroller is sent over the SPI three wire interface to load new frequencies and effect synthesizer control. When the synthesizer phase lock loop is locked, the signal SYNLCK will transition high. The synthesizer reference crystal is X1 at 18 MHz. It is internally divided by 1,440 to provide a reference frequency of 12.5 kHz. Dual modulus prescalers of 64 and 65 are used for the N and A registers respectively. The N register is an 11 bit programmable counter and the A register is a 7 bit counter. The frequency of the VCO can be calculated with the following equation:

$$f(vco) = (((64 \times N) + A) \times 18\ MHz) / 1{,}440$$

The microcontroller has the values of N and A for sixteen preselected separate receive and transmit frequencies loaded into memory. The receive and transmit phase lock loops can be loaded independently at any time.

The crystal frequency varies with temperature according to a known curve. The temperature of the radio is measured with a temperature sensor (U20, LM50C), which sends its output voltage to the A/D on the microprocessor. As mentioned above, this data is used by the microprocessor to control a DAC channel that will change the bias voltage of the TX signal to keep the frequency of the transmitter within specification.

The +5VTX and +5VRX supplies are filtered by Q3 and Q4 (both 2N2222A), which act as capacitance multipliers on C33 and C34, respectively, to increase their value many times above their nominal value of 1µF. This makes a very low RF impedance and creates highly filtered supplies for the VCO.

The synthesizer loop filter is made up of C102, R78, C145 and C114. Additional RC filtering is performed by R108 and C185, which cuts down on the reference sidebands. Modulation of the VCO is accomplished with the voltage on TXA. Modulation balance between high frequency and low frequency components is set by adjusting R107.

4.4.2 Transmitter:

TX VCO amplification to the output RF level is performed by discrete transistor Q15 (NE85633), a MMIC IC U24 (UPC1678GV), and finally bipolar transistor Q10 (MRF8512). The RF output level of this signal is approximately 300mW. A coaxial cable connects to MCX connector J4 and directs this signal to the input of the AMPLIFIER board.

4.4.3 Receiver Front End Section:

The received signal from the antenna switch on the AMPLIFIER board enters through a coaxial cable into MCX connector J3. It then enters a helical bandpass filter (BPF2), which has 20 MHz bandwidth from 450 MHz to 470 MHz and 2 dB insertion loss. The signal then flows through a MMIC amplifier (U18, INA-51063), another helical band pass filter (BPF1), and is then passed to the mixer.

4.4.4 First Mixer and IF Filter:

Through the mixer (U3), high side injection is used to combine the signal from the receiver front end and the output of the RX VCO. This results in a first IF of 54.45 MHz. This signal enters a band pass filter formed by C94, R80, C95, L11, L10, R81, and C48, and a matching network formed by C163 and L16. The signal next enters a two section 54.45 MHz crystal filter formed by CF1 and CF2. These combine to provide a four pole filter that has a 3 dB pass band width of ±7.5 kHz and a 30 dB stop band width of ±25 kHz. The insertion loss is 4 dB.

4.4.5 IF Section:

The signal from the IF Filter passes through the IF Amp (Q7, NE85633 transistor) before entering the FM IF chip (U15, MC3371). A triple multiplier formed by Q8 and Q9 (both are MMBTH10LT1 transistors) acts on the 18 MHz signal from crystal X1 to form the second LO at a frequency of 54 MHz. This second LO mixes with the receiver signal to produce the 2nd IF at 450 kHz. Amplification and limiting of the 2nd IF is performed internal to U15. Filtering is accomplished by ceramic filters CF3 and CF4. Frequency discrimination of the signal is performed with quadrature detection. L6 adjusts the phase of the 90 degree shifted 450 kHz signal to center the mixed result.

U15 produces the RXA signal, which passes directly to the modem receiver filter circuitry. The RSSI signal generated at pin 13 of U15 is scaled by Op Amp U8 (LM658AI) and then enters an A/D channel on the microcontroller. This signal is an analog indication of received signal strength. A strong RF signal of -70 dBm will generate a voltage from 2.25 to 2.50 VDC. A weaker signal of -110 dBm will produce a voltage between 0.65 and 1.35 VDC. This voltage is used to provide a programmable carrier detect.

4.4.6 Amplifier Control:

The second channel of DAC U13 is used to provide a power output control for the AMPLIFIER board. The current draw of the final amplifier stage of the AMPLIFIER board is differentially sensed with Op Amp U11 (MAX4172). An analog control loop is formed with Op Amp U14 ((LM7131) comparing the sensed current to the commanded output level. The resulting signal forms PCNTL which drives the base of the transistor that supplies DC power to the first amplification stage on the AMPLIFIER board. This circuit provides the ability for RF output power regulation.

5. AMPLIFIER CIRCUIT BOARD

5.1 Relay Protection:

Externally supplied DC voltage must pass through mechanical relay K1 in order to provide DC power to the AMPLIFIER. This relay is controlled with the digital signal AMPWR from the micro-controller. This relay is activated only if the sensed input voltage level is acceptable.

5.2 First Amplifier (2 Watt) Stage:

The RF signal from the output of the RFMOD pcb is amplified by Q4 (MRF652S) on the AMPLIER board. The adjustable capacitor VC1 is used to optimally match the input signal. The RF output level of Q4 is programmable. It receives DC power from Q5 (MJF122) which is driven by the signal PCNTL. As described in the RFMOD section, the PCNTL signal is generated by a servo loop which compares the differentially detected current through power resistor R5 (0.01 Ohm) to a command voltage supplied by a DAC also on the RFMOD board.

5.3 HI/LOW Power Switch

An externally mounted switch accessible by the user controls whether the transciever will transmit at a nominal RF output level of 2W (low power setting) or 35W (high power setting). When the switch is in the low power setting, PIN diodes D5, D7 (both MMBV3401L) , D3, and D6 (both MA4P1250) will be forward biased. This will direct the RF energy from the output of the first stage amplifier Q4 to bypass the second and third amplification stages on the AMPLIFIER board and travel directly out to the harmonic filter and antenna port. This RF low power path is impedance matched with adjustable capacitor VC3. When the switch is in the high power position, the PIN diodes are reverse biased and the RF signal is directed to the second and third amplification stages on the AMPLIFIER board. The RF signal in this path is impedance matched by adjusting capacitor VC2.

5.4 Second and Third Amplifier (35W) Stages:

The second and third amplification stages are formed by Q1 (MRF641) and Q2 (MRF650). These common emitter transistors are used in a lumped element design. Q1 is the pre-driver and Q2 is the final driver. Q1 is class C biased through inductor L6 and Q2 is class C biased through inductor L4.

5.5 Low Pass Filter:

The harmonic filter is formed with L8, L9, L10, C32, C43, C44, C45, and C46. This filter is a seven element Chebyshev filter with a cut off frequency of approximately 500MHz. It provides over 50 dB of attenuation at the 2nd Harmonic for frequencies in the 450 to 470MHz range.

5.6 Antenna Switch:

The signal KEYAMP is provided by the microcontroller and determines if the AMPLIFIER is in receive or transmit mode. When KEYAMP is high, the AMPLIFIER board is in the transmit state. This will forward bias PIN diodes D4 and D8 (both MA4P1250). In this state the RF will be directed out the antenna port (J2) because inductor L19 will block the RF path to the radio receiver on the RFMOD board (J4). When KEYAMP is low, D4 and D8 are reverse biased and RF energy received on the antenna connector J2 will be directed through L19 and into the receiver on the RFMOD board through the connector J4.