PC3220 PC Card

Circuit Diagrams / Descriptions and Block Diagrams

Rev 0.1

Revision History

Version	Date	Owner	Notes
0.1	06/18/02	M. Wilson	Initial version.
0.2	06/19/02	M. Horie	Revised Block Diagram and Description.

Table of Contents

1 INTRODUCTION

1.1 Scope

This document is to provide circuit diagrams, and descriptions, including block diagrams, of the AirPrime PC3220 PC Card.

1.2 Not Used

1.3 References

[1] AirPrime Document, ‘PC Card System Architecture, Rev 0.2, dated 5/15/2002
[2] PCI Bus Power Management Interface Specification Revision 1.1

2 HARDWARE ARCHITECTURE

PC3220 Block Diagram

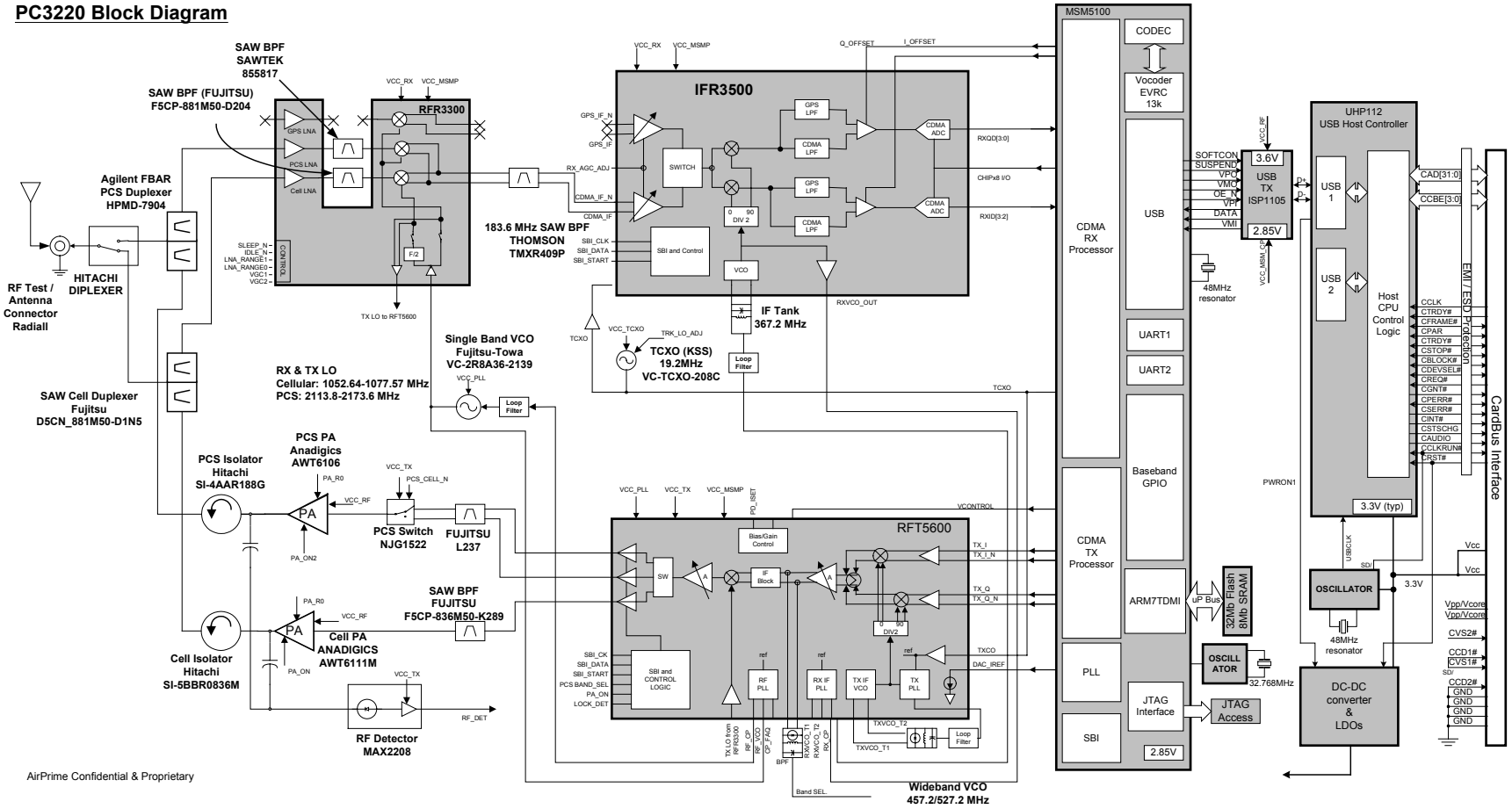

Figure 1: PC Card Hardware Block Diagram

Figure1 shows the hardware diagram of a PC Card supporting PCS band. The RF sections are shown on the left hand side of the block diagram, while the baseband sections are shown on the right hand side.

Component Name	Description
RF Receive Chain	
PCS RF SAW 855817 (SAWTEK) Cell RF SAW FAR-F5CP-881M50-D204 (Fujitsu)	RF SAW filter eliminates the images that would otherwise be mixed into the receiver IF band.
IF SAW TMXR409 (Thomson)	Selects the particular 1.23 MHz signal that is now centered at the IF band.
Dual Band Diplexer SLF-S080ML (Hitachi)	Separates signals in PCS and Cell bands
PCS Duplexer HPMD-7904 (Agilent) Cell Duplexer FAR-D5CN-881M50-D1N5 (Fujitsu)	The duplexers provide separation within each band between the RX and TX signals to allow full duplex operation (RX and TX operate simultaneously).
RFR3300 (Qualcomm)	RFR3300 includes LNA and mixer for GPS, PCS, and Cellular bands.
IFR3500 (Qualcomm)	The IFR3500 device provides key IF to digital baseband processing for subscriber unit receivers, including IF AGC amplification, quadrature downconversion to analog baseband, baseband filtering and amplification, and I and Q digitization
RF Transmit Chain	
RFT5600 (Qualcomm)	The RFT5600 IC provides transmitter signal path, from analog baseband to RF driver amplifiers, for multi-mode handsets. It contains the current reference for the transmit DACs, three PLL circuits, and Tx IF VCO circuit, buffer amplifiers for the RF_LO and TCXO signals, and various interface, control, and status circuits.
PCS TX RF SAW FAR-G6CN-1G8950-L237 (Fujitsu) Cell Tx RF SAW FAR-F5CE-836M50-K289 (Fujtisu)	Eliminates the images that would otherwise be mixed into the receiver IF band.
PCS PA AWT6106 (Anadigics) Cell PA AWT6111M5 (Anadigics)	Power Amplifier for the TX output power.

PCS Isolator SI-4AAR1880G01-T (Hitachi) Cell Isolator SI-5BBR0836M01-T (Hitachi)	This component provides a constant 50 ohm load to the PA even though the duplexer, diplexer and/or antenna impedance may change. Also, it keeps the RF detector from measuring any reflected power coming back from these components.
PLL Related	
Voltage Controlled Oscillator (VCO) VC-2R8A50-2139 (Fujtisu)	Generates the Main LO signal used by Rx and Tx chains
Voltage Controlled Temperature Compensated Crystal Oscillator (VCTCXO) VC-TCXO-208C (KSS)	Generates the 19.2 MHz reference signal used to phase lock the (3) PLLs.
Baseband	
MSM 5100 Baseband Processor (Qualcomm)	The MSM baseband processor integrates functions that support a CDMA subscriber unit. Subsystems within the MSM device include a CDMA processor, a Digital FM (DFM) processor (not used), a QUALCOMM-designed DSP for voice compression, an ARM7TDMI microprocessor. Also integrated in the MSM device are analog functions such as an audio voice codec, PLL, transmit DACs, ADCs, memories, a Universal Serial Bus (USB) device Controller (slave device), a R-UIM controller, peripheral interfaces, and an enhanced clock and power management architecture.
USB Transceiver (XCVR) ISP1105W (Philips)	The USB XCVR interfaces directly with the USB Controller of the MSM. It allows 3.3V programmable standard logic to interface with the physical layer of the Universal Serial Bus.
OpenHCI Controller UHP112 (TransDimension)	The USB OHCI chip conforms to the *(OpenHCI) Specification for the Universal Serial Bus* standard. It also acts as a USB to CardBus bridge. (HC) Hardware device which interfaces to the Host Controller Driver (HCD) and the Universal Serial Bus (USB). The interface to the HCD is defined by the OpenHCI Host Controller Interface. The Host Controller processes data lists constructed by the HCD for data transmission over the USB. The Host Controller contains the Root Hub as well.

2.1 RF

The dual band RF transceiver system of the PC3220 consists of three main subsystems: Receiver, Transmitter, and PLL. A general description of these RF subsystems is included in the following paragraphs.

2.1.1 Receiver section

The receiver section is comprised of a dual band, dual conversion superheterodyne receiver. The receiver is designed to process signals which are channelized by a combination of Frequency Division Multiple access (FDM) and Code Division Multiple Access. A brief overview of the signal flow and descriptions of each section is given.

2.1.1.1 Signal Flow

Received signals in the PCS Rx or Cell Rx bands are transferred from the dual band antenna to a frequency diplexer. The diplexer is a three port device (1 input, 2 output) that effectively separates the two bands by applying a low pass frequency response to the Cell Rx signals, and a high pass response to the signals at the PCS Rx band. Rx band signals at the outputs of the diplexer are applied to a frequency duplexer. In addition to providing the necessary isolation between Tx and Rx bands, the duplexer also applies a bandpass function from the duplexer's antenna to RX port. Received signals exiting the Rx port of the duplexer are applied to a Low Noise Amplifier (LNA). After amplification in the LNA, signals pass through an RF SAW bandpass filter, and are then downconverted in the mixer to an intermediate frequency (IF). Up to this point, the receiver has processed the entire Rx band. Once at the IF frequency, the signal passes through an IF bandpass filter which selects 1 CDMA frequency channel (1.25 MHz in width). The IF signal next passes through an IF AGC Amplifier where the gain is adjusted according to a control signal from the baseband processor. After proper level adjustment in the IF AGC Amplifier, the signal is applied to an I/Q downconverter where IF signals are downconverted to baseband I and Q components. The analog I and Q signals are filtered and then digitized by (2) 4-bit analog to digital converters. The resulting digital I and Q words are sent to the baseband processor for actual CDMA demodulation.

2.1.1.2 LNA/Downconverter

The LNA and downconvert mixer blocks are contained with the Qualcomm RFR3300 Integrated Circuit. A SAW filter is placed between the output of the LNA and the input to the Mixer. This filter rejects signals at the receive image frequency as well as protects the mixer from signals at the TX and other out of band frequencies. Filtered Rx signals are applied to the downconvert where they are mixed with main LO signal and translated to the 1st IF. The main LO signal generated by the PLL section in the RFT5600 provides the local oscillator used by the mixer. The frequency of the LO is selected to produce a 183.6 MHz IF signal. Signals at the output of the mixer are applied to an IF SAW filter. With a bandwidth of 1.25 MHz this filter selects IF signals centered at the LO-RF frequency of 183.6 MHz.

2.1.1.3 IF Section

IF signal conditioning, baseband conversion, and baseband digitization is performed in the Qualcomm IFR3500 IC. This IC contains an IF AGC amplifier, I/Q downconverter, A/D's, and an IF voltage controlled oscillator (VCO). Differential CDMA IF signals at the output of the IF SAW filter are applied to the IF AGC amplifier in the IFR3500. An analog voltage generated by the baseband processor adjusts the signal gain of the AGC amp to provide an optimum level into the A/D converters. This amplifier has a minimum of 85 dB dynamic range. CDMA IF signals at the output of the AGC amp are split into I and Q channels and simultaneously downconverted to baseband for analog to digital conversion. After digitization, the information is sent to the baseband processor for demodulation.

2.1.2 TX Section

The transmitter basically consists of a baseband to RF converter (the RFT5600), an RF SAW filter, SPDT switch, Power Amplifier, RF detector, and Isolator.

2.1.2.1 TX Signal Flow

A modulated analog baseband signal in the form of differential I and Q signals is provided to the RFT5600 IC from the baseband processor. Within the RFT5600 the CDMA baseband I and Q signals are mixed with the TX IF LO signal, and upconverted to the IF frequency. I and Q signals at IF are summed together, and applied to a differential AGC IF amplifier. An analog voltage generated by the baseband processor controls both TX IF and RF signal gain to achieve a minimum of 85 dB dynamic range. The output of the IF AGC amplifier is filtered with a simple L-C resonant tank. The primary function of this filter is to reduce spurious and noise at the receive band. After the IF filter, the CDMA signal is mixed with the main LO signal and upconverted to the RF transmit frequency. A single-sideband mixer is used to suppress the level of the undesired frequency product, thereby eliminating an image reject filter. After

upconversion, the PCS TX RF Band of 1850 to 1910 MHz is split into two 30 MHz bands. Transmit frequencies from 1850 to 1880 MHz are considered low band and frequencies from 1880 to 1910 MHz are considered high band. The signal flow for each band is similar, after upconversion the RF TX signal is amplified in a variable gain amplifier for RF AGC, and then applied to a final driver amplifier stage. Separate driver amplifiers are used for each band. Signals at the driver amp outputs of the RFT5600 are applied to a split band RF SAW filter. A split band SAW filter is simply 2 separate SAW filters, each covering 30 MHz of the TX Band. The narrow SAW filters achieve superior out of band rejection compared to a SAW filter covering the full TX band, especially over the RX frequency range of 1930 to 1990 MHz. A Single Pole Double Throw (SPDT) RF switch at the output of the split band SAW filter is used to select the TX CDMA signal band applied to the Power Amplifier (PA).

Operation of the transmitter in Cell CDMA mode is similar to PCS mode. Upconverted Cell TX signals within the RFT5600 are amplified in the RF AGC amp, and then applied to a single driver amplifier. The output of this driver amp is connected to an RF SAW filter covering the 25 MHz Cell Tx band. Filtered TX RF signals are then applied to the PA.

The TX signal level at the output of each PA is sampled with an RF detector circuit. Isolators positioned at the output of each PA provide the PA with a relatively constant load impedance under various antenna environments. With a constant load impedance, the gain of the PA is stabilized and PA generated spurious products are minimized. The transmit signal from each PA is sent to the antenna through the duplexer. The duplexer applies an asymmetrical bandpass transfer function to the TX band, providing over 50 dB of rejection of the TX signal to the RX port. This prevents the transmitter from interfering with the receiver.

2.1.2.2 Brief description of circuits for suppression of spurious radiation and brief description of circuit for limited modulation.

The RFT5600 receives baseband I and Q differential input signals, and produces a TX RF CDMA output signal. Steps are taken to ensure spurious, and harmonic signals generated in the upconversion process are adequately attenuated. First, in producing the 'TX IF Frequency, a synthesized TX IF LO is used. In PCS mode the TX IF LO is centered at 527.2 MHz, and in Cell mode an IF LO of 457.2 MHz is generated. The LO is divided by 2 within the RFT5600 to produce the required IF LO frequency. The 'TX baseband signal from the MSM is lowpass filtered in the MSM prior to the RFT5600. The output of the TX IF AGC amplifier section of the RFT5600 is bandpass filtered prior to the RF upconverter. Implemented as a simple LC resonator, this filter provides the necessary attenuation of Rx band noise.

Upconverted TX RF signals at the output of the RFT5600 driver amplifiers are passed through RF SAW filters to eliminate all but the desired frequency band. The filtered RF is input to the appropriate Power Amplifier (PA) which is capable of producing an output signal level compatible with industry standards. A diode detector samples each PA output signal. The detector output voltage, which is proportional to the RF signal level, is applied to an A/D integrated with the baseband processor. The processor maps the detector voltage to a Tx power level computed during the RF calibration process, and adjusts the TX signal level such that the output of the card does not exceed the maximum limit. Finally the TX RF signal at the PA output passes through the duplexer, which applies bandpass filtering to select only the TX RF frequency range. The output of the duplexer is connected to the dual band antenna.

The PCS TX RF output of the RFT5600 is filtered by a split-band RF SAW band pass filter. The nominal specification of the filter is as follows:

- Pass band (1850-1880 MHz): 1850-1880MHz
- Attenuation: DC ~ 1770 MHz: 25dB min.
  1930 MHz ~ 1960 MHz: 35dB min.
  1960 MHz ~ 3000 MHz: 25dB min.
- Pass band (1880 - 1910 MHz): 1880-1910MHz
- Attenuation: DC ~ 1800 MHz: 25dB min.

1960 MHz ~ 1990 MHz: 35dB min.
1990 MHz ~ 3000 MHz: 25dB min.

The Cell TX RF output of the RFT5600 is also filtered with an RF SAW filter. Specified performance of this filter includes:

- Pass band: 824-849 MHz
- Attenuation: DC ~ 800 MHz: 30dB min.
  869-894 MHz: 40dB min.
  894-1210MHz: 35dB min.
  1210-2000 MHz: 20 dB min.

Finally, spurious, harmonics, and noise generated by the PA and the RFT5600 are filtered by the duplexer. The nominal specification of the PCS duplexer is as follows:

- TX Passband: 1850 MHz ~ 1910 MHz
- Rx band attenuation: 1930 MHz ~ 1990 MHz: 40 dB min.

The Cell duplexer is specified to provide the following performance:

- TX Passband: 824 MHz ~ 849 MHz
- Rx band attenuation: 869 MHz:~ 894 MHz: 41 dB min.

2.1.2.3 TX Dynamic Range

The transmit signal level at the output of the transceiver is controlled over a dynamic range extending from –56dBm to +25.0. The baseband processor provides AGC by controlling the RF and IF signal gain within the RFT5600. An AGC range in excess of 86 dB complies with TX signal dynamic range requirements specified in IS-95.

2.1.3 PLL Section

The PLL subsystem within the RFT5600 synthesizes three LO signals; the Main LO applied to both the receiver, and transmitter, the RX IF LO centered at 367.2 MHz applied to the IFR3500, and the TX IF LO. The IF LO's are single fixed frequency LO's while the Main LO covers the frequency range of 2113.6 to 2173.6 MHz in PCS mode and 2105.2 to 2155.2 MHz in Cell CDMA mode. The low noise reference signal used by each PLL is provided by a 19.2 MHz Voltage Controlled Temperature Compensated Crystal Oscillator (VCTCXO).

2.1.3.1 Frequency Stabilization

All LO signals are phase locked to the 19.2 MHz VCTCXO reference signal, and therefore exhibit the low phase noise and excellent stability of this reference. An analog control voltage generated by the baseband processor adjusts the center frequency of the VCTCXO. This forms an Automatic Frequency Control (AFC) loop.

2.1.3.2 PLL Operation

A general description of the PLL operation is given using the PCS Main LO as an example.

The 19.2 MHz reference signal is applied to the reference divider in the main synthesizer of the RFT5600, which divides the 19.2 MHz by 384 to generate the internal comparison frequency of 50 KHz. This is one of the inputs to the phase detector. The other input to the phase detector is the Voltage Controlled oscillator (VCO) output signal divided by N. The divider ratio N is selected to be the ratio between the desired VCO output frequency and the reference frequency of 50 KHz. The phase-frequency detector

output is a current waveform, which has an average DC value that is proportional to the phase error between the comparison frequency and the VCO frequency divided by the N counter. The output of the phase-frequency detector is passed through the loop filter. The loop filter is a low pass filter functioning to remove all but the DC component of the phase detector output under steady state conditions. For the PC3220 a third order loop filter consisting of 2 resistors and 3 capacitors provides the necessary rejection of the reference frequency spurious. The phase detector average DC current value multiplied by the impedance of the loop filter generates the tune voltage applied to the VCO. This tuning voltage adjusts the output frequency of the VCO. A sample of the signal at the output of the VCO is sent back to the prescaler input of synthesizer where the VCO signal frequency is divided by 64 and then applied to the N divider. When there is a phase error, between reference and the output of the N divider, the PLL outputs a correction current. Since phase is the integral of frequency, phase adjustment means that VCO output frequency will also be adjusted to the desired frequency. The output of the main VCO is applied to the RFR3300 Rx IC. A buffer amplifier within the RFR3300 provides the main LO to the RFT5600. Programmable PLL parameters include; R counter, N counter, prescaler, phase detector, charge pump current,etc. All control words are transferred from the baseband processor to the RFT5600 via the Serial Bus Interface (SBI). The 19.2 MHz VCTCXO reference signal applied to the PPL has a specified frequency error of +-2PPM over the -30 °C ~ +80 °C temperature range. Within the AFC loop, the center frequency of the VCTCXO is adjusted by an analog voltage generated by the baseband processor.

2.1.3.3 Summary of Signals generated by the three PLLs.

2.1.3.3.1 Main LO Frequency Synthesizer: 2113.6 to 2173.6 MHz in PCS mode, 2105.2 to 2155.2 MHz in Cell CDMA mode

The main LO PLL loop consists of the synthesizer, loop filter, VCO, and VCTCXO. It generates the Main Local Oscillator for the TX RF and the RX RF.

Rx IF synthesizer: 367.2 MHz

Rx IF PLL loop consists of a synthesizer, VCO using active element internal to the IFR3500, loop filter and VCTCXO. This PLL generates the fixed frequency of 367.2, which is twice the RX IF of 183.6 MHz . A divide by 2 LO divider within the IFR3500 divides the 367.2 MHz LO by 2 to produce the 183.6 MHz signal required to translate the RX IF to baseband.

2.1.3.3.2 TX IF Synthesizer: 527.2 MHz in PCS mode, 457.2 MHz in Cell mode

The TX IF PLL loop is comprised of a synthesizer, VCO internal to the RFT5600, loop filter, and VCTCXO. In PCS mode, the oscillation frequency is programmed to 527.2 MHz, which is twice the TX IF of 263.6 MHz. Similar to the IFR3500 an internal divide by 2 is used within the RFT5600.

2.1.4 RF Section Interfaces

The external interfaces to the RF section in the PC3220 are the antenna and RF test connector. The interface between the baseband section and the RF section is internal to the PC3220.

2.2 BaseBand

2.2.1 DC Power Section

DC Power is supplied by PC, operating between 3.0V and 3.6V. All regulators operate in linear mode. There is one switching supply in the PC3200. The regulators and the switching supply used are listed below:

- VCC_3V3 : supplied by PC for Host Controller, USB Transceiver and each regulator except for TX regulator (3.0 – 3.6V)
- VCC_RF : switching supply for PA and TX regulator (3.6V DC)
- VCC_MSMCP: voltage regulator for MSM interfaces to RX and TX sections (2.85V DC)

- VCC_MSMA: voltage regulator for MSM Analog sections (2.60V DC)
- VC_TCXO: voltage regulator for VC-TCXO (2.85V DC)
- VCC_RX: voltage regulator for RF Rx part (2.85V DC)
- VCC_TX: voltage regulator for RF TX part (3.0V DC)

2.2.2 Digital Section

- MSM (Mobile Station Modem) ASIC is chip responsible for CDMA/FM mobile station's base-band digital signal processing. For this chip to function, and TCXO (19.2MHz) and SLEEP_XTAL_IN (32.768 kHz) are required as basic clocks.
- MSM consists of a PLL circuit that uses TCXO (19.2MHz) to generate the CPU clocks of 19.68 MHz or 26.24 MHz. CHIPx8 (9.8304 MHz) or CHIPx16 (19.6608 MHz) are also generated by the PLL. Intermediate frequencies within the PLL circuit are 1.92 MHz and 78.72 MHz.
- MSM consists of CDMA core and DFM core. CDMA core is a part for processing CDMA signal consisting of modulator/demodulator, interleaver/deinterleaver and encoder/decoder in the CDMA mode. The DFM core is not used by PC3200.

2.2.3 Memory Section

Memory section consists of Flash memory and SRAM.

- Flash memory: store to main program. 32Mbit
- SRAM: performs to read and write data. 8Mbit

The system uses CSP type memory, combination of Flash memory and SRAM.

2.2.4 Hardware Interface

The CardBus PC Card conforms to PC Card form-factor and 68-pin connector, and includes a high-speed signal interface based on the PCI bus. The Universal Serial Bus (USB) interface is used to provide an efficient interconnect between the PC3200 and a personal computer (via the USB-CardBus Bridge). Figure 2 shows the hardware interfaces for the PC Card and the laptop.

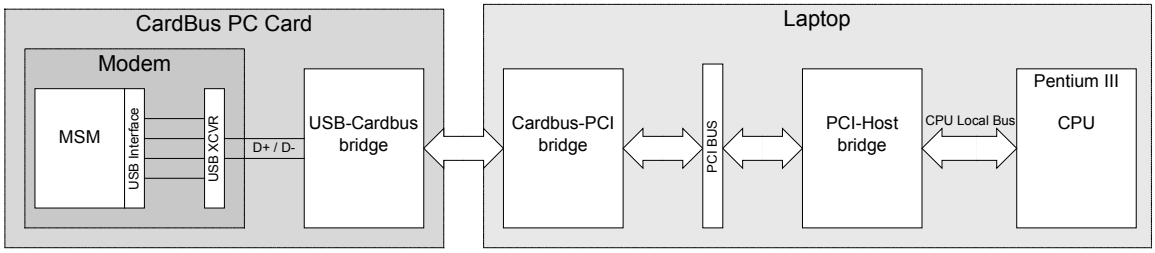

Figure 2: Hardware Interface System Diagram

- The **modem** is a USB device that includes both the MSM CDMA baseband processor and the USB Transceiver.
    - The MSM's USB controller interface supports full-speed (12 Mbps) data rates, and can be used to transfer general data, phone diagnostic data between the modem and a OpenHCI Host controller.
    - USB transceiver (XCVR) chip converts MSM's 2.85V GPIO signals to the 3.3V standard USB interface. It's capable of transmitting and receiving serial data at full speed data rates.
- The **USB-CardBus bridge (OpenHCI host controller)** interfaces the modem to the laptop via the CardBus interface to transfer user data and control signals. The Host Controller Driver and

Host Controller work in tandem to transfer data between client software and a USB device. Data is translated from shared-memory data structures at the PC client software end to USB signal protocols at the USB device end, and vice-versa. The TransDimension chip is used for the OpenHCI Host Controller.

- A **CardBus-PCI bridge** detects when a PC Card is installed in a socket, configures the interface to provide enhanced capabilities available to 32-bit PCI devices (including bus mastering), and provides the connection between PC Card socket and the PCI Bus.

- The **PCI-Host bridge** provides the interface between the PCI Bus and the CPU.

2.2.4.1 Modem

The modem is a USB device (to the PC) supporting the full speed data rate (12 Mbps) only. It supports the following endpoints.

Table 1: Endpoints Supported

Direction of the endpoints:
IN – From Module to Host
OUT – From Host to Module

Note: The shaded rows are descriptions for end points not currently supported by the PC Card.

Endpoint #	Type	Packet Size (bytes)	FIFO Size (bytes)	Endpoint Description
0	Control IN	16	16	The control endpoints are used to configure a device at attach time and can be used for other device-specific purposes, including control of other pipes on the device. Data transferred on control endpoints follow a predefined message structure.
0	Control OUT	16	16	See Control IN
1	Interrupt IN	16	16	The interrupt endpoint is used to convey status information for the serial lines USB emulates: RI, DSR, CD, etc.
2	Bulk Data IN	64	256	The bulk data endpoints are used for lower speed data transfers with smaller FIFO. This is currently not used.
3	Bulk Diagnostic IN	64	128	The bulk diagnostic endpoints are used for lower speed data transfers with smaller FIFO. This is currently not used.

4	Isochronous IN (Not currently supported)	16	32	The isochronous endpoints are currently **NOT** supported by the AirPrime CDMA modules. Isochronous transfers occupy a pre-negotiated amount of USB bandwidth with pre-negotiated delivery latency. (Also called streaming real time transfers)
5	Bulk Data OUT	64	256	See Bulk Data IN
6	Bulk Diagnostic OUT	64	128	See Bulk Diagnostic IN
7	Isochronous OUT	16	32	See Isochronous IN
10	Bulk Burst IN	64	4096	The bulk burst endpoints are used for high-speed data transfers. However, only one set of endpoints (bulk data or bulk burst) is used based on a compilation flag in the DMSS software. Currently, bulk burst is used for data transfer
11	Bulk Burst OUT	64	1024	See Bulk Burst IN

Simultaneous Endpoints
The software driver and modem firmware are modified to support simultaneous endpoints: Bulk Diagnostic IN/OUT, and Bulk Burst IN/OUT.

Sleep Requirement
If USB not suspended, modem can't sleep due to TCXO still being active. See [2] for more detail on PC card power management.

2.2.4.2 OpenHCI Host Controller

The Host Controller in the PC Card is the TransDimension UHP112, a two-port PCI to USB OpenHCI Host Controller. It supports
- A 32-bit 33MHz PCI interface compliant with PCI Local Bus Specification Revision 2.1s.
- Two downstream USB ports
- Full compliance with USB Specification Revision 1.1
- OpenHCI Open Host Controller Interface Specification for USB Release 1.0a compatible
- Provides advanced power management capabilities compliant with PCI Bus Power Management Interface Specification Revision 1.1 (See [2] for detail)
- Fully compatible with Windows OpenHCD drivers