SIERRA WIRELESS

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# 1XRTT AC555 Detailed Circuit Description

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| **Document #:** | **2110622** |
| **Revision:** | **C** |

## Table of Contents

# 1 General

## *1.1 Purpose*

This document details the logic circuitry of the AC555 modems.

## *1.2 Scope*

This document covers only the logic portion of the product.

## *1.3 Glossary of terms*

1XRTT – Qualcomm's CDMA2000 Standard.
ASIC – Application-Specific Integrated Circuit
FPGA – Field Programmable Gate Array
PCMCIA – Personal Computer Memory Card International Association
PWM – Pulse Width Modulated
TCXO – Temperature Controlled Oscillator
USB – Universal Serial Bus

## *1.4 References*

| Ref. # | Doc. # | Document title |
|---|---|---|
| R-1 | | MSM5105 Device Specification |
| R-2 | | RFT3100 Device Specification |
| R-3 | | IFR3000 Device Specification |

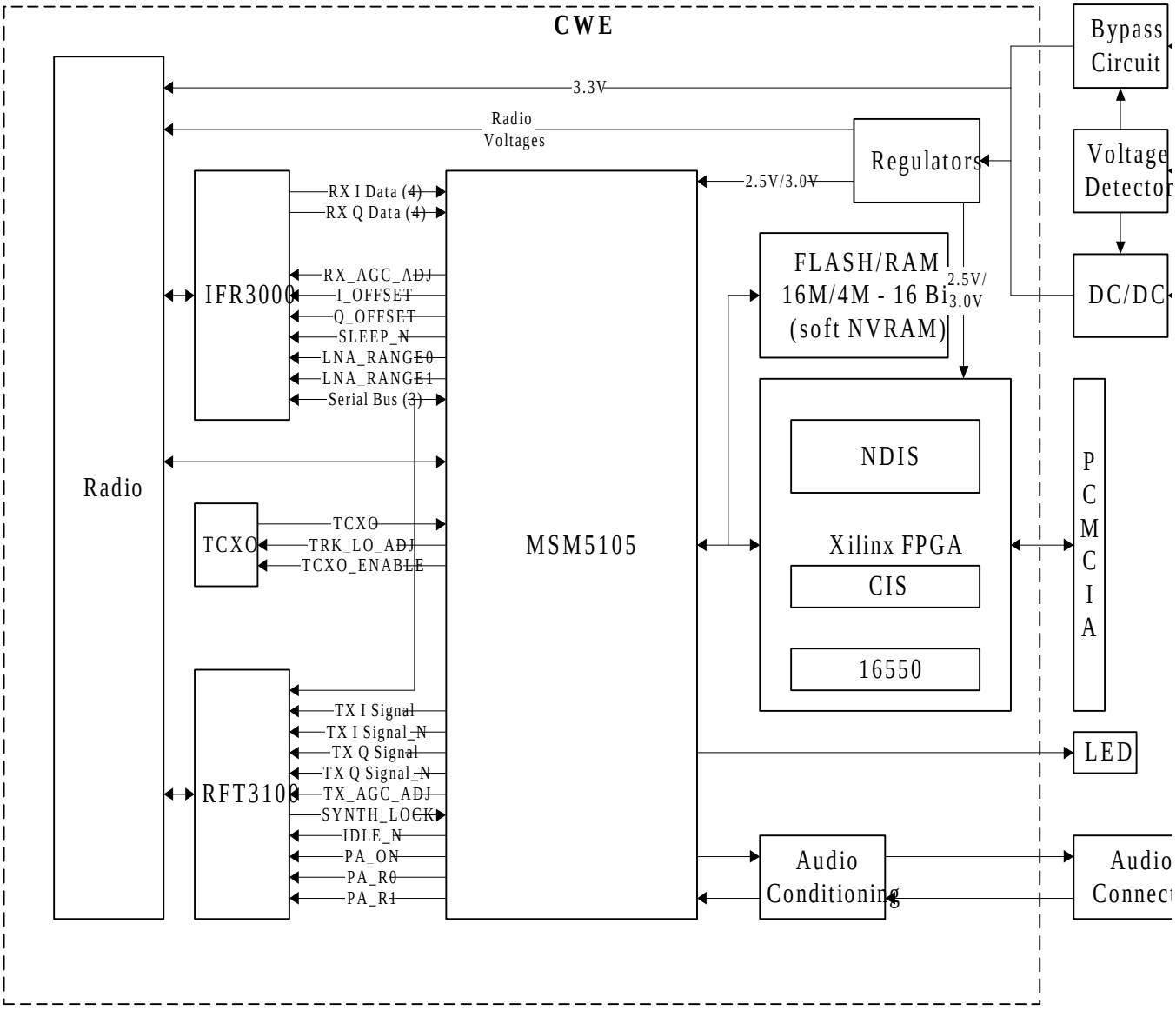
## *1.5 Revision history*

| Revision | Date | Author | Summary of changes | ECO # |
|---|---|---|---|---|
| A | Nov 24, 2000 | Phillips | Original | |
| B | Dec 7, 2000 | Phillips | Modified document based on feedback. | |
| C | Aug 2, 2001 | D. Kwong<br>T. McKeen | Added RF section | |

# 2 Circuit Description

## *2.1 LOGIC*

### 2.1.1 Block Diagram




### 2.1.2 MSM5105

The MSM5105 is a Qualcomm's ASIC. It's the lower cost version of the MSM5100. Both chips are the 1XRTT version of the MSM3100. The MSM3100 is not compatible with the MSM3000, which we used on the AirCard510. The MSM5105 contains an ARM7 micro controller, a DSP, an 8 channel A/D converter, voice codec, 1 USB port, 2 UART ports, and some other glue logic.

The MSM5105 uses the FLASH to store its firmware and the RAM to store variables. The FLASH and RAM are combined in one stacked chip part. This type of part was chosen to save space on the PCB. The FLASH supports "read while write" operation, which allows the data that used to be stored in the external EEPROM to move into the FLASH. The FLASH ROM has 16 Megabits of storage arranged in 2M by 16bit words. The FLASH is sectorized so that it can be reprogrammed in blocks. The RAM is a 4 Megabit part arranged in 256k by 816 bit words. One quarter of the FLASH is reserved to replace the function of the EEPROM. The special bank can also store data such as the CIS and FPGA programming information that is not used when the CDMA engine is running.

The MSM5105 runs off the radio's 19.68MHz TCXO clock. It has a secondary 32.768kHz clock, which it uses when in sleep mode to wake up the TCXO clock.

The MSM3000 has two interfaces to other parts of the circuit. The first is the interface to the FPGA/ASIC. The FPGA/ASIC is attached to the MSM5105 through its memory bus. This allows the FPGA/ASIC to be part of the MSM5105's memory map. The second interface is to the radio. The transmit and receive signals are sent from the MSM5105's DSP to the radio as I and Q data. The receive data is digital but the transmit data is analog. This is different from the AirCard510, which was entirely digital. The other control signals are on/off signals such as the PA_ON and PWM signals such as TX_AGC_ADJ. PWM signals once properly filter can server as D/A outputs.

### 2.1.3 FPGA/ASIC

The logic interface chip is an FPGA during development and ASIC during production. It serves the purpose of PCMCIA interface. The PCMCIA allows the modem to be plugged into and powered on in any PCMCIA socket. The FPGA/ASIC provides the CIS information the PCMCIA host needs. This information is programmed into the ASIC by the MSM5105 upon boot up. The FPGA/ASIC also contains a 16550 serial port emulator and an NDIS interface with dual 256 by 16bit synchronous FIFOs. The 16550 port is for FAX and circuit switched connections. The NDIS is for packet connections and status information.

### 2.1.4 DC to DC Converter

The modem has one DC-to-DC converter, which is uses to convert 5.0V down to 3.3V. This allows the modem to work in both 5.0V and 3.3V PCMCIA sockets. It is capable of delivering 1Amp of continuous current at an efficiency of over 90%. There is a voltage detector, which senses if the input voltage is 3.3V. If it is, then the DC/DC converter is switched off and the bypass FET is switched on.

### 2.1.5 Voltage Regulators

The modem has multiple low-dropout regulators. One is used to power the MSM5105 and the Xilinx FPGA. The others are there to provide various voltages to the radio. The regulators also have the addition functions of providing isolation and volt-dip protection.

### 2.1.6 Audio Circuitry

The AirCard555 is capable of doing voice calls. For this reason connections are made to the MSM5105's built-in codec to provide microphone input and speaker output on the audio connector.

# 3 Aircard 555 Radio

## *3.1 RF Circuit, Cellular and PCS Transceiver*

The transceiver is a spread spectrum O-QPSK full duplex modem capable of operating in the AMPS (824 – 894 MHz) and PCS (1850 – 1990 MHz) bands. Max output power is +23.0 dBm as outlined in the IS2000 and IS-98D CDMA standard with a max current draw of 800 mA while transmitting at this level. Channel spacing for the above bands is 30 KHz for AMPS and 50 KHz for PCS.

## *3.2 Specifications*

Aircard 555 will comply with the requirements of IS-2000 and IS-98-D.

**General**

**Table 1: Power Supply**

| | |
|---|---|
| DC Power Supply | 3.3V +/- 5% in series with a source impedance of 0.5 ohms (minimum of 3.0V under load) |
| | |

**Table 2: Transceiver Specifications**

| | | |
|---|---|---|
| | AMPS | PCS |
| Transmit Frequency | 824 to 848 MHz | 1850 to 1910 MHz |
| Receive Frequency | 869 to 893 MHz | 1930 to 1990 MHz |
| Channel Spacing | 30 KHz | 50 KHz |
| Modes | Receive, Full Duplex Transmit | |
| Modulation | O-QPSK, BW = 1.25MHz | |
| Performance Bandwidth | 25 MHz | 60 MHz |
| Frequency Stability | +/- 2.5 ppm over all environmental conditions | |
| **Transmitter** | | |
| Transmit Output Power (conducted) | 200 mW (23 dBm), adjustable to .010 uW (-50 dBm) @ +3.3Vdc | |
| Transmitter Spurious Outputs | Per FCC Part 22, 24 | |
| | | |

| **Receiver** | |
|---|---|
| Sensitivity (conducted) | -104 dBm for 1% FER (AMPS)<br>-104 dBm for 1% FER (PCS) |
| ACPR<br>PCS<br>AMPS | <br>-42 dBc @ 1.25MHz<br>-42 dBc @ 885KHz |
| Spurious Emissions | Per FCC 15 |

**Table 4: Environmental Specifications**

The product must, as a minimum, meet all PCMCIA specifications (release 2.01, section 3.6) except for operating temperatures as shown below:

| | |
|---|---|
| Operation Temperature | -30 to +65 deg. C |
| Humidity | 95% non-condensing |
| Vibration | Per PCMCIA spec<br>15G peak, 10-2000 Hz (non-operating) |
| ESD | Per PCMCIA spec |
| Shock | Per PCMCIA spec |
| Drop | 30 in. onto non-cushioning vinyl covered concrete |
| | |

**Physical Specifications**

Aircard 555 will be a type II PCMCIA card with minimal (<15mm) or no extension other than the antenna.

**Antenna Specifications**

The antenna is a removable hinged flip-up antenna that is capable of withstanding a drop onto vinyl from 30 inches (per PCMCIA spec) while in any extended position without damage (while out of slot). The antenna, when not in use, will fold down or rotate. The RF output of the Aircard 555 will have a 50 ohm coaxial connection to support remotely mounted antennas and test connections.

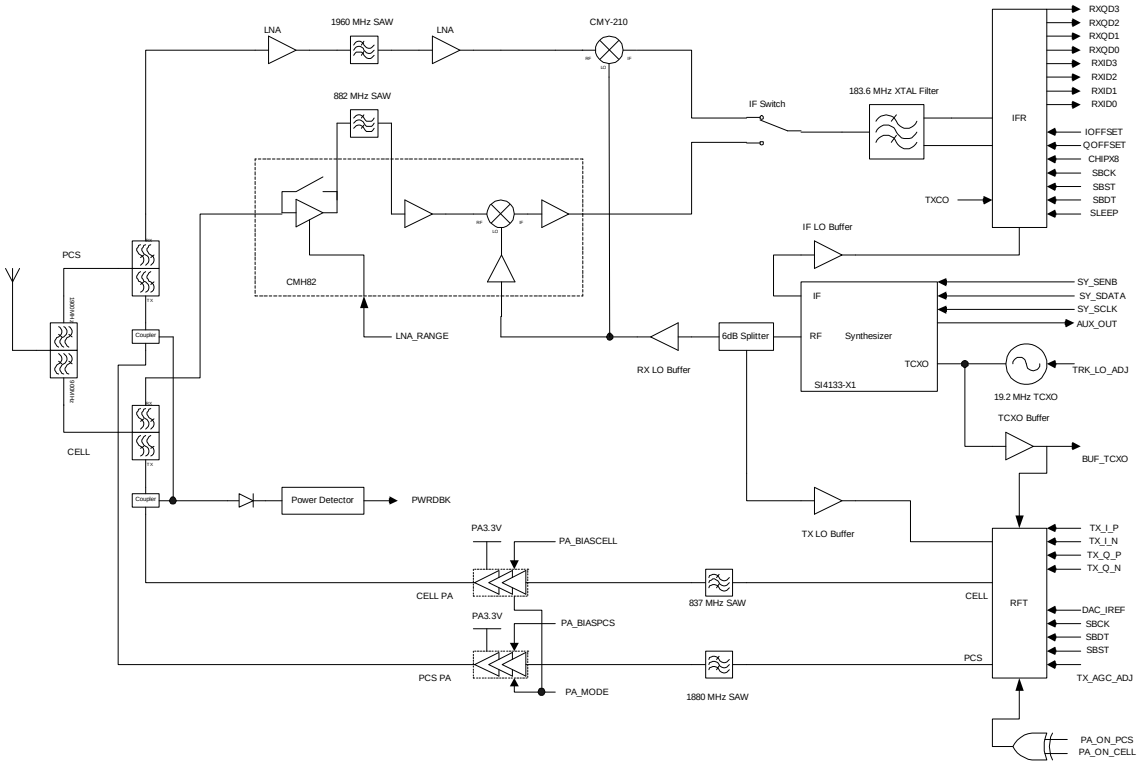
The gain of the antenna will be in the range of 0 to –1.0 dBi.

### *3.3 Architecture*

A block diagram of the radio section is given below in Figure 2. The Aircard 555 wireless modem consists of two main sections, i.e. the Control Logic Circuits and the Radio Transceiver Circuits. Qualcomm's MSM5105 in the logic section controls all functions in the transceiver. It is responsible for programming the synthesizer, RF power selection, enabling and disabling the transmitter and receiver sections, and performing electronically tuned adjustment.

The transceiver uses a single synthesizer for both the transmitter and receiver. The operation of the synthesizer is described in section 2.4, Frequency Generation Unit. The synthesizer uses high-side injection for both the AMPS and PCS bands. The synthesizer produces a frequency that is 183.6 MHz above our desired RX frequency (RX first LO) and 263.6 MHz above our desired TX frequency for PCS (228.6 MHz for AMPS). The transmitter and receiver are described in more detail in the appropriate sections.

Figure 2. Radio Block Diagram



### *3.4 Frequency Generation Unit*

The frequency generation unit (FGU) generates the local oscillator signals for the receiver and the transmitter. It consists of a 3 phased locked loops that produces a synthesized signal in the range of 1052.61 to 1077.61 MHz for AMPS, 2113.6 to 2173.6 MHz for PCS, and a dedicated IF LO of 367.2 MHz (2xIF) all contained within Silicon Lab's Si4133-X1 synthesizer. The desired frequency is programmed by the MSM via the synthesizer control lines (SY_SENDB, SY_SDATA, SY_SCLK).

This LO signal is routed to the transmitter where it is downconverted by mixing with a AMPS or PCS TX IF (283.6 and 228.6 MHz respectively) modulated signal to produce our transmit carrier frequency. It is also routed to the receiver mixer where it downconverts receive signals into the first IF of 183.6 MHz. The FGU also supplies an IF frequency of 367.2 MHz to the IFR3000 subsystem where it is frequency divided by two providing our second LO.

#### 3.4.1 19.2 MHz Reference Oscillator

The Reference Oscillator produces a 19.2 MHz output sine wave signal. It has digital temperature compensation that provides frequency stability of +/- 2.5 ppm over the temperature range of -30 deg. C. to +80 deg. C. Total frequency stability over temperature, voltage and load variation is +/ 0.3 ppm. The reference oscillator feeds the SI4133-X1 synthesizer chip, MSM5105, RFT3100 and IFR3000.

#### 3.4.2 LO Buffer Amplifiers

The output of the synthesizer (RF section) is split via a 6dB resistive splitter and fed into two LO buffers (RX and TX). These signals are amplified by the buffers to increase its output level providing enough LO drive to the cellular and PCS mixers. The IF LO buffer's output is fed to the IFR3000.

### *3.5 Transmitter*

The transmitter produces an output frequency in the range of 824 to 849 MHz AMPS and 1850 to 1910 MHz PCS, with channel assignments as per the AMPS and PCS frequency allocation specifications. The transmit chain consists of the RFT3100, cellular and PCS saw filters, power amplifiers, power detectors, duplexers and a diplex filter. The majority of the transmit duties are performed by Qualcomm's RFT3100 O-QPSK IQ modulator and PA driver chip. This chip consists of 2 differential IQ modulators, onboard IF synthesizer, an upconverter, cellular and PCS PA drivers, and integrated automatic level control circuit. The output of the FGU is mixed with the output of the modulator to produce our desired transmit carrier in the desired band of operation. It is further

processed by filtering and amplification before being applied to the duplexer, diplexer and antenna.

### 3.5.1 Power Amplifier

The PA amplifies the transmit signal to produce 200mW of RF power before being applied to the duplexer. The PA's gain can be switched from low power mode to high power mode by utilizing the PA_MODE switch, large signal gain is increased by 6 dB.

### 3.5.2 Automatic level control

A high Z resistive power coupler is used to tap the output of the PA which is then fed Schottky diode for power detection. The result is fed to one of the MSM's ADC in which the MSM uses accordingly to maintain our desired output.

### 3.5.3 Duplexer and Diplexer

The RF output of the PA is fed to the duplexer, which combines the transmitter and receiver sections to use one antenna port. The duplexer also provides additional bandpass filtering for the transmitter and receiver. To separate the AMPS and PCS bands a diplexer is used before the antenna.

## *3.6 Receiver*

The receiver is a single conversion super heterodyne type, with an IF of 183.6 MHz. Receive signals coupled into the antenna passes through the diplexer and fed to the desired bands duplexer before being fed to their respective RX front ends. For PCS the output of the duplexer is fed to the first LNA it is then filtered by SAW bandpass filter and then fed to the second LNA. From this point the output of the second LNA is fed to a downconverter. The receive signal is downconverted to an IF of 183.6 MHz before going the IF switch. For AMPS, the receive chain is very similar to that of the PCS chain, the LNA stages and mixer stage are handled by a single chip (CMH82) rather than discretely.

The local oscillator for this both mixers are provided by the FGU. The downconverted signal is fed to a IF switch. This is where the AMPS and PCS receive chains common point in the circuit. The switched signal is then bandpass filtered by a 183.6 MHz SAW filter and then fed into the IFR3000. This IC first mixes our 183.6 MHz IF signal with a IF LO of 183.6 MHz (generated by dividing 367.2 MHz FGU IF signal) giving us

baseband data. This signal further undergoes a series of amplifiers, limiters and serial to parallel shift registers before being applied to MSM5105.

### *3.7 Baseband Audio Processing – Transmitter and Receiver*

Baseband data signals to the radio are buffered, amplified and level shifted before being applied to the transmit modulator.
Transversely, a demodulated receive signal is fed to the MSM5105 processor for decoding.

### *3.8 Tuning Functions*

All tuning functions in the transceiver are performed electronically. The tuning voltages are controlled by the MSM5105 with its onboard digital-to-analog converters. The radio's tuning functions are described below.

#### 3.8.1 TRK_LO_ADJ

Centering of the synthesizer reference oscillator is achieved by adjusting its DC bias (via the TRK_LO_ADJ) to the crystal.

#### 3.8.2 PA_ON_PCS, PA_ON_CELL

Used to switch the internal PA drivers of the RFT3100 to desired band of operation.

#### 3.8.3 TX_AGC_ADJ

TX_AGC_ADJ controls the RF power at the output of RFT3100 device.

#### 3.8.4 I_OFFSET, Q_OFFSET

Used to adjust the balance between the I and Q lines of the IFR3000 to give us orthoganality.

#### 3.8.5 SY_SENDB, SY_SDATA, SY_SCLK

Control lines for the Si4133-X1 synthesizer, used to program the three synthesizers to operate within their desired frequency range.

### 3.8.6 SBCK, SBST, SBDT

This is the serial bus interface (SBI) control lines used to program the IFR3000 and RFT 3100.

## *3.9 Power Supply*

The Aircard 555 radio draws its power from the host computer through the PCMCIA interface.

PC_VIN, +5.0Vdc is filtered directly out of the PCMCIA connector and then used to supply power to the transmitter and receiver. VBAT is further regulated down to +3.0Vdc using three separate integrated circuit regulators to provide RX_POW, TCXO_POW, TX_POW PA_BIAS and PA_3.3V, which in turn powers the receiver, FGU, and part of the transmitter respectively. Each regulator has its own individual control pin so it can be turned on and off independently.