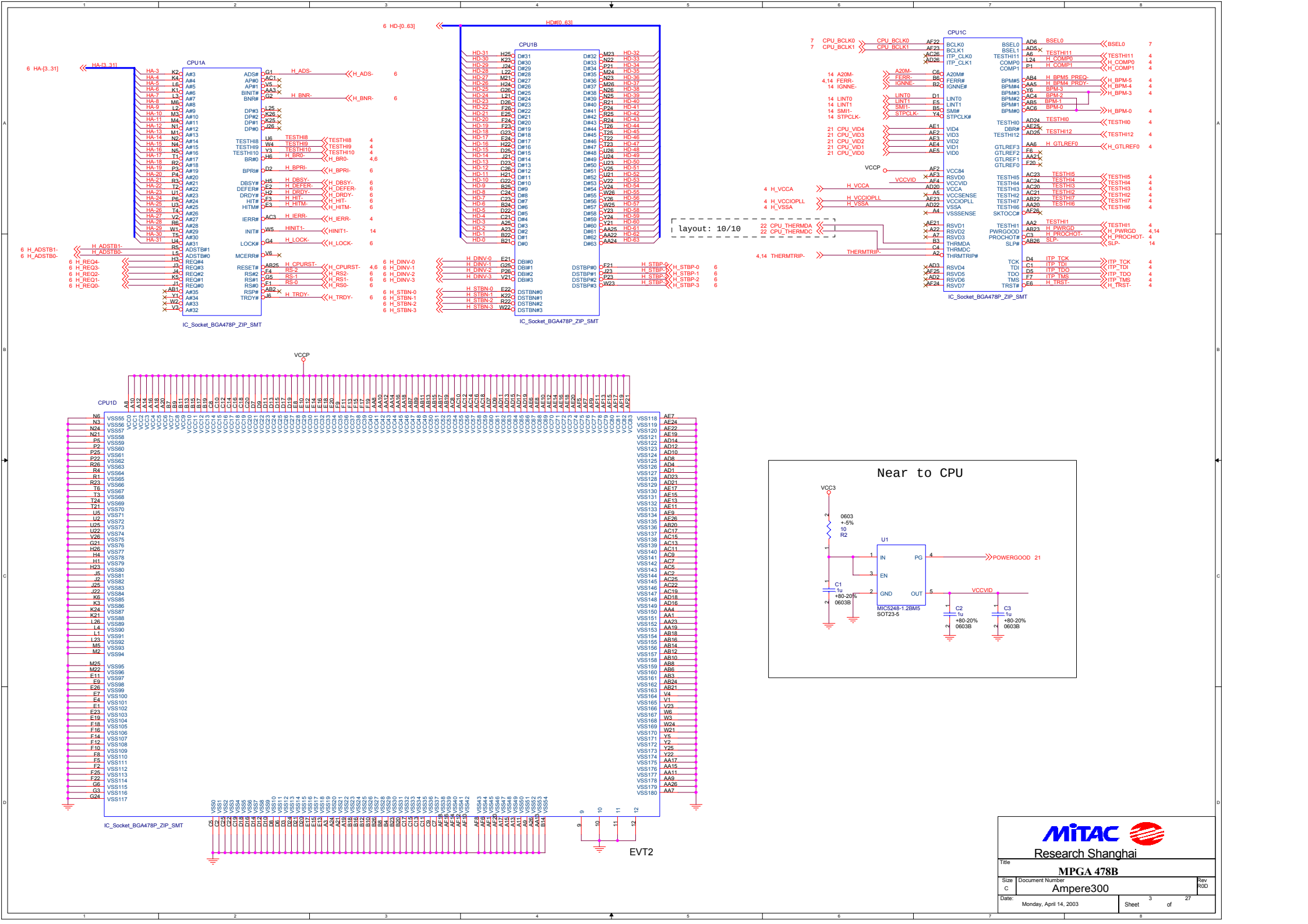
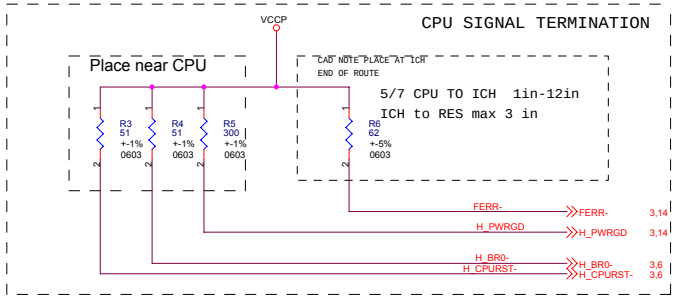
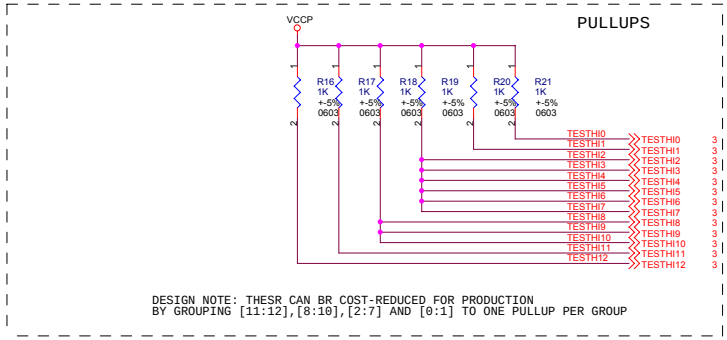

CPU1A
IC_Socket_BGA478P_ZIP_SMT
CPU1B
IC_Socket_BGA478P_ZIP_SMT
CPU1C
IC_Socket_BGA478P_ZIP_SMT
CPU1D
IC_Socket_BGA478P_ZIP_SMT
layout: 10/10
Near to CPU
MIC5248-1.2BM5
SOT23-5
EVT2
MiTAC
Research Shanghai
MPGA 478B
Ampere300
Monday, April 14, 2003

CPU SIGNAL TERMINATION



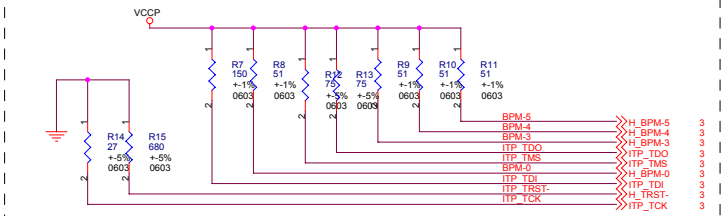
PULLUPS



DESIGN NOTE: THESR CAN BR COST-REDUCED FOR PRODUCTION
BY GROUPING [11:12],[8:10],[2:7] AND [0:1] TO ONE PULLUP PER GROUP

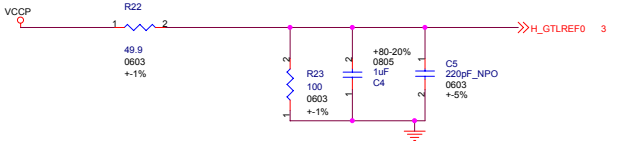
ITP/TAP TERMINATION

DESIGN NOTE: ASSMING STD AGTL+ TERMINATION VALUE OF 51 OHM, DESIGN GUIDE STILL HAS 40 OHM...



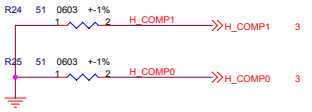
CAD NOTE: PLACE THESE RESISTORS CLOSE TO THE CPU SOCKET

GTLREF GENERATION CIRCUITS



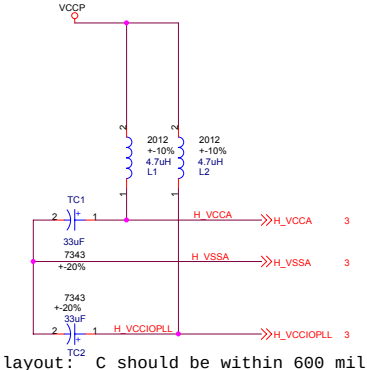
CAD NOTE: ONE 220PF CAP PER GTL REF PIN

PRECISION FSB COMPENSATION RESISTORS



Place near CPU

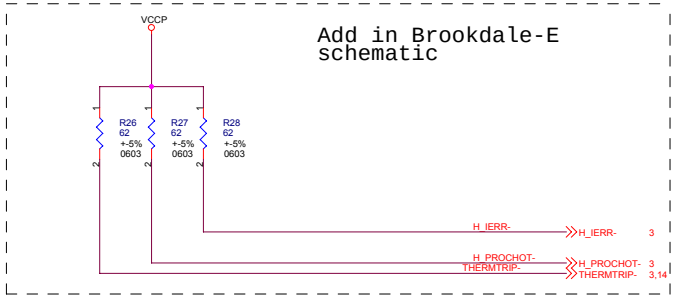
PLL SUPPLY FILTER



layout: C should be within 600 mils of VCCA and VSSA pin

L should be close to C

Trace min 12mil



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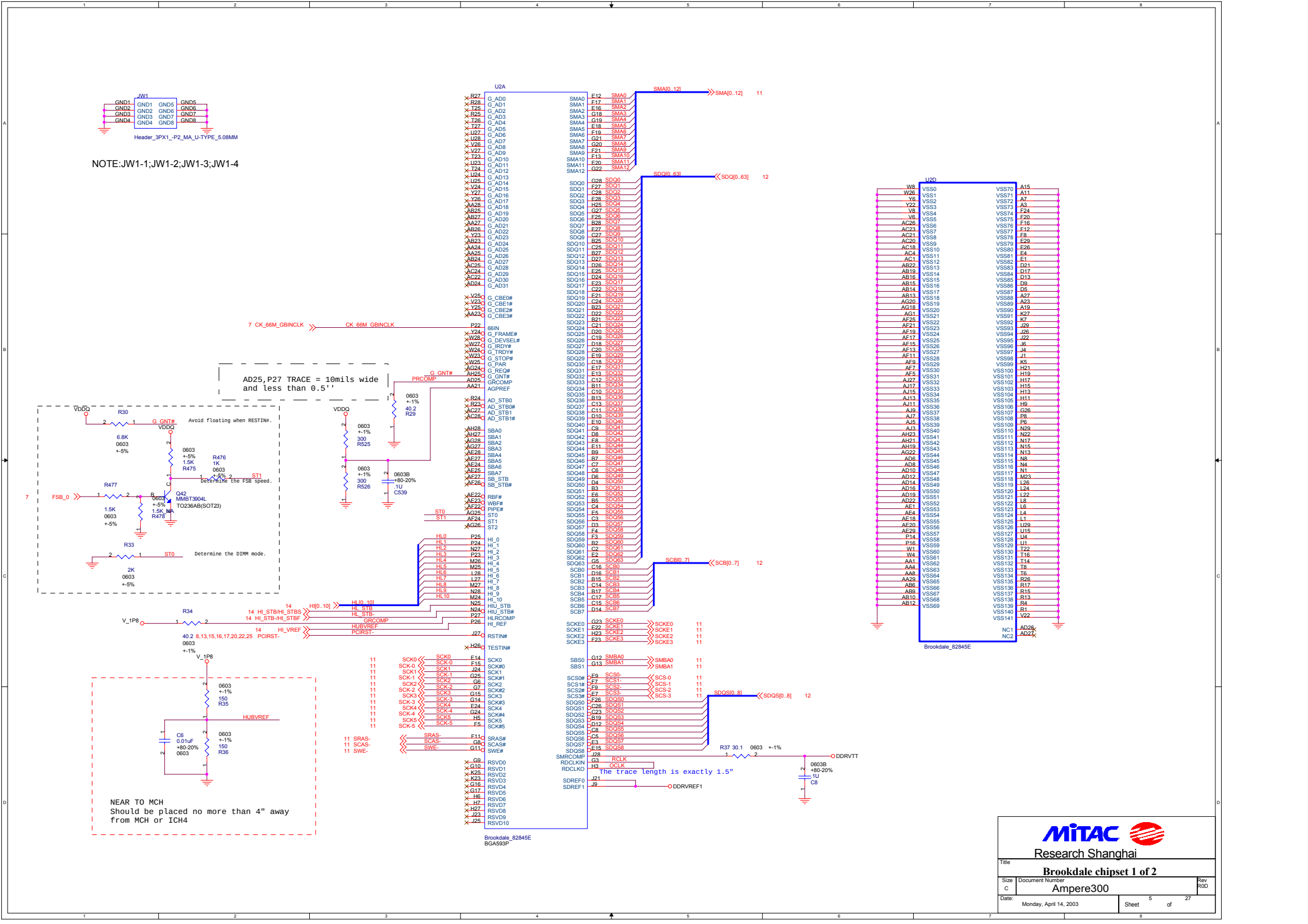
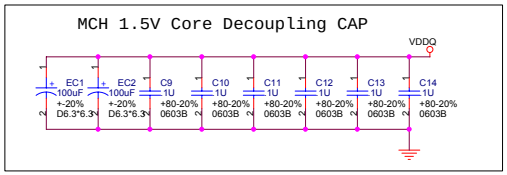
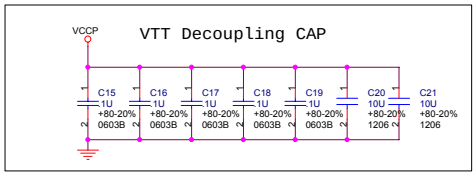
Title: CPU PULLUPS/PULLDNS/TERMINATION

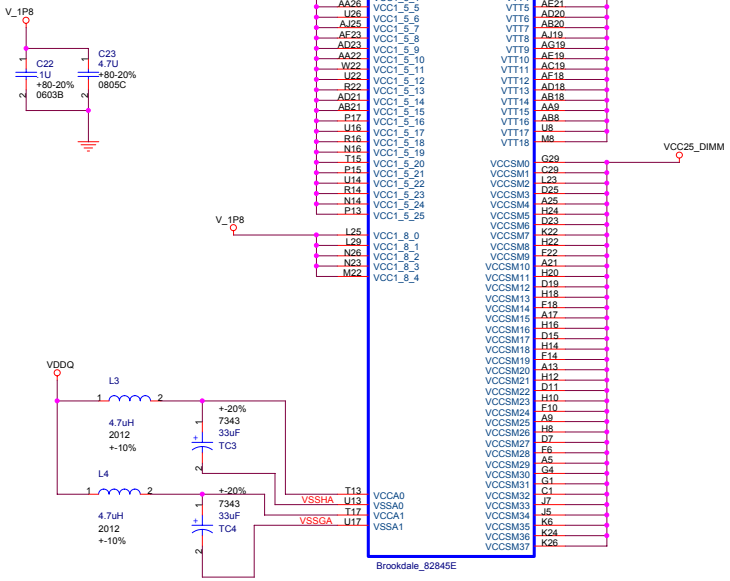
Size: C | Document Number: Ampere300 | Rev: R0D

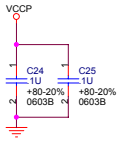
Date: Monday, April 14, 2003 | Sheet 4 of 27

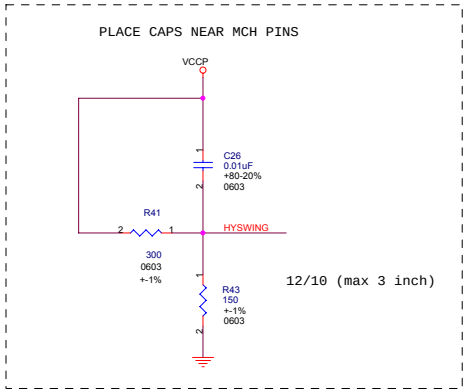

JW1
Header_3PX1_-P2_MA_U-TYPE_5.08MM
NOTE:JW1-1;JW1-2;JW1-3;JW1-4
U2A
Brookdale_82845E
BGA593P
AD25,P27 TRACE = 10mils wide
and less than 0.5''
Avoid floating when RESTIN#.
Determine the FSB speed.
Determine the DIMM mode.
The trace length is exactly 1.5"
NEAR TO MCH
Should be placed no more than 4" away
from MCH or ICH4
U2D
Brookdale_82845E
MiTAC
Research Shanghai
Brookdale chipset 1 of 2
Ampere300
Monday, April 14, 2003

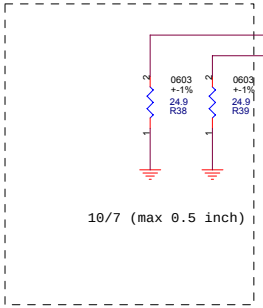


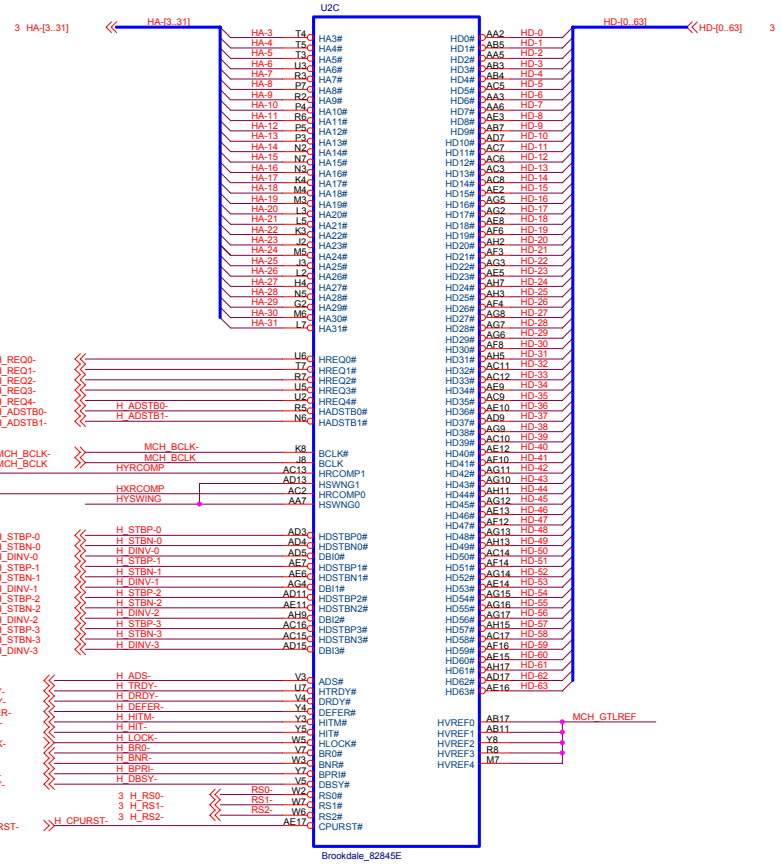


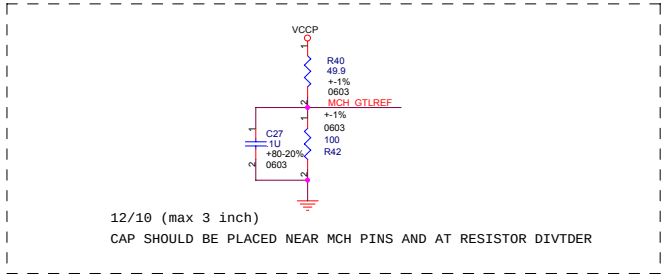












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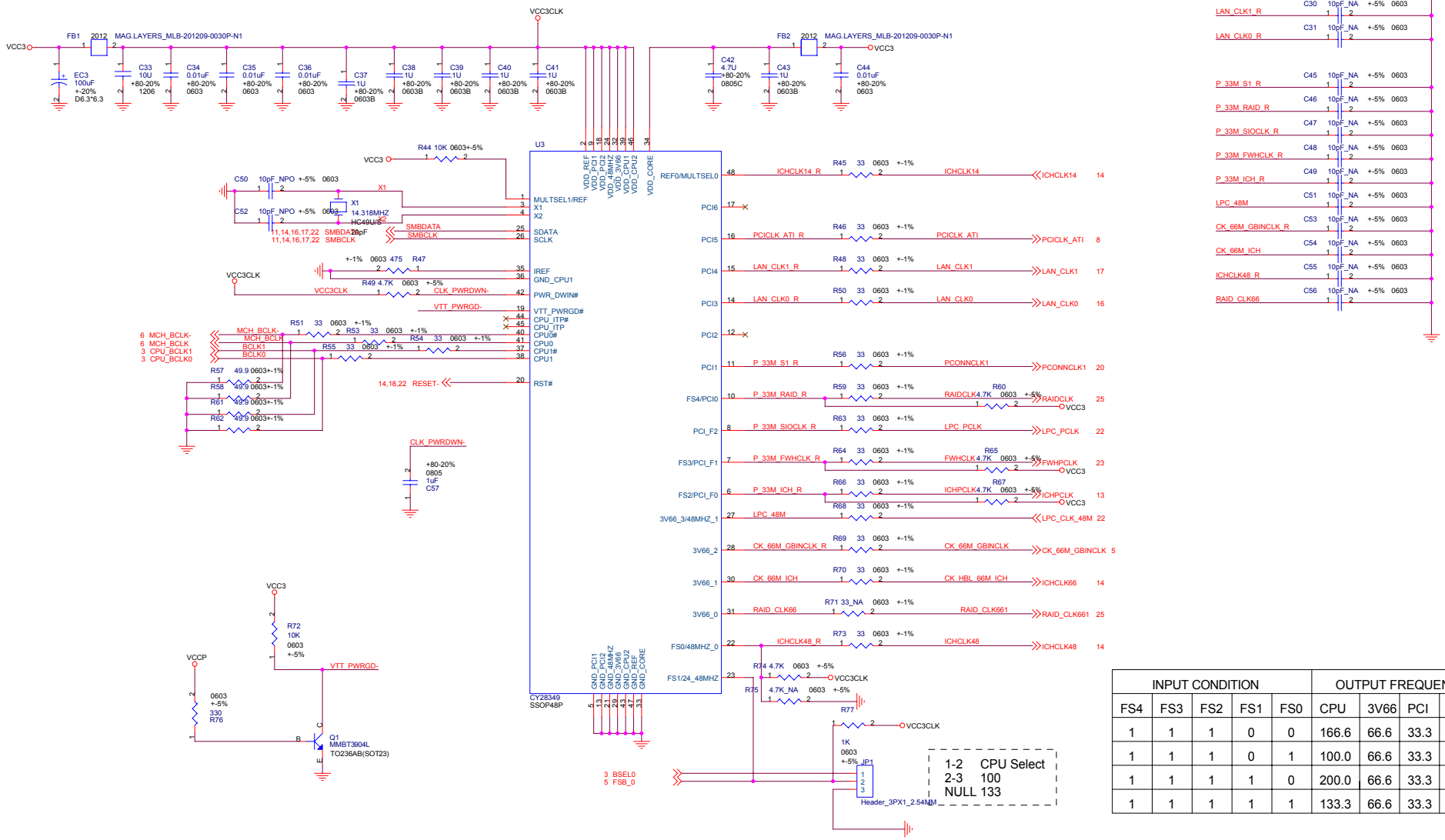
Title	Brookdale chipset 2 of 2	
Size C	Document Number Ampere300	Rev R0D
Date: Monday, April 14, 2003	Sheet 6 of 27	



INPUT CONDITION					OUTPUT FREQUENCY			
FS4	FS3	FS2	FS1	FS0	CPU	3V66	PCI	PLL Gear Constant
1	1	1	0	0	166.6	66.6	33.3	48.00741
1	1	1	0	1	100.0	66.6	33.3	48.00741
1	1	1	1	0	200.0	66.6	33.3	48.00741
1	1	1	1	1	133.3	66.6	33.3	48.00741

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Title: Clock Gen

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ATI RAGE XL:
LPVDD: TMDS PLL Power; 2.5V
LPVSS: TMDS PLL Ground;
TXVDDR: TMDS Transmitter Power; 2.5V
TXVSSR: TMDS Transmitter Ground.

This Correct Foot Print
Of D1 to D7

3 Signal
1 GND
2 VCC

REQ0
GNT0
AD17

U4A
RAGE_XL_215R3LASB41
BGA256P

X2
29.498928MHZ
HC-49U/S
20pF

J1
DSUB_15P/3R_R/A_BL5.08_PC99

MAG.LAYERS_MLB-201209-0030P-N1
MAG.LAYERS_MLB-201209-0070A-N4
MAG.LAYERS_MLB-201209-0017A-N2

Raychem_MINISMDM160-02
1812

NC7ST08
SOT23-5

BAV99
SOT23

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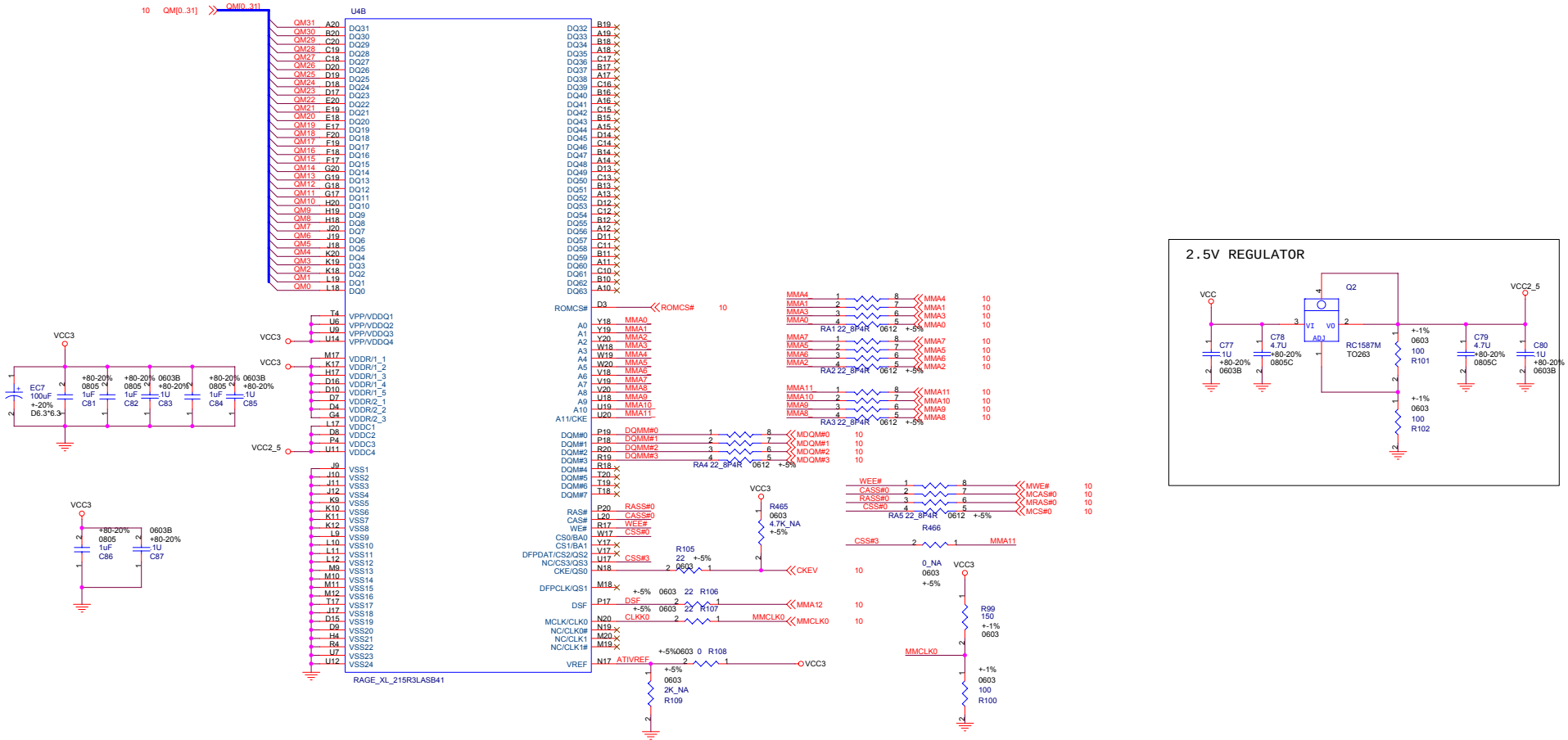
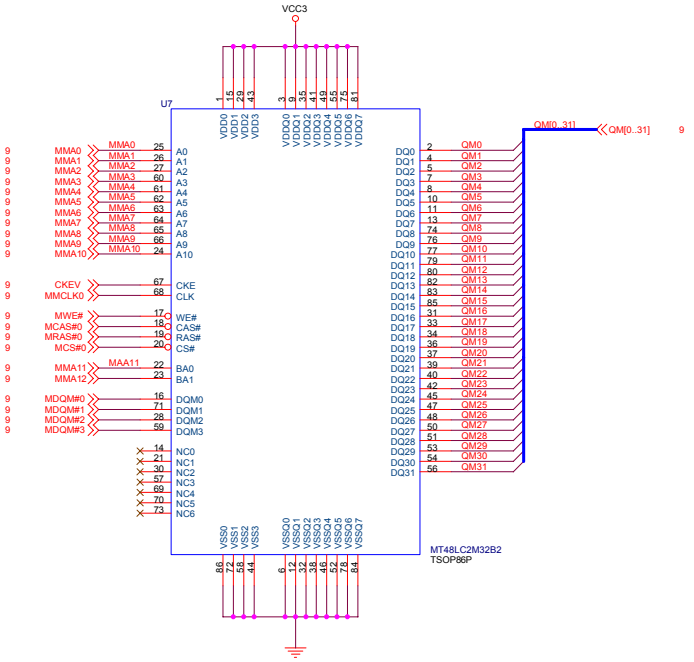
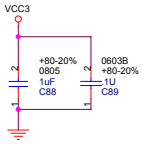
Research Shanghai

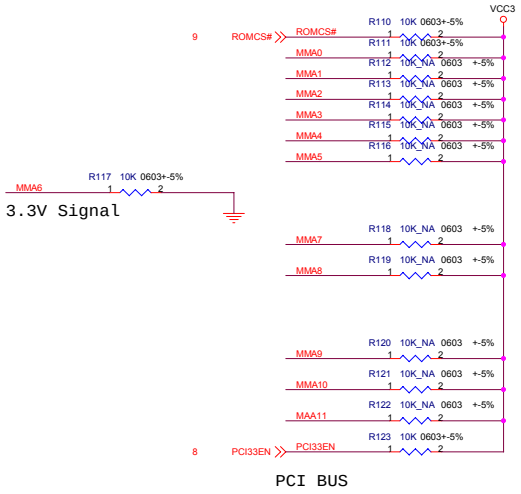
Title: ATI 1
Size: C
Document Number: Ampere300
Rev: R0D
Date: Monday, April 14, 2003
Sheet 8 of 27



MiTAC Research Shanghai			
Title: ATI 2			
Size: C	Document Number: Ampere300		Rev: R0D
Date: Monday, April 14, 2003		Sheet 9 of 27	







ROMCS#	ADD IN CARD
DNI	DON'T READ BIOS STRAPS
10K	READ BIOS STRAPS (DEFAULT)

MMA0	BUS CLOCK SELECT
	SEE TABLE BELOW

MMA2	MMA1	AGP SKEW
DNI	DNI	DEFAULT
X	X	TBD

MMA4	MMA3	1XCLK SKEW
DNI	DNI	DEFAULT
X	X	TBD

MMA5	ID DISABLE
DNI	NORMAL (DEFAULT)
10K	IDSEL DISABLE

MMA6	BUS TYPE
	SEE TABLE BELOW

MMA7	VGA DISABLE (OPTIONAL)
2-3	VGA IS ENABLED (DEFAULT)
1-2	VGA IS DISABLED

MMA8	ENINITB (OPTIONAL)
2-3	INT PIN ENABLED (DEFAULT)
1-2	INT PIN DISABLED

MMA9	IDSEL IN AGP MODE(OPTIONAL)
DNI	AD16 (DEFAULT)
10K	AD17

MMA11	MMA10	AGP VCO GAIN
DNI	DNI	DEFAULT
X	X	TBD

PCI133EN	PCI BUS
	AGP BUS

MiTAC Research Shanghai

Title: ATI MEM

Size	Document Number	Rev
C	Ampere300	R0D

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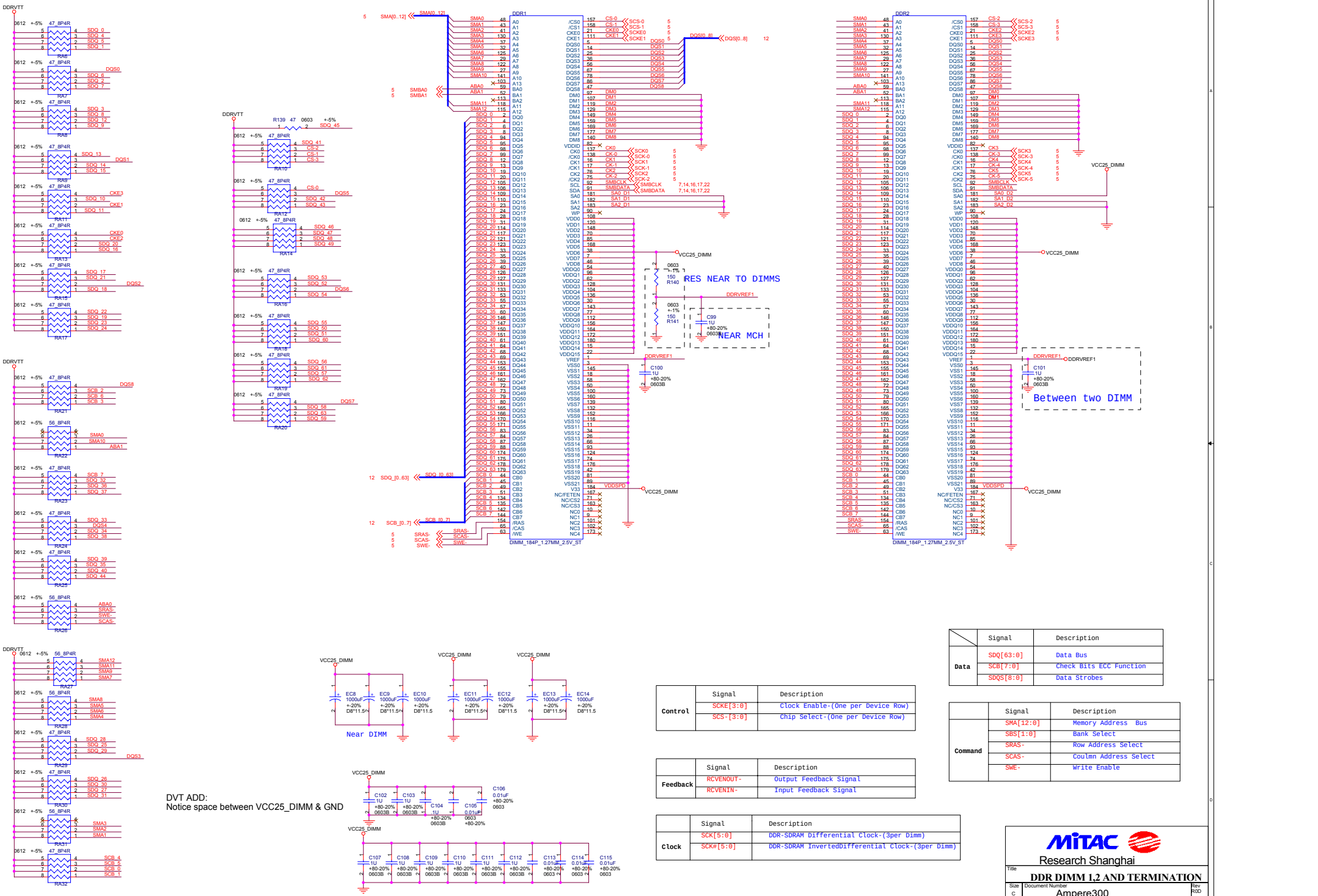


	Signal	Description
Data	SDQ[63:0]	Data Bus
	SCB[7:0]	Check Bits ECC Function
	SDQS[8:0]	Data Strobes

	Signal	Description
Control	SCKE[3:0]	Clock Enable-(One per Device Row)
	SCS-[3:0]	Chip Select-(One per Device Row)

	Signal	Description
Command	SMA[12:0]	Memory Address Bus
	SBS[1:0]	Bank Select
	SRAS-	Row Address Select
	SCAS-	Coulmn Address Select
	SWE-	Write Enable

	Signal	Description
Feedback	RCVENOUT-	Output Feedback Signal
	RCVENIN-	Input Feedback Signal

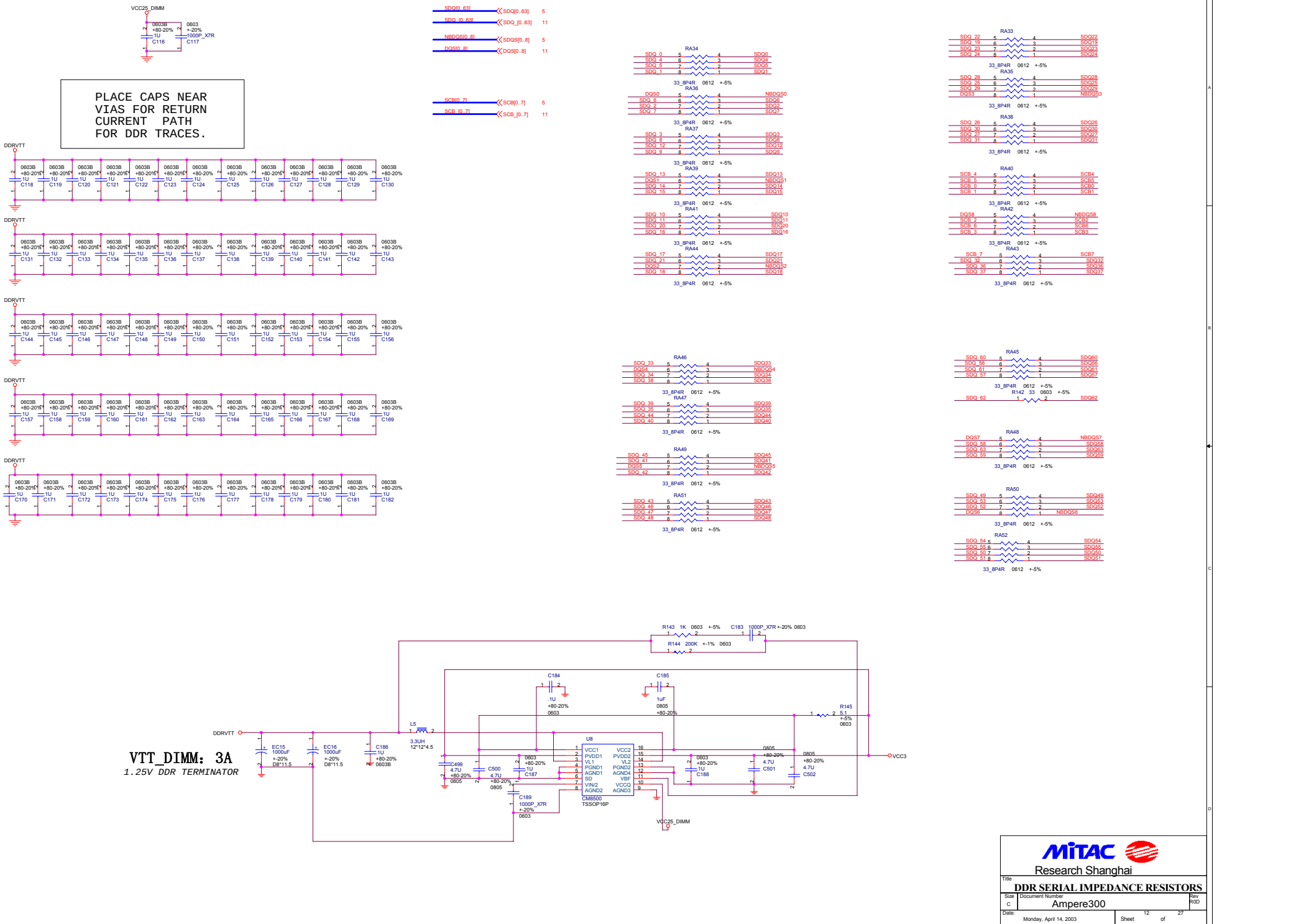
	Signal	Description
Clock	SCK[5:0]	DDR-SDRAM Differential Clock-(3per Dimm)
	SCK#[5:0]	DDR-SDRAM InvertedDifferential Clock-(3per Dimm)

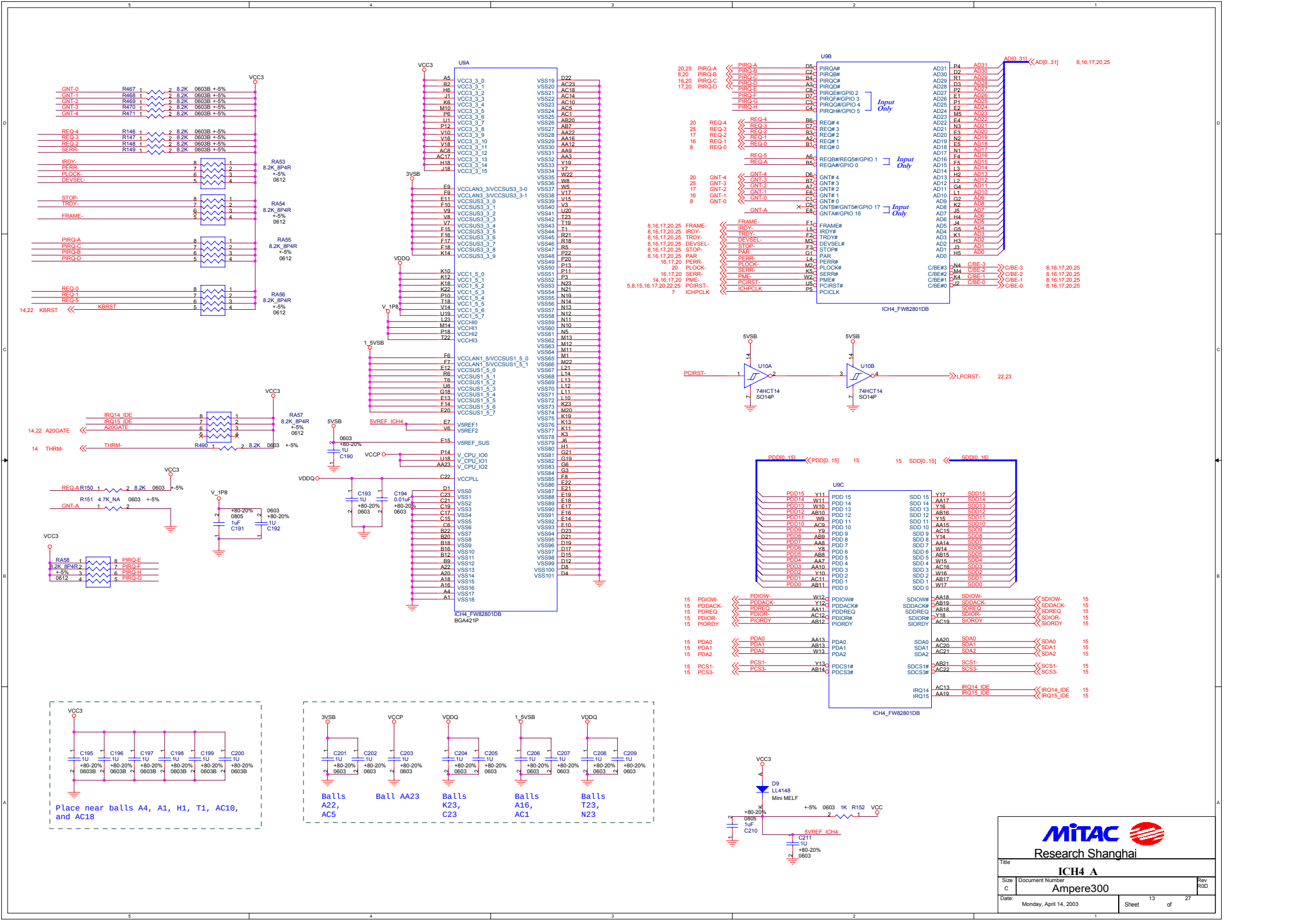
MiTAC Research Shanghai

Title: DDR DIMM 1,2 AND TERMINATION

Size	Document Number	Rev
C	Ampere300	ROD

Date: Monday, April 14, 2003 Sheet 11 of 27


VCC25_DIMM
PLACE CAPS NEAR VIAS FOR RETURN CURRENT PATH FOR DDR TRACES.
DDRVTT
SDQ[0..63]
SDQ_[0..63]
NBDQS[0..8]
DQS[0..8]
SCB[0..7]
SCB_[0..7]
RA33
RA34
RA35
RA36
RA37
RA38
RA39
RA40
RA41
RA42
RA43
RA44
RA45
RA46
RA47
RA48
RA49
RA50
RA51
RA52
33_8P4R 0612 +-5%
R143 1K 0603 +-5%
C183 1000P_X7R +-20% 0603
R144 200K +-1% 0603
R142 33 0603 +-5%
C184 .1U +80-20% 0603
C185 1uF 0805 +80-20%
R145 5.1 +-5% 0603
L5 3.3UH 12*12*4.5
EC15 1000uF +-20% D8*11.5
EC16 1000uF +-20% D8*11.5
C186 1U +80-20% 0603B
U8
CM8500 TSSOP16P
VCC1 PVDD1 VL1 PGND1 AGND1 SD VIN/2 AGND2
VCC2 PVDD2 VL2 PGND2 AGND4 VBF VCCQ AGND3
C499 4.7U +80-20% 0805
C500 4.7U +80-20% 0805
C187 1U +80-20% 0603
C188 1U +80-20% 0603
C501 4.7U +80-20% 0805
C502 4.7U +80-20% 0805
C189 1000P_X7R +-20% 0603
VCC3
VTT_DIMM: 3A
1.25V DDR TERMINATOR
MiTAC
Research Shanghai
Title
DDR SERIAL IMPEDANCE RESISTORS
Size C
Document Number Ampere300
Rev R0D
Date: Monday, April 14, 2003
Sheet 12 of 27


U9A
ICH4_FW82801DB
BGA421P
U9B
ICH4_FW82801DB
U9C
ICH4_FW82801DB
U10A
U10B
74HCT14
SO14P
Place near balls A4, A1, H1, T1, AC10, and AC18
Balls A22, AC5
Ball AA23
Balls K23, C23
Balls A16, AC1
Balls T23, N23
Input Only
MiTAC
Research Shanghai
Title
ICH4_A
Size C
Document Number Ampere300
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Date: Monday, April 14, 2003
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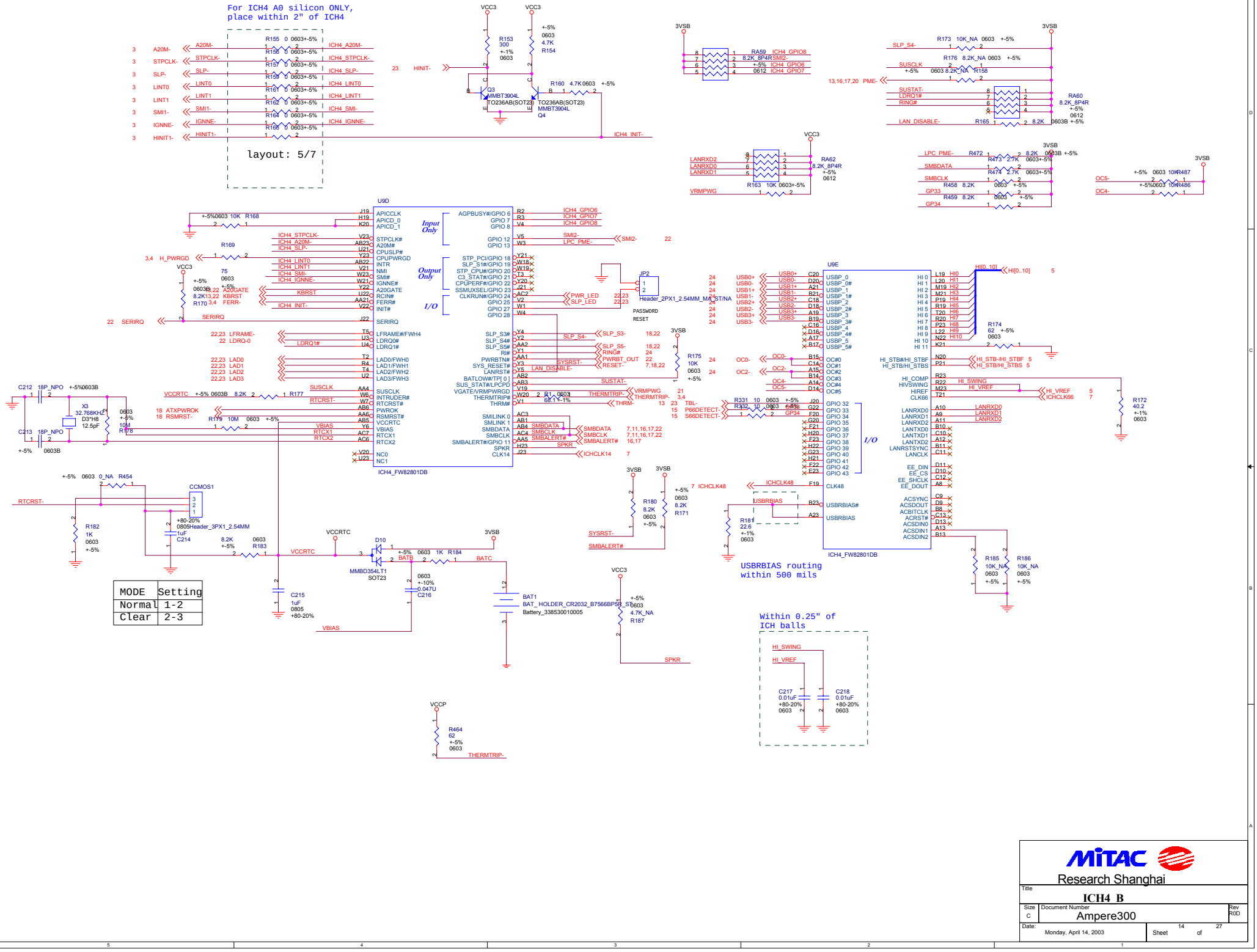
For ICH4 A0 silicon ONLY,
place within 2" of ICH4
layout: 5/7
U9D
ICH4_FW82801DB
U9E
ICH4_FW82801DB
JP2
Header_2PX1_2.54MM_MA_ST/NA
PASSWORD
RESET
CCMOS1
Header_3PX1_2.54MM
MMBD354LT1
SOT23
BAT1
BAT_HOLDER_CR2032_B7566BP5R_ST
Battery_338530010005
Q3
MMBT3904L
TO236AB(SOT23)
Q4
MMBT3904L
TO236AB(SOT23)
X3
32.768KHZ
12.5pF
USBRBIAS routing
within 500 mils
Within 0.25" of
ICH balls
MODE Setting
Normal 1-2
Clear 2-3
MiTAC
Research Shanghai
Title
ICH4_B
Size C
Document Number
Ampere300
Rev R0D
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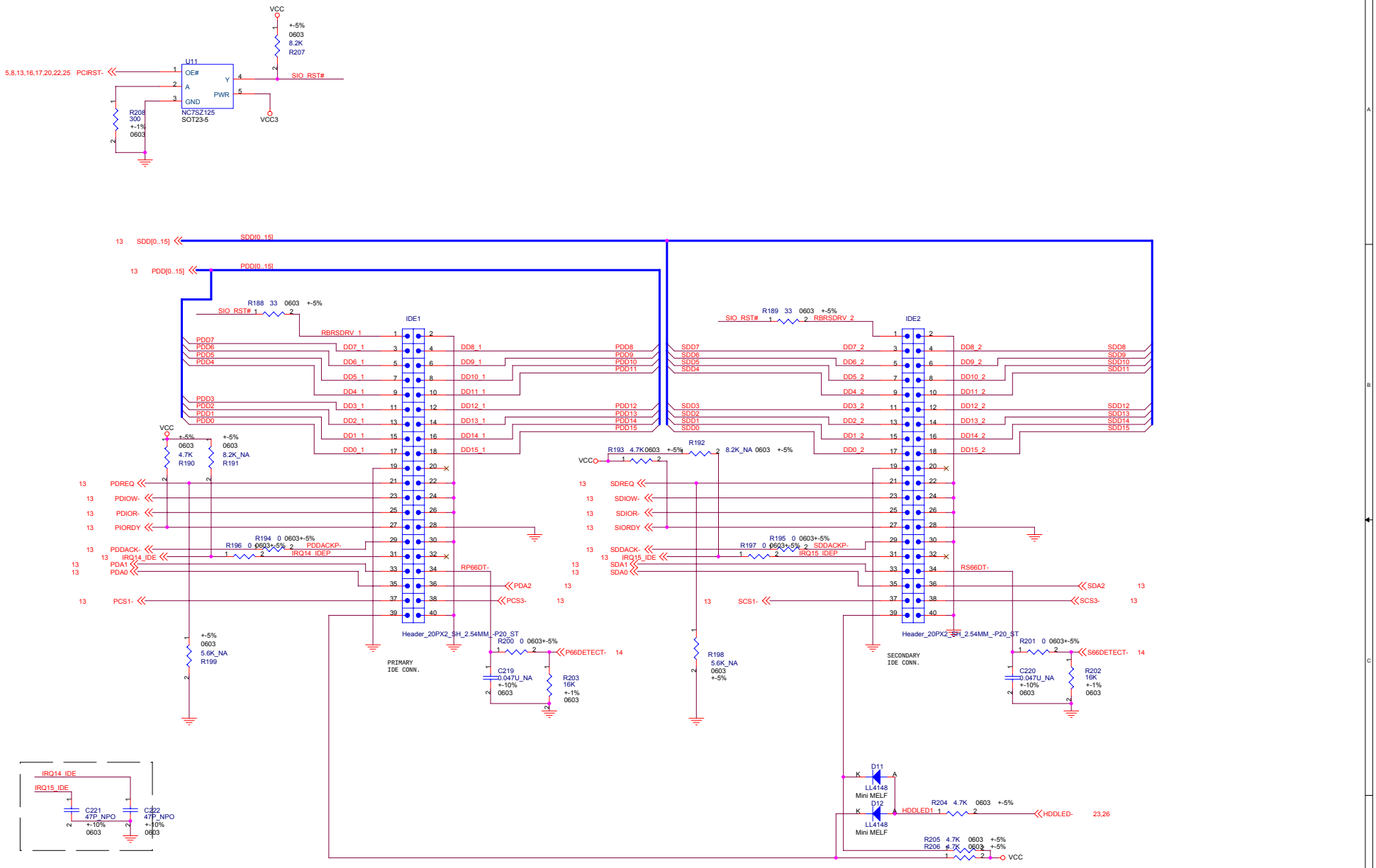
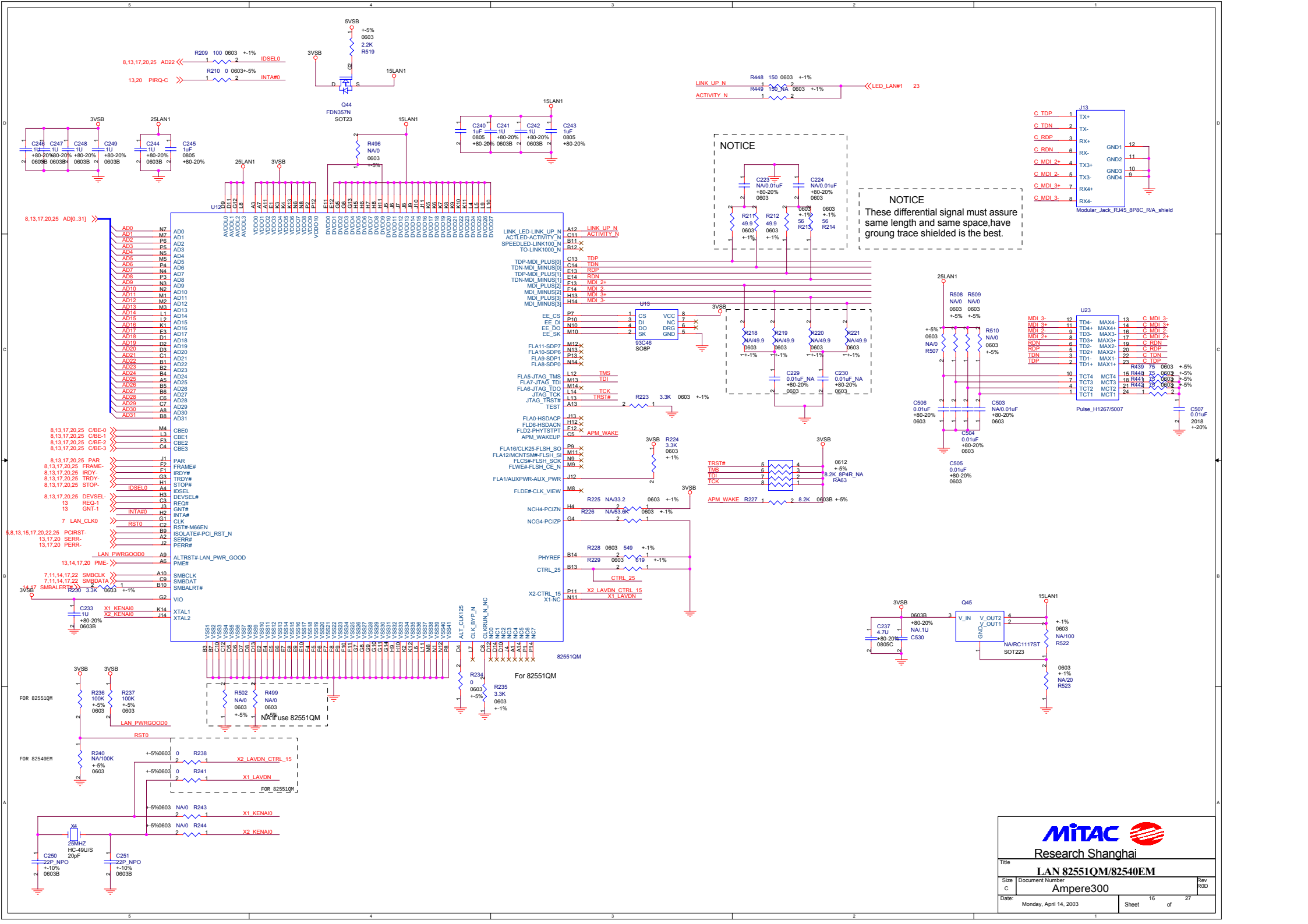
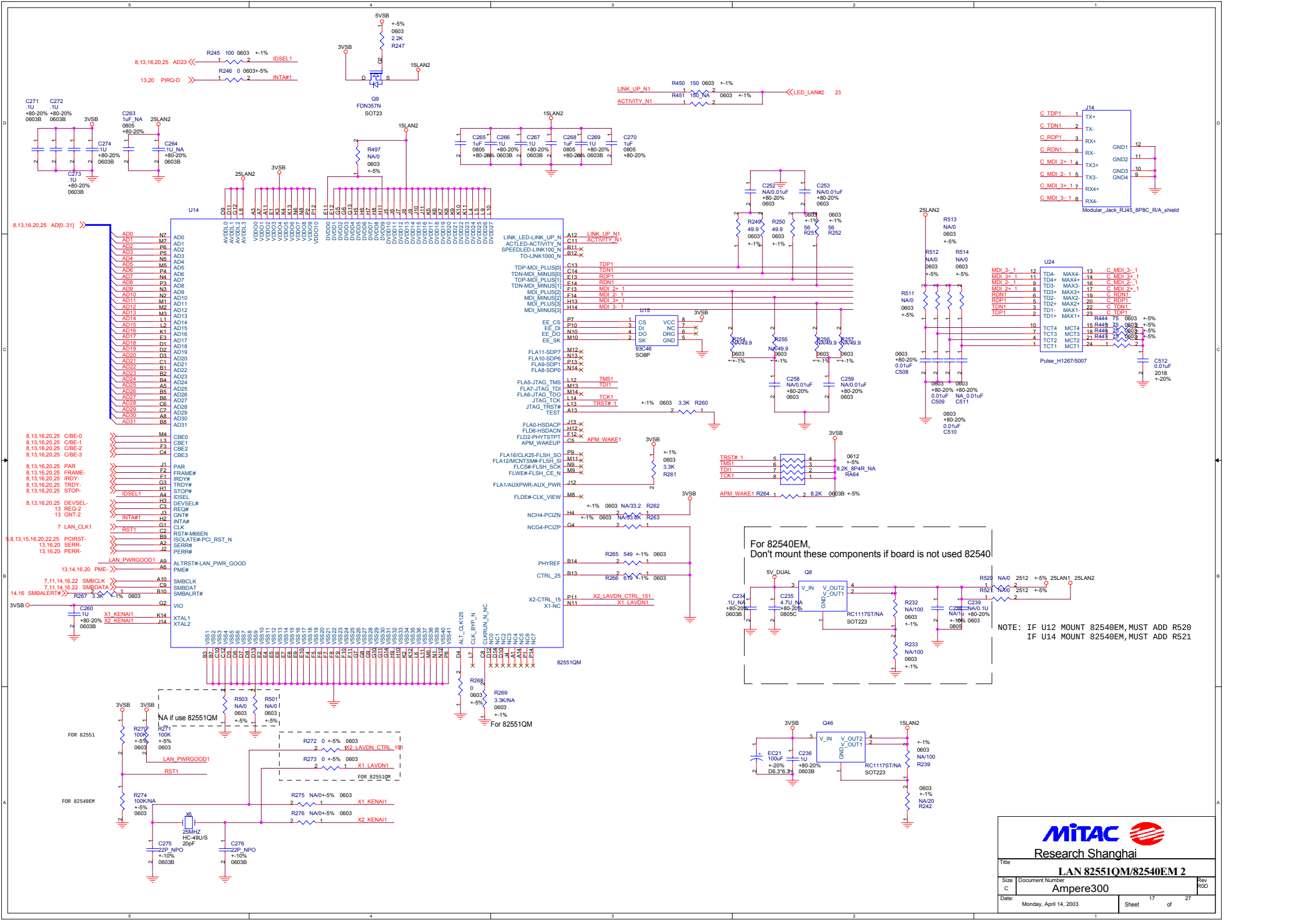


MiTAC Research Shanghai		
Title: IDE CONN 1,2		
Size: C	Document Number: Ampere300	Rev: R0D
Date: Monday, April 14, 2003	Sheet 15 of 27	


NOTICE
These differential signal must assure same length and same space,have groung trace shielded is the best.
For 82551QM
NA if use 82551QM
FOR 82551QM
FOR 82540EM
Modular_Jack_RJ45_8P8C_R/A_shield
Pulse_H1267/5007
93C46
SO8P
82551QM
Research Shanghai
LAN 82551QM/82540EM
Ampere300
Monday, April 14, 2003


U14
82551QM
U15
93C46
SO8P
U24
Pulse_H1267/5007
Modular_Jack_RJ45_8P8C_R/A_shield
Q8
Q46
RC1117ST/NA
SOT223
X5
25MHZ
HC-49U/S
20pF
For 82551QM
NA if use 82551QM
For 82540EM,
Don't mount these components if board is not used 82540
NOTE: IF U12 MOUNT 82540EM,MUST ADD R520
IF U14 MOUNT 82540EM,MUST ADD R521
MiTAC
Research Shanghai
Title
LAN 82551QM/82540EM 2
Size C
Document Number
Ampere300
Rev R0D
Date: Monday, April 14, 2003
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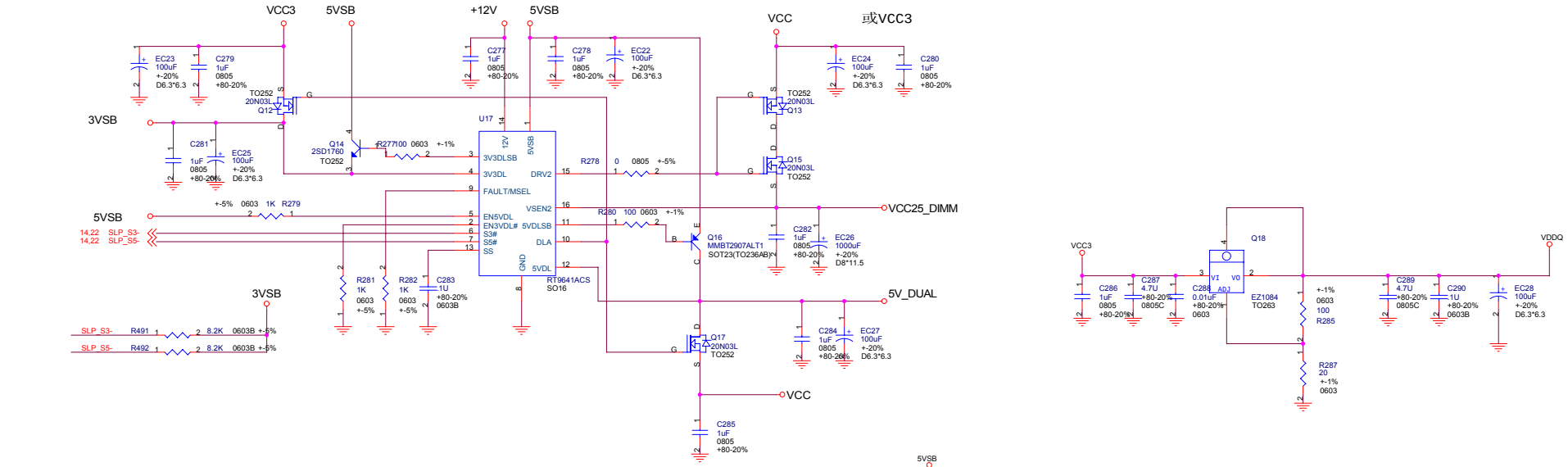
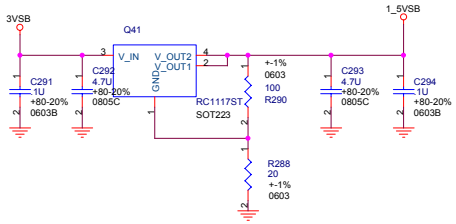
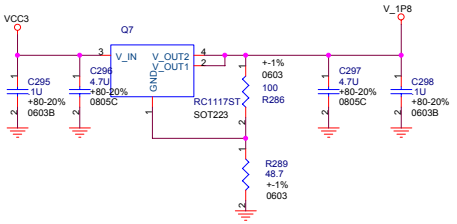
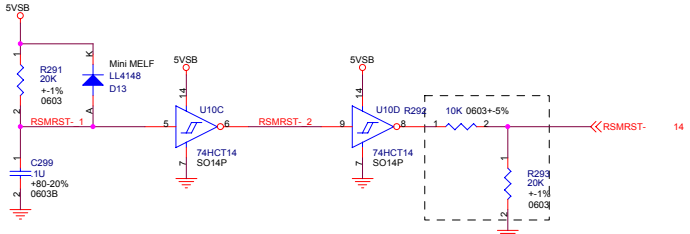
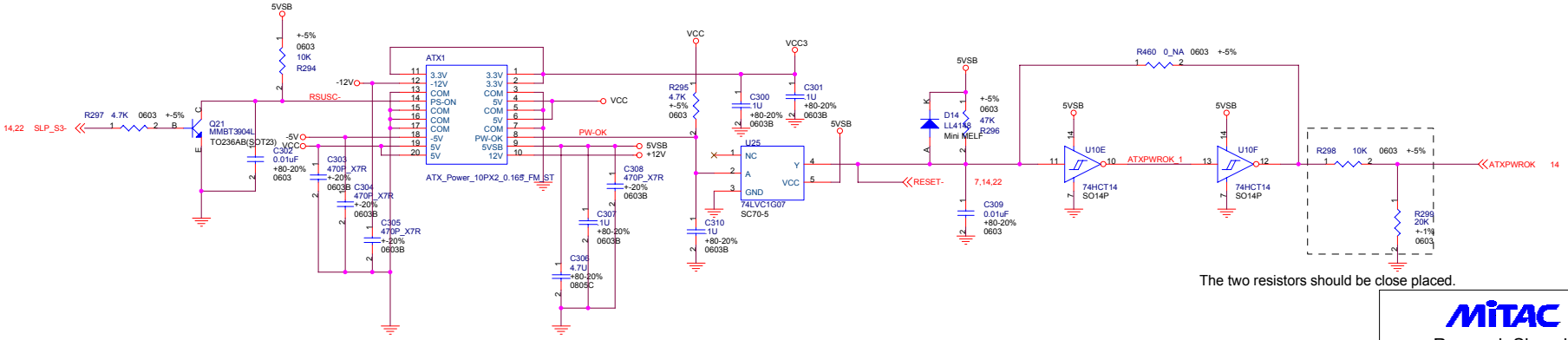








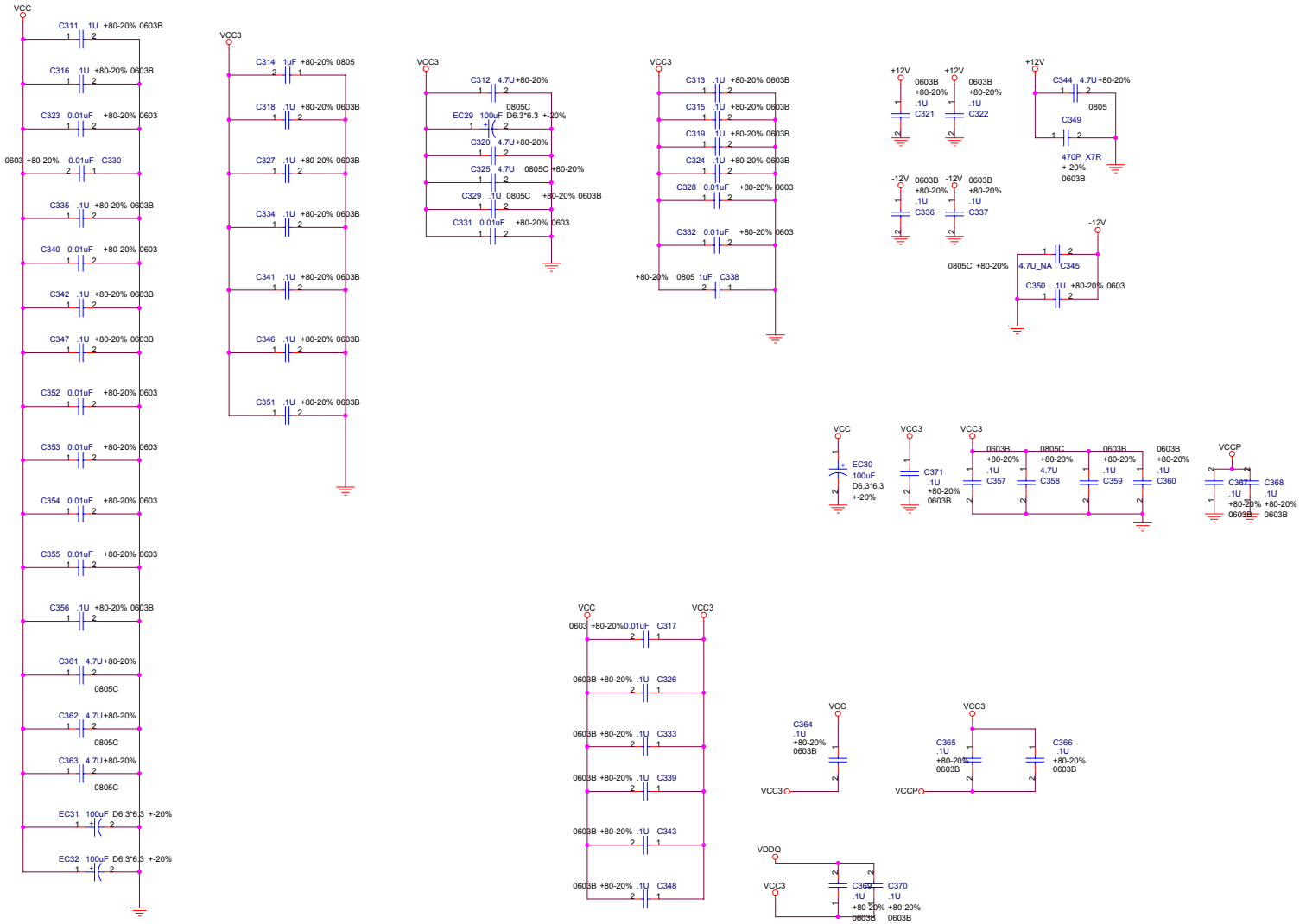
The two resistors should be close placed.



The two resistors should be close placed.

MiTAC Research Shanghai

Title	POWER	
Size: C	Document Number: Ampere300	Rev: R0D
Date: Monday, April 14, 2003	Sheet 18 of 27	



MiTAC Research Shanghai

Title: Decoupling/EMI caps

Size	Document Number	Rev
C	Ampere300	R0D

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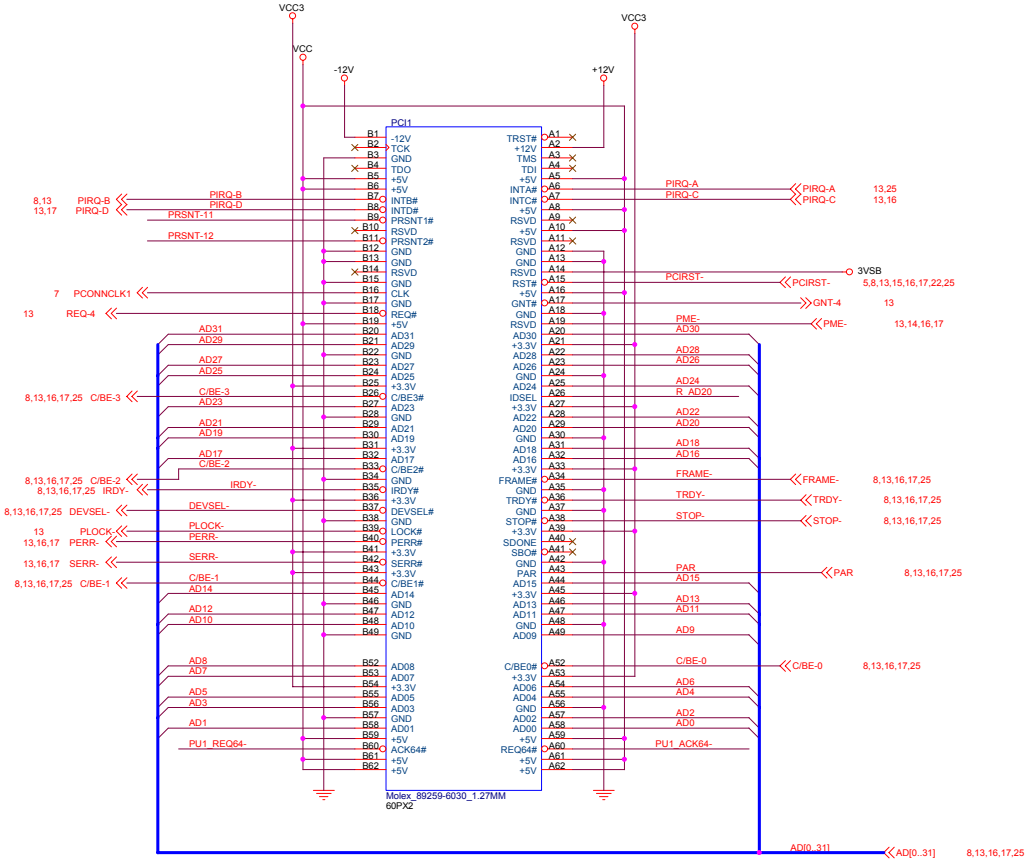
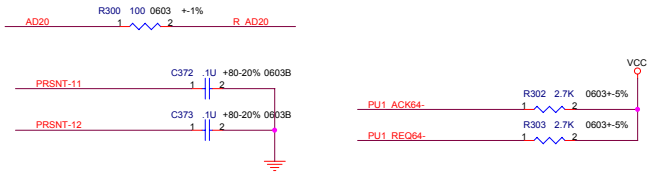


AD=20
PCI SLOT 1



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Title	PCI1 & PCI2	
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Infineon - 10N03 / 05N03
Fairchild - 7030BL / 7030BL
CET - 7030L / 8030L
GS - 70N03 / 75N03
IR - 3704S / 3711

Rubycon / Panasonic / Chemi-Con

+12V_POWER L6 0.5uH D12*P5

EC33 1200uF +-20% D10*23
EC34 1200uF +-20% D10*23
EC35 1200uF +-20% D10*23
EC36 1200uF +-20% D10*23

ATX2 MA/.1/GOLD

3 POWERGOOD

U18 CS5301 SOP32P

C377 2200P_X7R
C378 0603B +-10%
C379 0603B +80-20% .1U
C382 0.01uF_NA +80-20% 0603
C383 560p_NA +-10% 0603
C384 0.01uF_NA +80-20% 0603
330pF_NA 0603 +-20%
R309 10K 0603+-5%
R311 0 0805 +-5%
R312 20K 0603 +-1%
R313 82K +-5% 0603
R314 30K +-1% 0603
R527 NA 0603 +-5%
R315 5.6K

14 VRMPWG

C387 47P_NA +-10% 0603

R306 0 0805 +-5%
C376 1uF 0805 +80-20%
D16 BAT54SLT1 SOT23
SOD123 MBR0520 D15
R307 1 +-5% 0805
R308 1 +-5% 0805
R310 56K 0603 +-5%

Q22 FDP7030BL TO220
Q23 FDP7030BL TO220
Q24 FDP7030BL TO220
Q25 FDP7030BL TO220
Q26 FDP7030BL TO220
Q27 FDP7030BL TO220

C380 1uF 0805 +80-20%
C381 4.7U +80-20% 0805C
C385 1uF 0805 +80-20%
C386 4.7U +80-20% 0805C
C391 1uF 0805 +80-20%
C392 4.7U +80-20% 0805C

L7 0.43uH D18*P7 +-20%
L8 0.43uH D18*P7 +-20%
L9 0.43uH D18*P7 +-20%

C388 1uF 0805 +80-20%
C389 1uF 0805 +80-20%
C390 1uF 0805 +80-20%

R316 2.2K 0603 +-5%
C394 .1U +80-20% 0603B
R317 3.3K +-1% 0603
C393 0.01uF +80-20% 0603
C395 0.01uF +80-20% 0603
C396 0.01uF +80-20% 0603

R318 16K 0603 +-1%
R319 16K 0603 +-1%
R320 16K 0603 +-1%

C533,C535,C536 NEAR CS5301 INPUT PIN

C528,C529,C530 NEAR CS5301 OUTPUT PIN

JS1 JP_SMT4_DFS_NA JP_NET53
JS2 JP_SMT4_DFS_NA JP_NET53
JS3 JP_SMT4_DFS_NA JP_NET53

J6 WS111R_HeatSink

PWM USE HEATSINK HOLES

R321 1K 0603+-5%
RA65 1K_8P4R +-5% 0612

R322 0_NA 0603 +-5%
RA66 0_8P4R_NA +-5% 0612

Rubycon / Panasonic / Chemi-Con

EC37 750uF +50-10% D10*10.5
EC38 750uF +50-10% D10*10.5
EC39 750uF +50-10% D10*10.5
EC40 750uF +50-10% D10*10.5
EC41 750uF +50-10% D10*10.5
EC42 750uF +50-10% D10*10.5
EC43 750uF +50-10% D10*10.5
EC44 750uF +50-10% D10*10.5
EC45 750uF +50-10% D10*10.5
EC46 2200uF +-20% D10*20
EC47 2200uF +-20% D10*20
EC48 2200uF +-20% D10*20
EC53 750uF +50-10% D10*10.5

C397–C406 10U +80-20% 1206
C408–C417 10U +80-20% 1206
C418–C427 10U +80-20% 1206
C428–C435 10U +80-20% 1206

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Title	VRM9.2	
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PSON active strapping
IN : PSON is high active (push-pull output)
OUT: PSON is low active (open-drain output)

LPC Base address strapping
IN : 4E
OUT: 2E

VID switch circuit

FDD Pull ups

LCD Interface

EVT2

Decoupling Caps

Title	LPC 87366
Size	C
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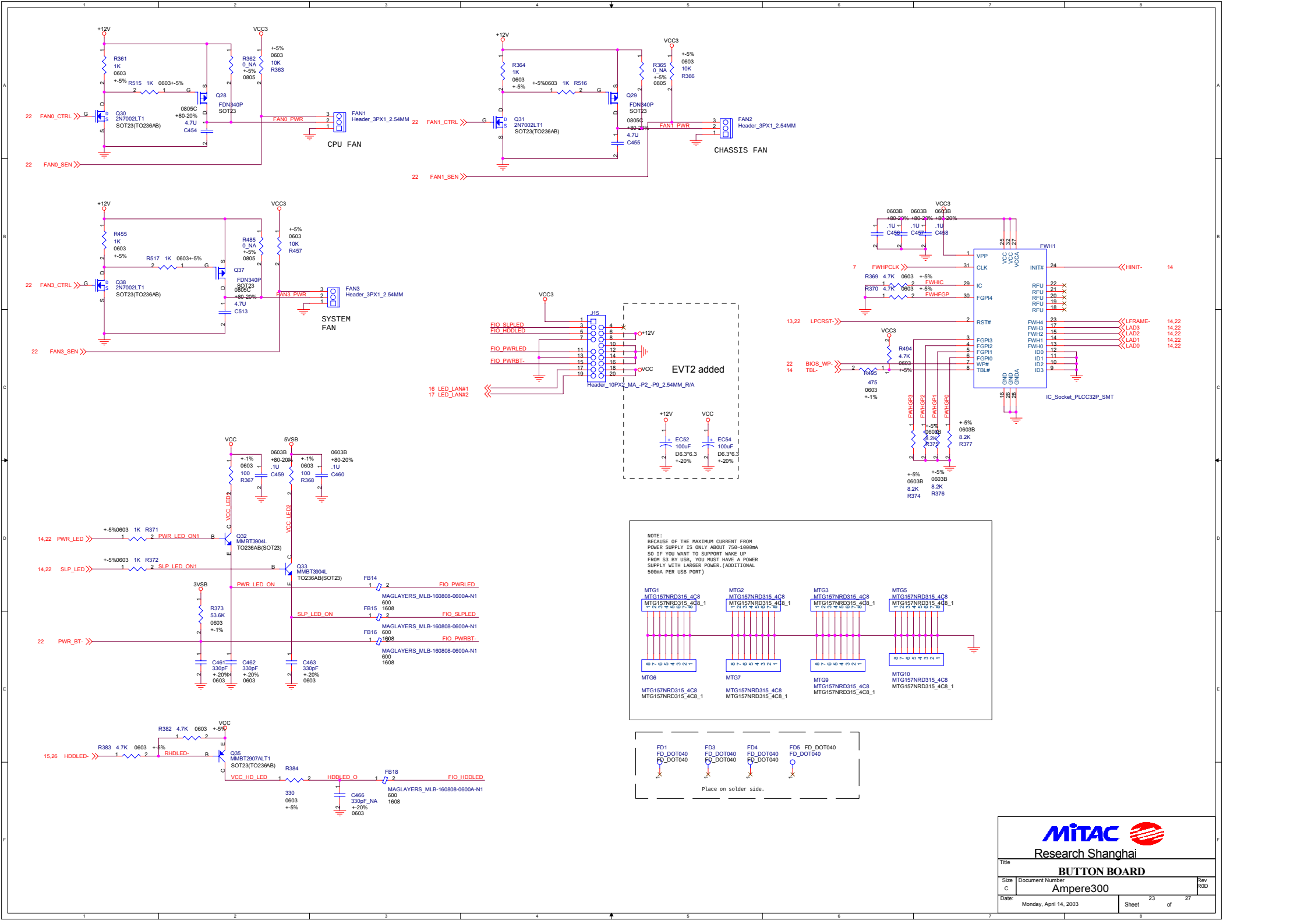
+12V
VCC3
R361 1K 0603 +-5%
R362 0_NA +-5% 0805
+-5% 0603 10K R363
R515 1K 0603+-5%
Q28 FDN340P SOT23
Q30 2N7002LT1 SOT23(TO236AB)
0805C +80-20% 4.7U C454
22 FAN0_CTRL
22 FAN0_SEN
FAN0_PWR
FAN1 Header_3PX1_2.54MM
CPU FAN
R364 1K 0603 +-5%
R365 0_NA +-5% 0805
+-5% 0603 10K R366
R516 1K 0603 +-5%
Q29 FDN340P SOT23
Q31 2N7002LT1 SOT23(TO236AB)
0805C +80-20% 4.7U C455
22 FAN1_CTRL
22 FAN1_SEN
FAN1_PWR
FAN2 Header_3PX1_2.54MM
CHASSIS FAN
R455 1K 0603 +-5%
R485 0_NA +-5% 0805
+-5% 0603 10K R457
R517 1K 0603+-5%
Q37 FDN340P SOT23
Q38 2N7002LT1 SOT23(TO236AB)
0805C +80-20% 4.7U C513
22 FAN3_CTRL
22 FAN3_SEN
FAN3_PWR
FAN3 Header_3PX1_2.54MM
SYSTEM FAN
J15
FIO_SLPLED
FIO_HDDLED
FIO_PWRLED
FIO_PWRBT-
16 LED_LAN#1
17 LED_LAN#2
Header_10PX2_MA_-P2_-P9_2.54MM_R/A
EVT2 added
EC52 100uF D6.3*6.3 +-20%
EC54 100uF D6.3*6.3 +-20%
0603B +80-20% .1U C456
C457
C458
FWH1
VPP
CLK
IC
FGPI4
RST#
FGPI3
FGPI2
FGPI1
FGPI0
WP#
TBL#
INIT#
RFU
FWH4
FWH3
FWH2
FWH1
FWH0
ID0
ID1
ID2
ID3
GND
GNDA
7 FWHPCLK
R369 4.7K 0603 +-5% FWHIC
R370 4.7K 0603 +-5% FWHFGP
13,22 LPCRST-
22 BIOS_WP-
14 TBL-
R494 4.7K 0603 +-5%
R495 475 0603 +-1%
FWHGP3
FWHGP2
FWHGP1
FWHGP0
8.2K R377
8.2K R374
8.2K R376
HINIT-
LFRAME-
LAD3
LAD2
LAD1
LAD0
IC_Socket_PLCC32P_SMT
VCC
5VSB
+-1% 0603 100 R367
+-1% 0603 100 R368
0603B +80-20% .1U C459
C460
VCC_LED1
VCC_LED2
14,22 PWR_LED
14,22 SLP_LED
+-5%0603 1K R371
+-5%0603 1K R372
PWR_LED_ON1
SLP_LED_ON1
Q32 MMBT3904L TO236AB(SOT23)
Q33 MMBT3904L TO236AB(SOT23)
3VSB
PWR_LED_ON
SLP_LED_ON
R373 53.6K 0603 +-1%
22 PWR_BT-
C461 330pF +-20% 0603
C462 330pF +-20% 0603
C463 330pF +-20% 0603
FB14 FB15 FB16
MAGLAYERS_MLB-160808-0600A-N1 600 1608
FIO_PWRLED
FIO_SLPLED
FIO_PWRBT-
R382 4.7K 0603 +-5%
R383 4.7K 0603 +-5%
15,26 HDDLED-
RHDLED-
Q35 MMBT2907ALT1 SOT23(TO236AB)
VCC_HD_LED
R384 330 0603 +-5%
HDDLED_O
C466 330pF_NA +-20% 0603
FB18
FIO_HDDLED
NOTE:
BECAUSE OF THE MAXIMUM CURRENT FROM POWER SUPPLY IS ONLY ABOUT 750-1000mA SO IF YOU WANT TO SUPPORT WAKE UP FROM S3 BY USB, YOU MUST HAVE A POWER SUPPLY WITH LARGER POWER.(ADDITIONAL 500mA PER USB PORT)
MTG1 MTG2 MTG3 MTG5
MTG157NRD315_4C8
MTG157NRD315_4C8_1
MTG6 MTG7 MTG9 MTG10
FD1 FD_DOT040
FD3 FD_DOT040
FD4 FD_DOT040
FD5 FD_DOT040
Place on solder side.
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Research Shanghai
Title
BUTTON BOARD
Size C
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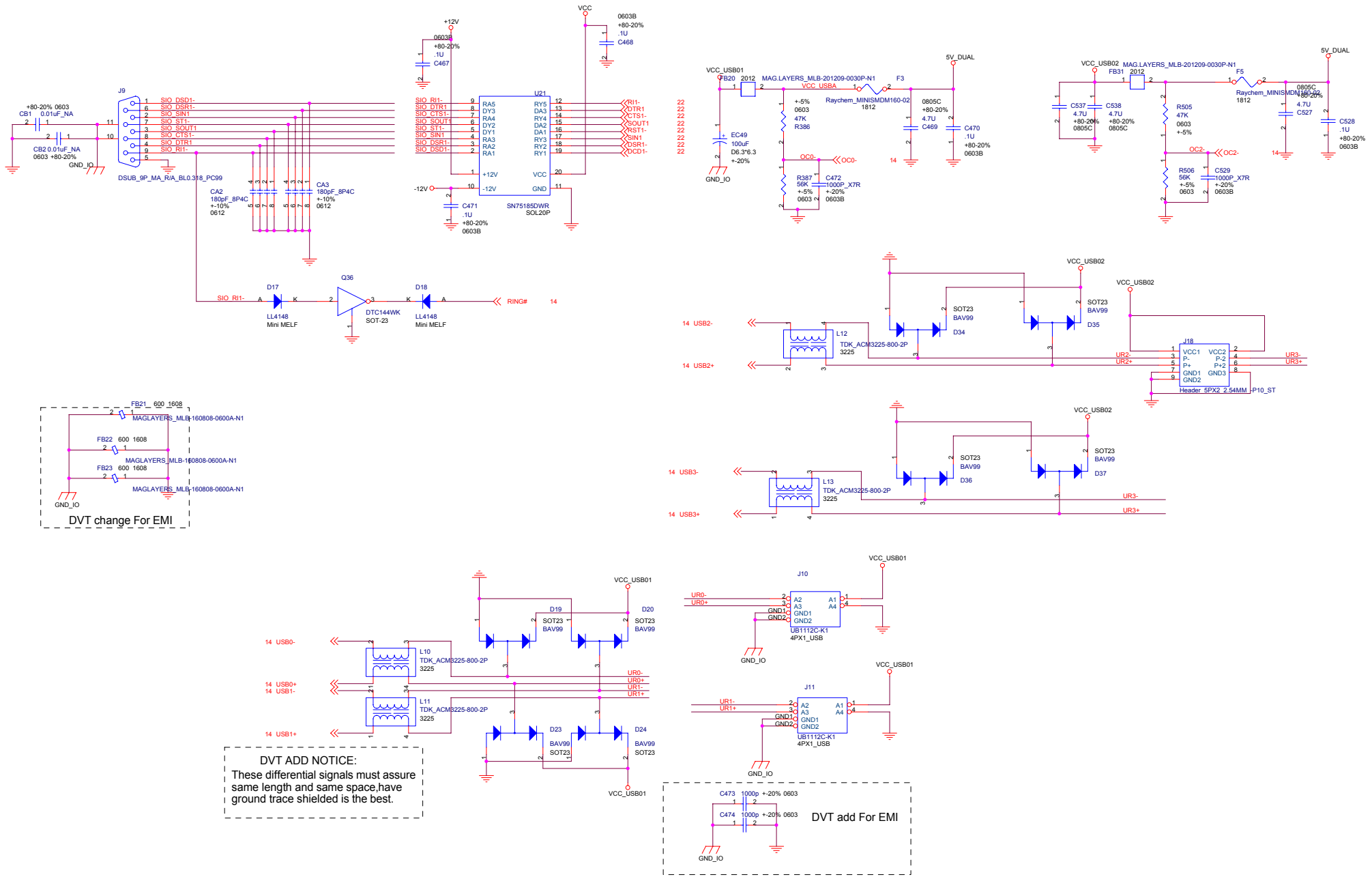

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Title: REAR IO			
Size: C	Document Number: Ampere300		Rev: R0D
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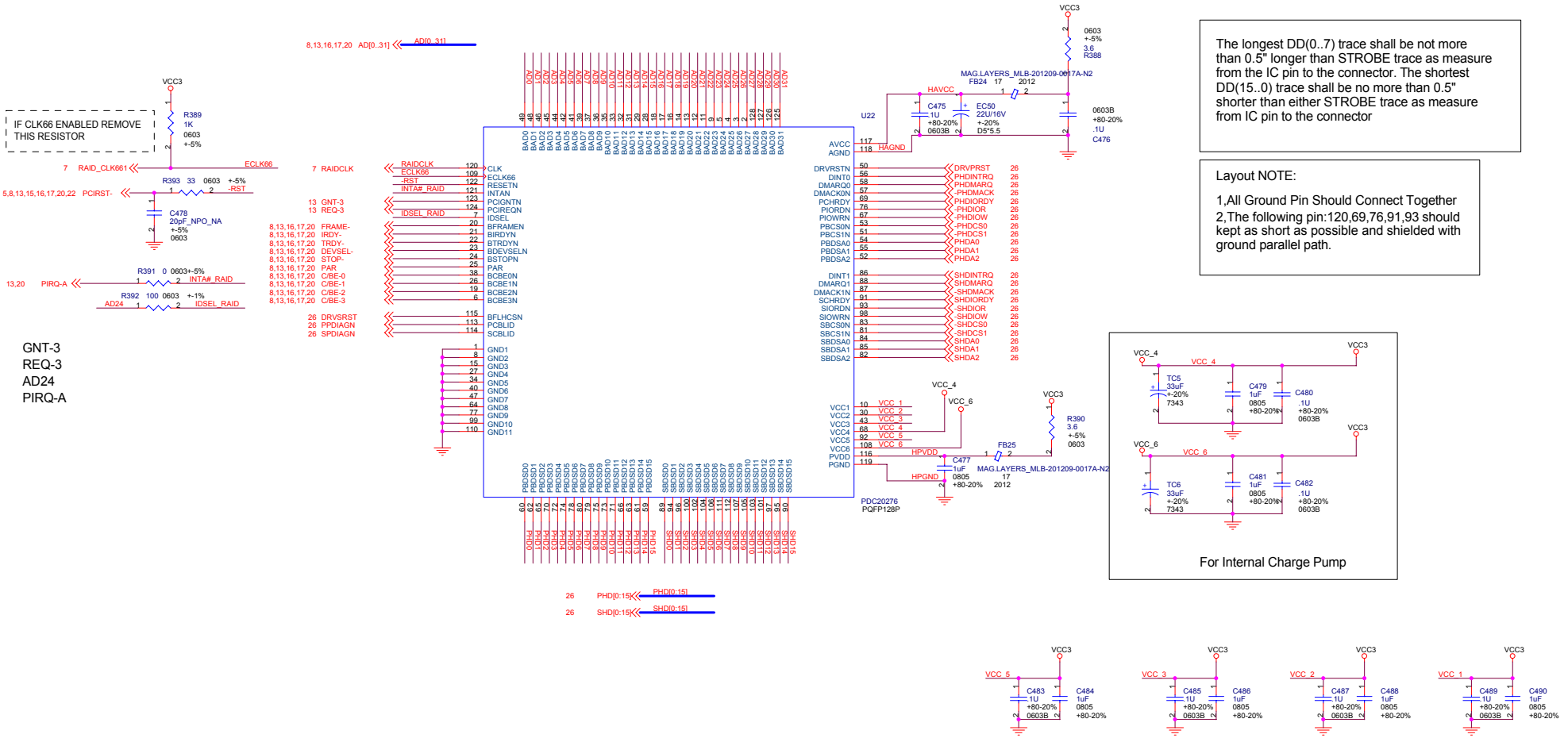

The longest DD(0..7) trace shall be not more than 0.5" longer than STROBE trace as measure from the IC pin to the connector. The shortest DD(15..0) trace shall be no more than 0.5" shorter than either STROBE trace as measure from IC pin to the connector

Layout NOTE:

1,All Ground Pin Should Connect Together

2,The following pin:120,69,76,91,93 should kept as short as possible and shielded with ground parallel path.

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Title	PDC20276	
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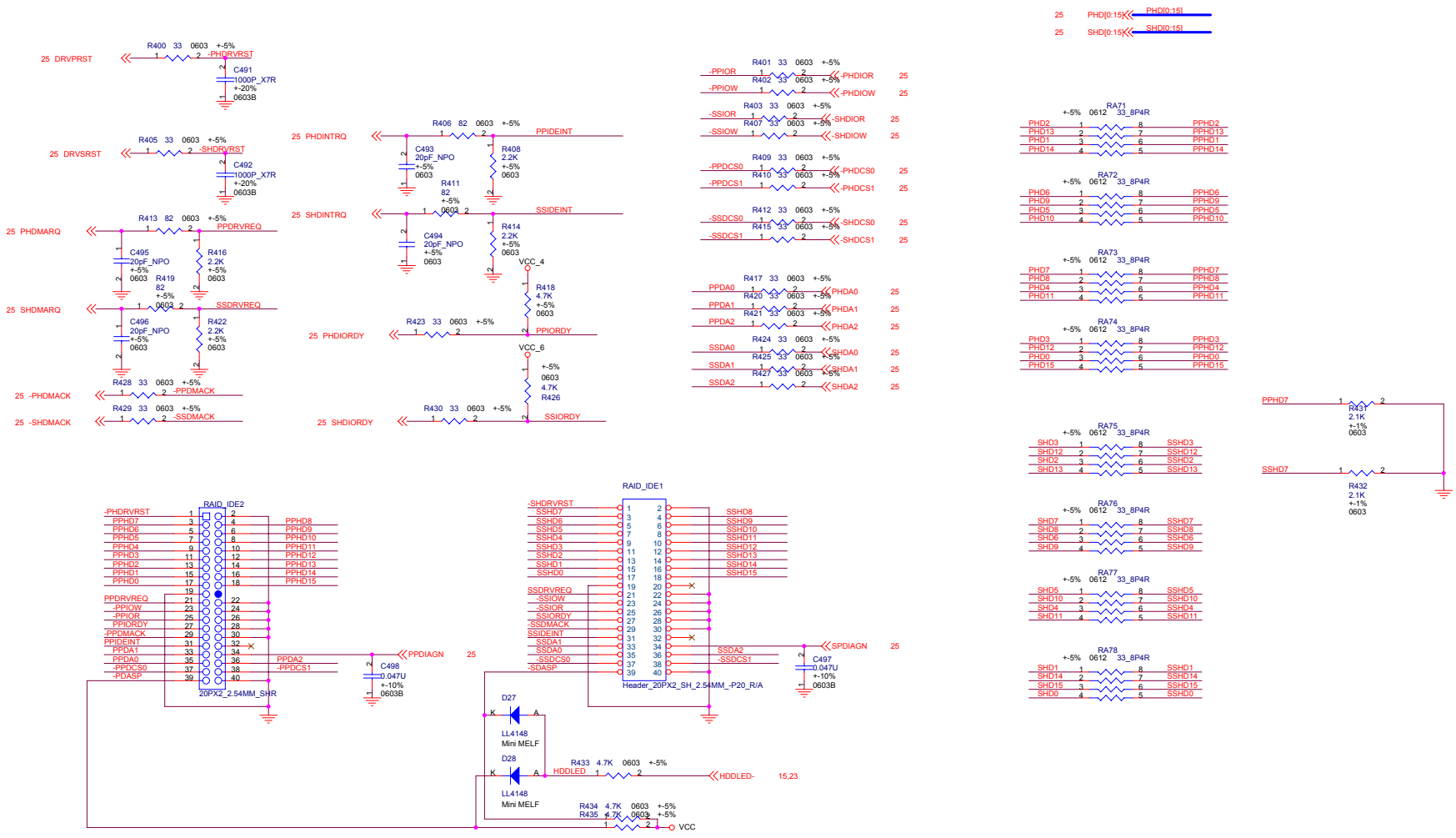

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Title: IDE CONN 3,4

Size	Document Number	Rev
C	Ampere300	R0D

Date: Monday, April 14, 2003

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