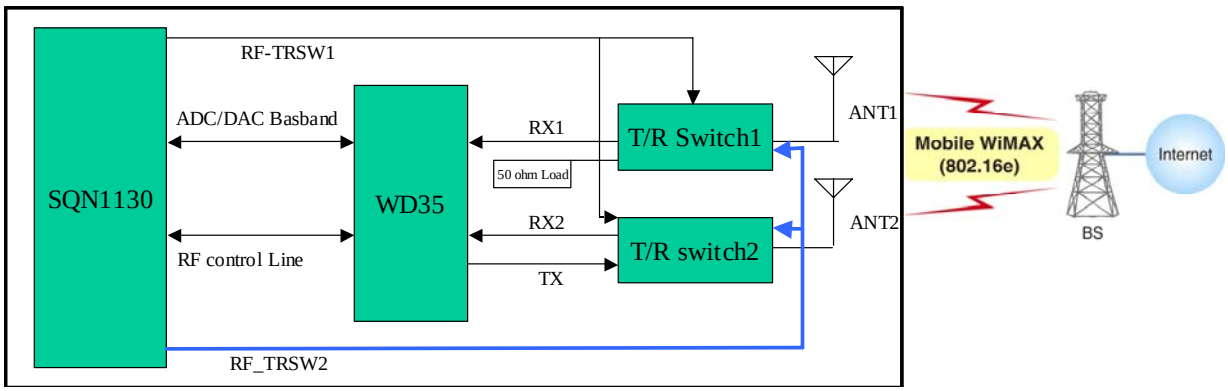
DWM-112 Profile and Block Diagram

The DWM-112 is requirement for **IEEE 802.16e WiMAX USB Adapter**. This Card is based on Sequans /Maxim chipset that complied with IEEE 802.16e standard at 2.5GHz band.



The WiMAX communicate with DWM-112

➢ IEEE 802.16e Section

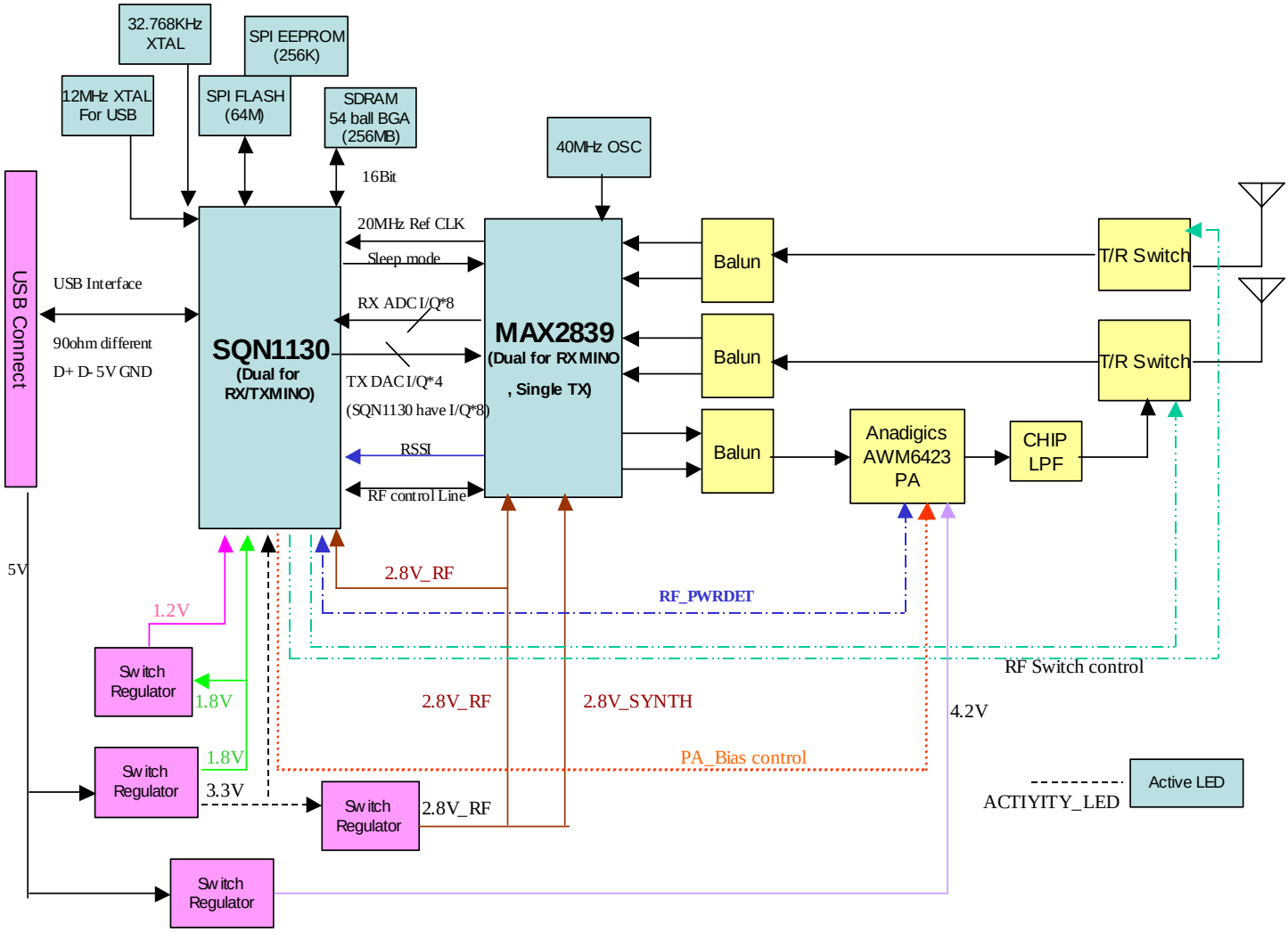
Feature	Detailed Description
Standard	• IEEE 802.16e
Radio and Modulation Schemes	• QPSK -1/2, QPSK -3/4, • 16QAM-1/2, 16QAM-3/4 • 64QAM-1/2, 64QAM-2/3, 64QAM-3/4, 64QAM-5/6 • OFDMA
Operating Frequency	• 2.496GHz to 2.69GHz for licensed band
Channel Numbers	• Depends on the limitation of country regulatory
Duplex Modes	• TDD
Channel Bandwidth	• For profile 3A, support 5MHz and 10MHz bandwidth

➢ General Section

Feature	Detailed Description
Interface	• USB2.0
Antenna Type	• Internal PCB antenna • 3.9dbi(Maxim Gain)
Wireless transmission PHY	• 512 FFT OFDMA

	• 1024 FFT OFDMA • Support SIMO
Operating Voltage	• +5VDC
Current Consumption	• Max. Current: 0.5A
LEDs	• Power • Link

➢ Functional Block Diagram



The DWM-112 has two major sections: the digital section, and the analog/RF section. The digital section consists of the SQN1130, SDRAM, Flash, USB port and LED. The analog/RF section use transceiver MAX2839 support for 2.5 GHz channel for IEEE 802.16-2005 (Mobile WiMAX) with 3paths(1T2R). The transmit path consists of a balun filter to matching, an external output power booster (OPB) and the low pass filter. The receiver path consists of a balun. The transmit path and receiver path share the same one

antennae that provide for signal diversity.

Digital Section

This section describes the blocks that make up the digital section in the DWM-112

_ SQN1130
_ SDRAM memory
_ Flash memory
_ LEDs
_ Power supplies

➢ SQN1130

Sequans SQN1130 System-on-Chip (SoC) is a full-featured; single-chip baseband WiMAX controller that performs MAC and PHY functions specified by the IEEE 802.16-2005 (Mobile WiMAX) specification.

- Standard Compliance: IEEE 802.16-2005 Compliant with WiMAX Profile Wave 2

PHY	● S-OFDMA ● 512 or 1024 FFT ● TDD with configurable UL/DL split (up to 75% in DL) ● Configurable RTG and TTG ● Modulation: QPSK, 16-QAM, 64-QAM, plus pilot, preamble and ranging modulations ● 6-bit encoding CQICH ● Coding: repetition, randomization, CC (1/2 to 3/4), CTC (1/2 to 5/6), interleaving ● Cyclic prefix 1/8 ● Frame duration 5 ms ● Channels of 5 and 10 MHz. ● Spectral masks: WiBRO, ETSI, programmable ● Interference rejection: digital filtering ● RSSI and CINR Measurements and Computations ● SIMO: DL STC (Matrix A / B) ● Antenna diversity on DL: STC (Matrix A) ● MAP Support: Normal, Compresed, Sub-DL-UL ● Power control: open-loop, closed-loop ● • H-ARQ UL and DL.

- **The SQN1130 contains the following subsystems:**

- A CPU subsystem, including an ARM926-ES processor, a SIM controller, a SDRAM controller, a SPI controller, a UART, 2 timers, a watchdog, and a DMA controller.
- A HOST interface supporting connection to a host CPU or network via a MII, USB or SDIO interface.

- **WiMAX subsystem comprising**

- PHY hardware, including a double receives channel and double transmission channel for MIMO capabilities
- WiMAX DSP core reserved for internal processing of the WiMAX interface
- WiMAX MAC hardware in transmission and reception for efficient processing of heavy processing functions.
- RFIC Interface composed of 4 RF ADCs and DACs, and 1 Global Purpose ADC/DAC
- Support subsystems such as power and clocks.

SDRAM Memory

The DWM-112 use the SDRAM with 268,435,456 bits synchronous high data rate Dynamic RAM organized as 4 x 4,194,304 words by 16 bits. Synchronous design allows precise cycle control with the use of system clock and I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst lengths and programmable latencies allow the same device to be useful for a variety of high bandwidth and high performance memory system applications.

Flash Memory

The DWM112 implements a 128 Mbit (16M x 8) Serial Flash Memory, with advanced write protection mechanisms, accessed by a high speed SPI-compatible bus. The memory can be programmed 1 to 256 bytes at a time. An enhanced Fast Program/Erase mode is available to speed up operations in factory environment.

LED

The LED is the feedback for power.

Power Supplies

The USB DWM-112 requires an input voltage of 5V form PC or NB. The 5 V input is regulated to the following voltages for the digital section:

_ **3.3 V and 1.8V for SQN1130, Flash and SDRAM -** A RT8020PQW PWM regulator is used for this purpose.

_ **2.8 V for MAX2839 -** A RT9193 low drop out regulator is used for this purpose.

_ **1.2 V for SQN1130 -** A XC60210B122 low drop out regulator is used for this purpose.

RF Front End Section

This section provides information and design guidelines for transmit and receive paths between the antennae and MAX2839. For the DWM-112, a radio transceiver supports three paths for one transmit path and two receiver paths to provide MIMO environment.

➢ MAX2839

The DWM-112 implements the MAX2839 single-chip Direct Conversion RF transceiver IC designed for 2 GHz NLOS wireless broadband MIMO systems. It incorporates one transmitter and two receivers, with 25dB isolation between each receiver. The IC includes all circuitry required to implement the complete RF transceiver function, providing fully integrated receive paths, transmit path, VCO & tank, frequency synthesis, and base band/control interface. It includes a fast-settling Sigma-Delta RF Fractional Synthesizer with ~25Hz frequency step size. The IC also integrates on-chip AM detector for measuring transmitter I/Q imbalance and LO leakage. An internal transmit to receive loop back mode allows for receiver IQ imbalance calibration. The Local Oscillator IQ quadrature phase error can be digitally corrected in ~0.25O steps. The IC supports full duplex mode of operation for either internal or external loop back.

➢ Balun

The output of the 2.5 GHz balun is directed to a semi-lumped low pass filter and multi-layer ceramic band-pass filter combination.

➢ Power Amplifier

The Power Amplifier is a high performance device that delivers exceptional linearity and efficiency at high levels of output power. Designed for portable or mobile applications in the 2.5-2.7 GHz band, it supports the IEEE 802.16e-2005 wireless standard. The DWM-112 support +4.2 V for power amplifier and need low-current bias input. The integrated detector can be used to monitor output power, and the integrated 25 dB step attenuator enables gain

control. No external circuits are required for biasing or RF impedance matching.

- **Antenna Switch**

This antenna switch can provide DWM-112 transmit/receive switch, antenna diversity switch, or band-selection switch.

- **40 MHz Oscillator**

The 40 MHz oscillator provides the core clock for the MAX2839. This oscillator is attached to the MAX2839. The MAX2839 then provides 20 MHz clock to SQN1130.

- **RF Section Voltage Regulators**

Three voltage regulators provide 4.2 V and 2.8 V to the RF front end. The output power booster uses the 4.2 V by using XC6010B422 for the purpose. And the 2.8V is used for MAX2839 to drive it.