

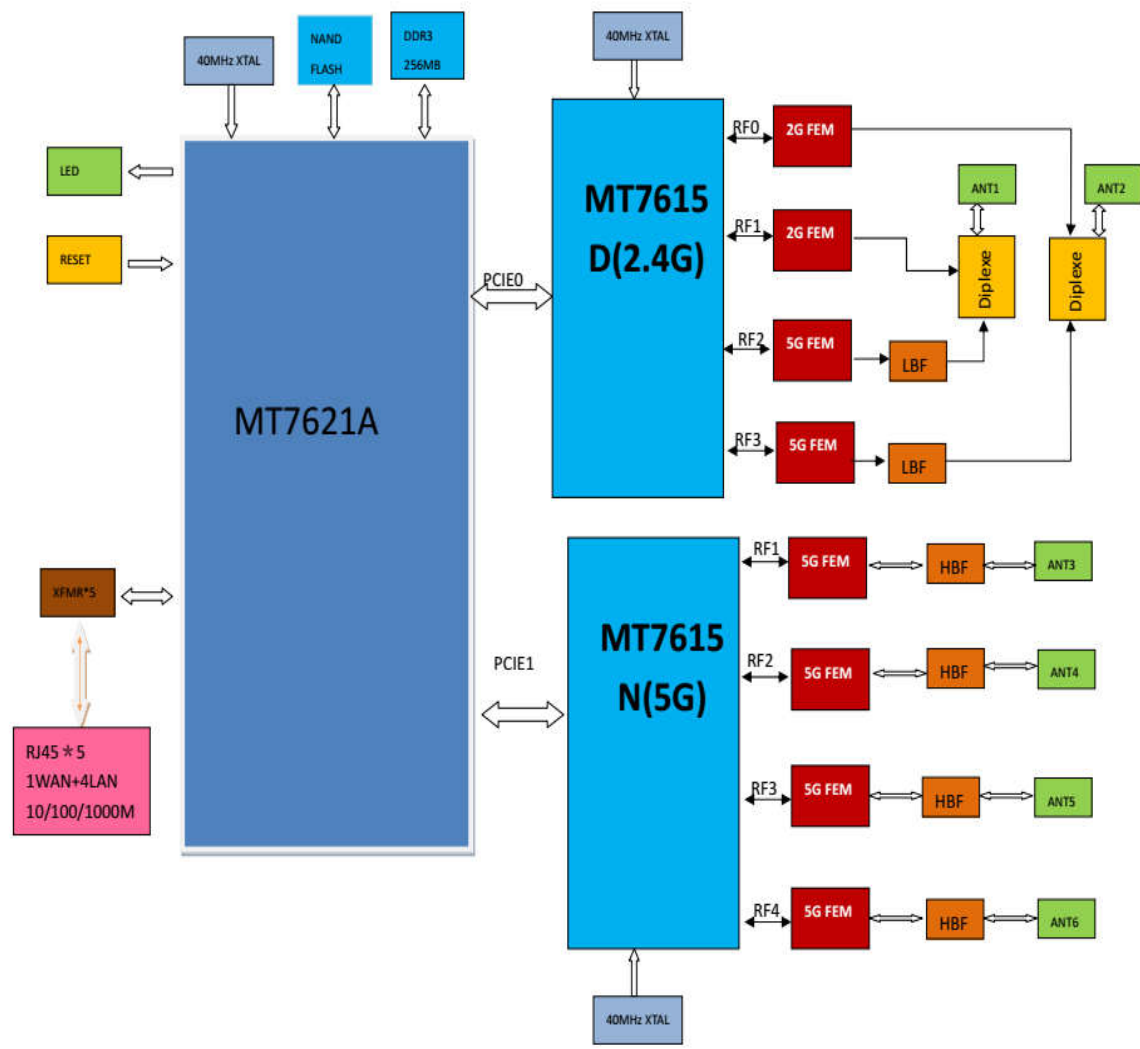


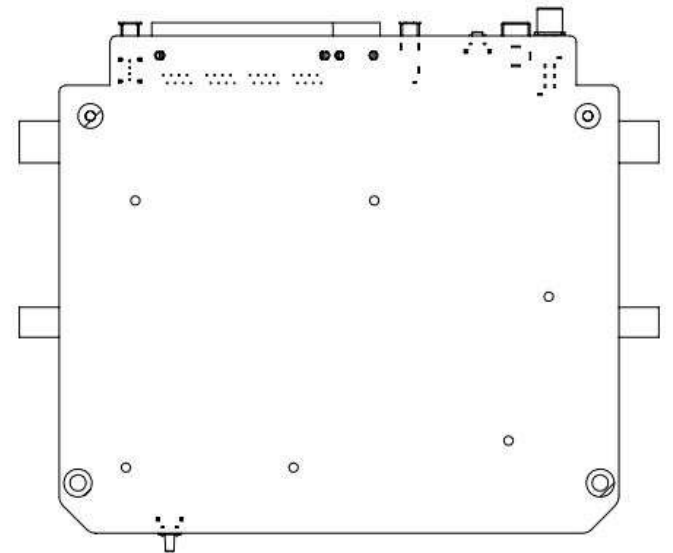
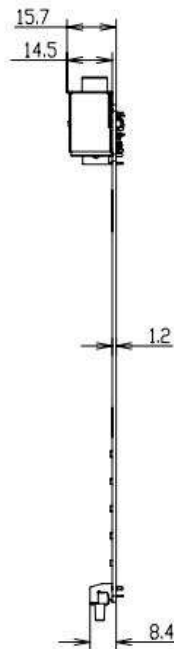
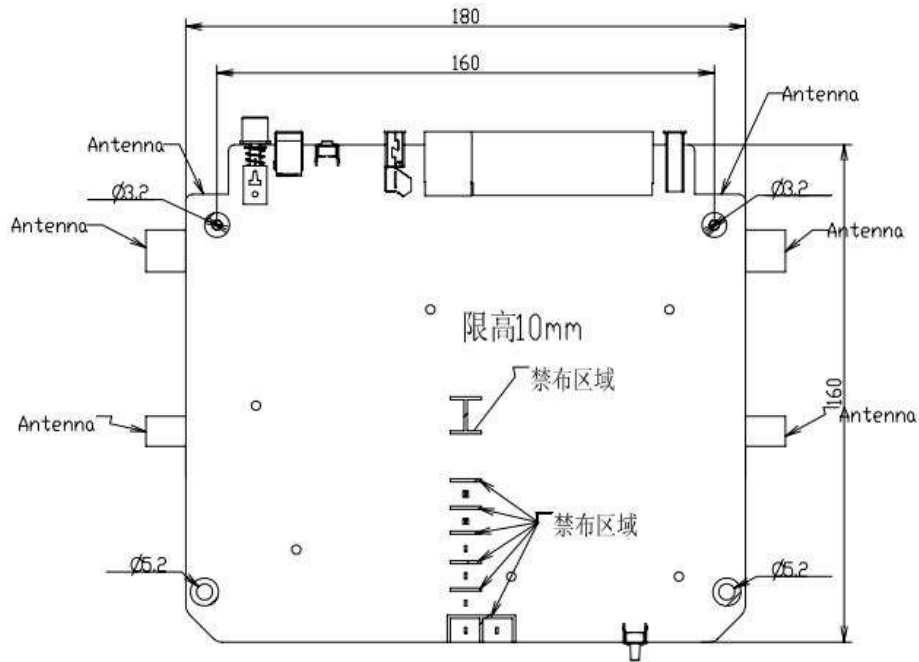
Module Number	DIR-3060
Product Type	4 LAN+1 WAN+2.4G 2T2R+5G Low Band 2T2R+5G High Band 4T4R +WPS+RESET+POWER

Revision History

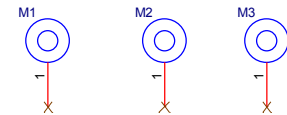
Version	Description	Designer	Date
0.1	Initial release	liuying	2017/03/09

	DIR-3060			
	Cover			
Size B	Document Number	Design By: Liuying	Review By:	Rev 0.1
Date:	Sheet 1 of 23			

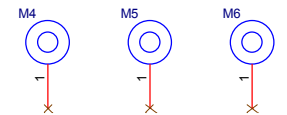




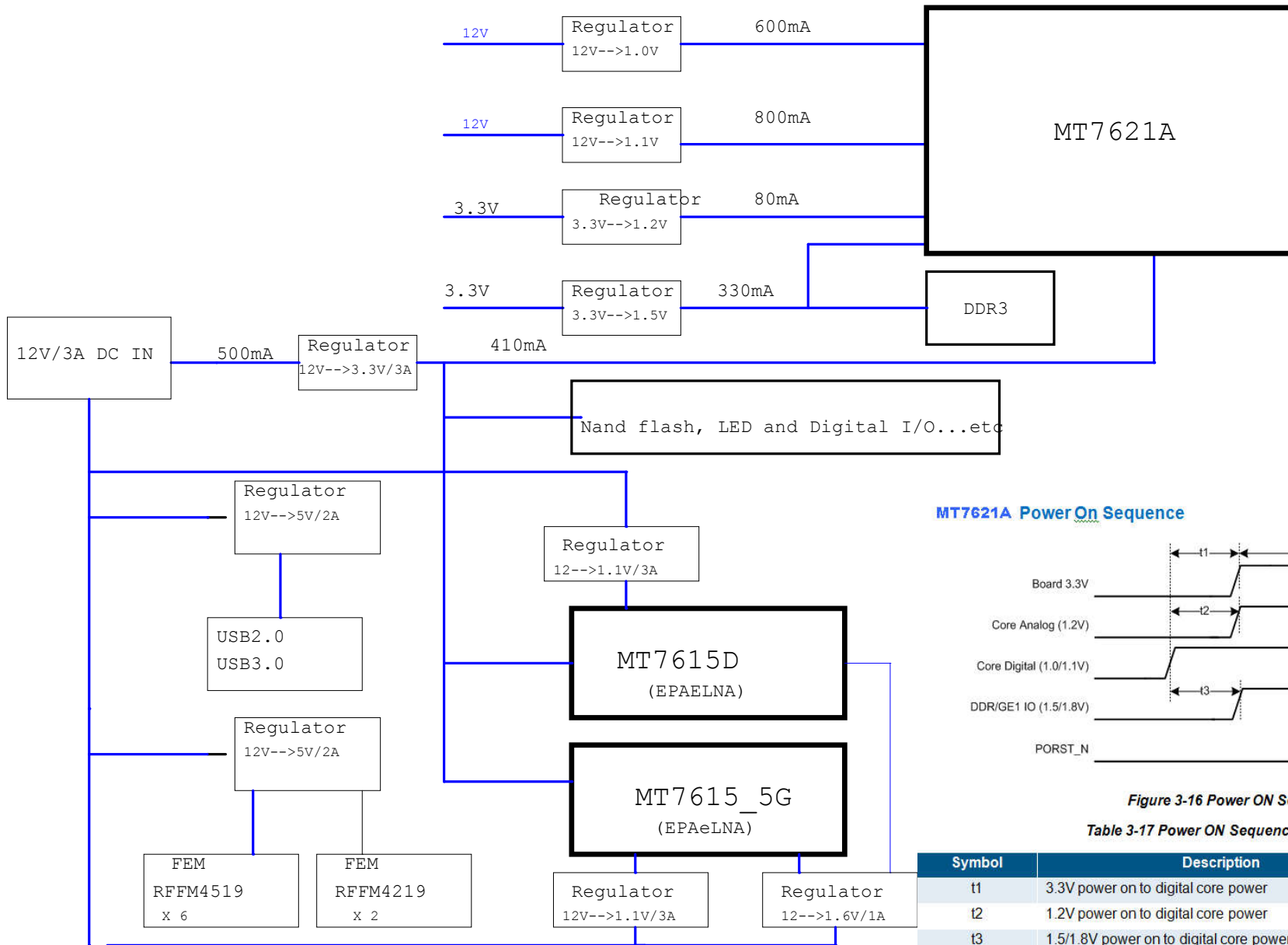
FILDMARK/fildmc\_40/C40S120  
 FILDMARK/fildmc\_40/C40S120



FILDMARK/fildmc\_40/C40S120  
 FILDMARK/fildmc\_40/C40S120



<b>T&amp;W</b> ELECTRONICS		DIR-3060		
		DXF		
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Date:	JAN. 28, 2013	Sheet	3	of 23



**MT7621A Power On Sequence**

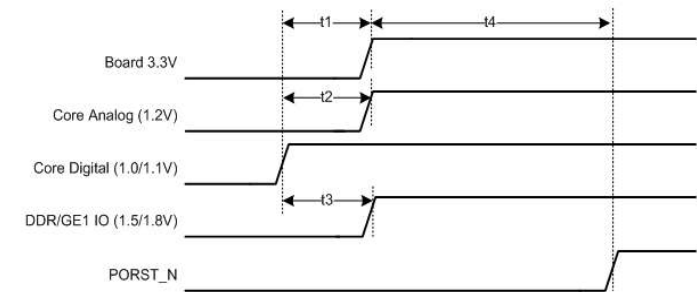


Figure 3-16 Power ON Sequence

Table 3-17 Power ON Sequence Diagram Key

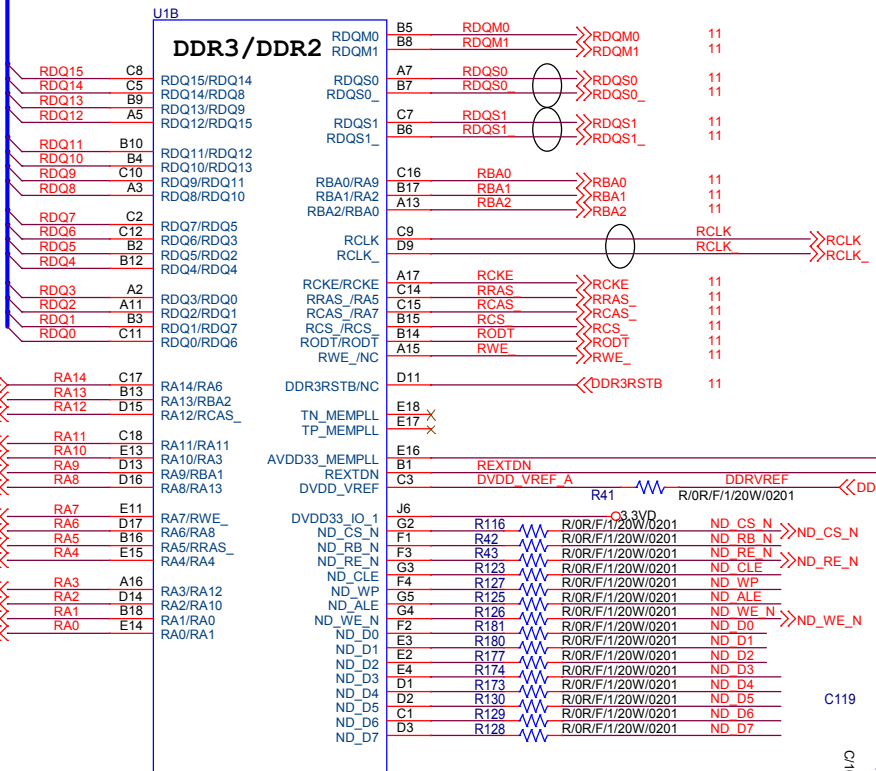
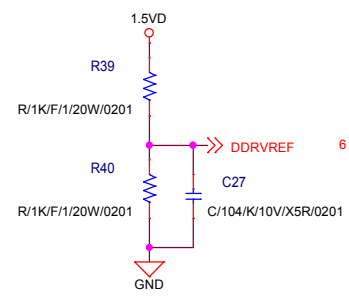
Symbol	Description	Min	Max	Unit
t1	3.3V power on to digital core power	1	-	ms
t2	1.2V power on to digital core power	1	-	ms
t3	1.5/1.8V power on to digital core power	1	-	ms
t4	3.3V power on to PORST_N de-assertion	100	-	ms



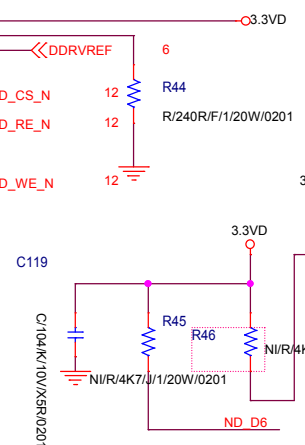
11 RDQ[0:15]

DDR3/DDR2 Interface  
The pinout is different when use DDR3 and DDR2

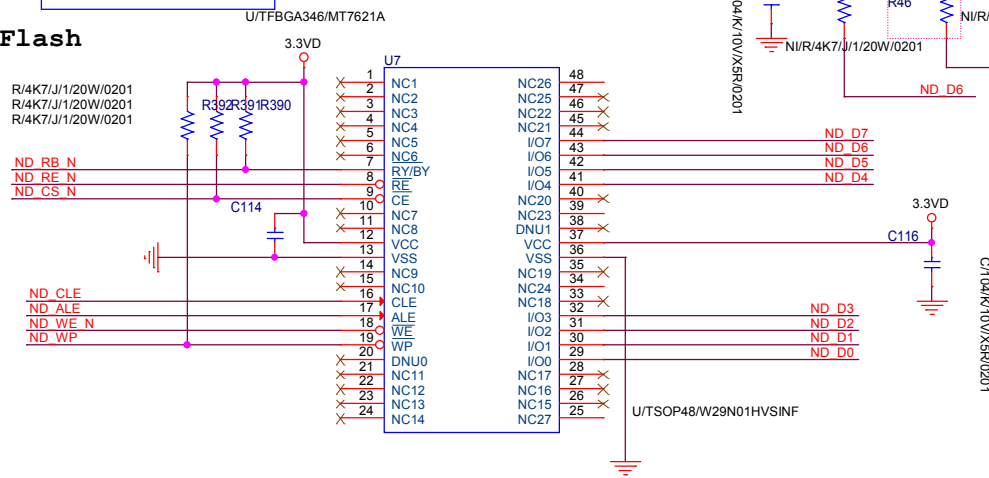
diff pair



spi_cs0 (I/O)	nd_cs_n (O)
spi_cs1 (I/O)	nd_we_n (O)
spi_clk (I/O)	nd_re_n (O)
spi_miso (I/O)	nd_d[4] (I/O)
spi_mosi (I/O)	nd_d[5] (I/O)
spi_wp (I/O)	nd_d[6] (I/O)
spi_hold (I/O)	nd_d[7] (I/O)



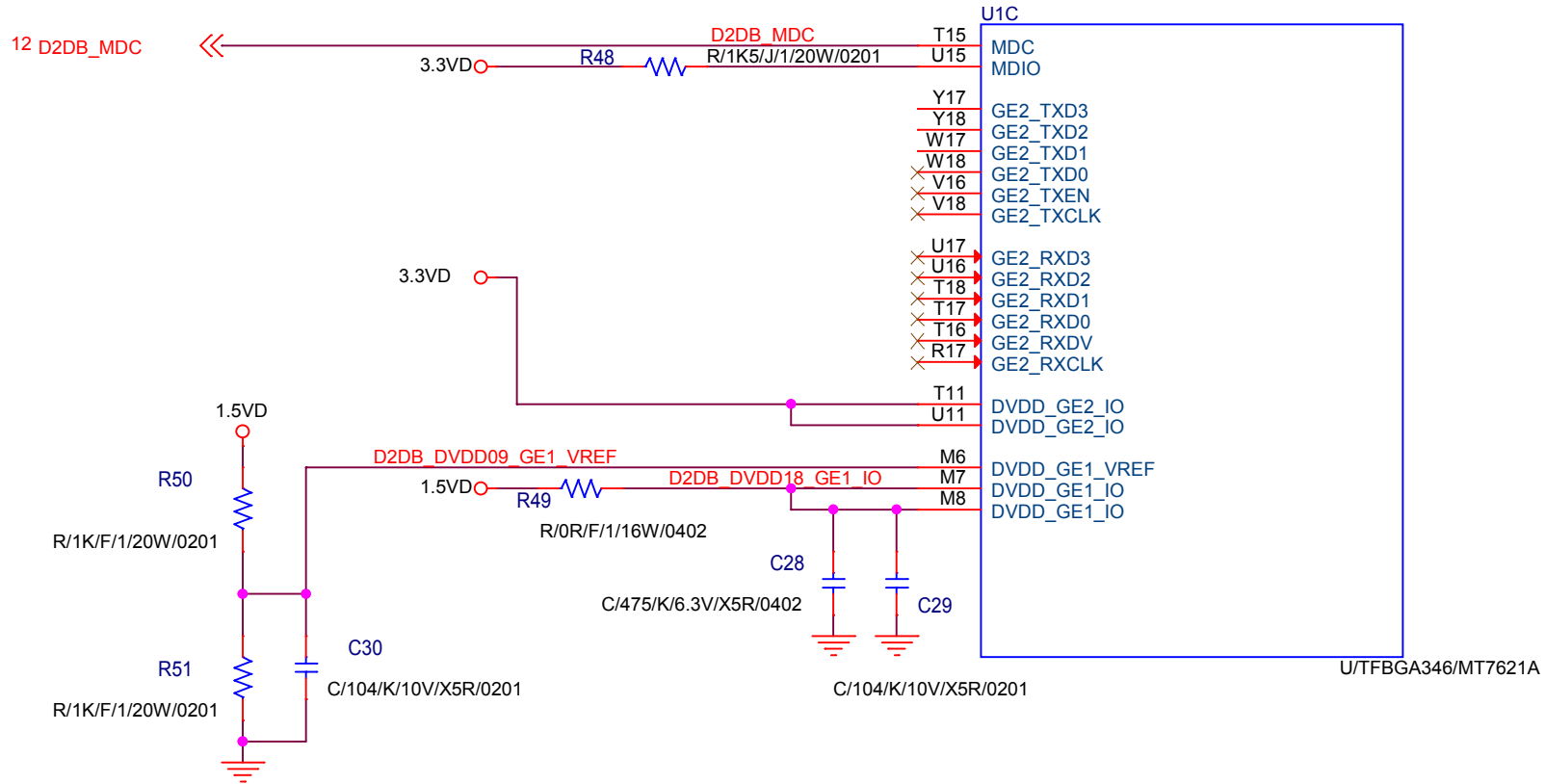
Nand Flash/ SD-XC/SPI Flash



SPI Flash

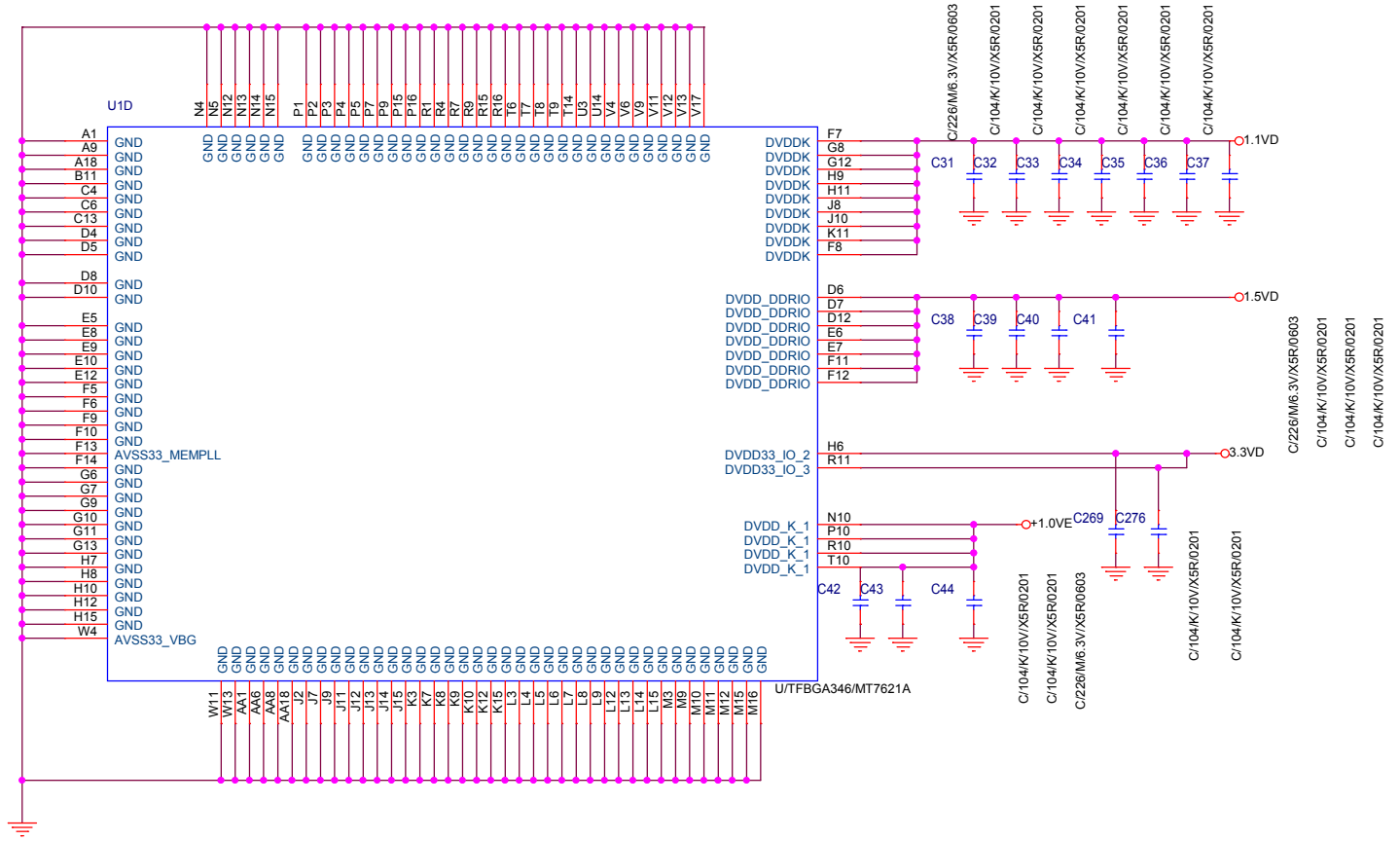
<b>T&amp;W</b> ELECTRONICS		DIR-3060	
		MT7621A_DDR3/FLASH	
Size B	Document Number	Design By: liuying	Review By:
Date:		Sheet	6 of 23

# RGMII Interface



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		MT7621A_RGMII		
Size <b>A</b>	Document Number	Design By: <b>liuying</b>	Review By:	Rev <b>0.1</b>
Date:		Sheet <b>7</b> of <b>23</b>		

### MT7621 Power

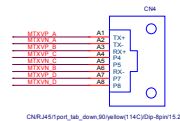
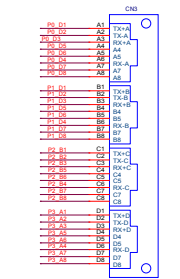
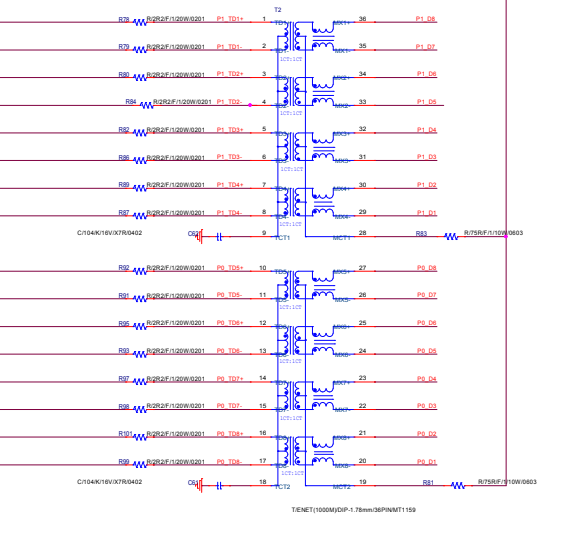
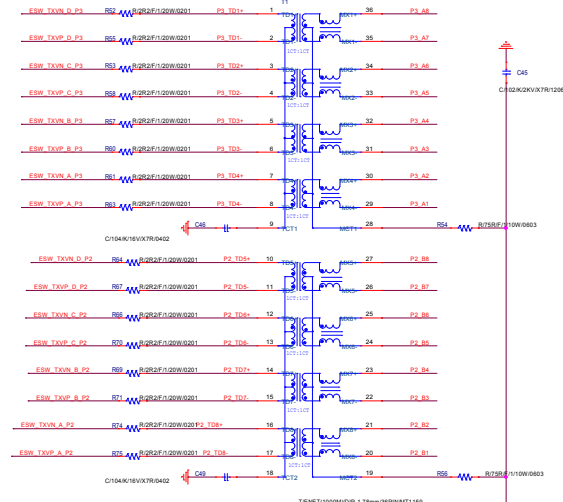
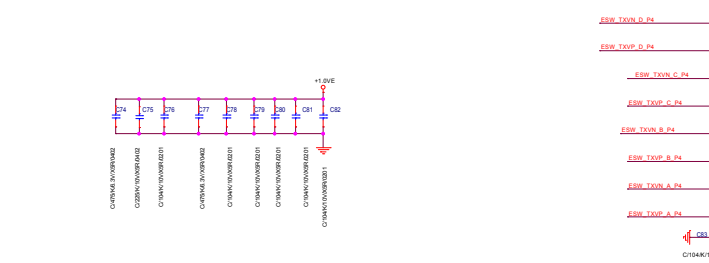
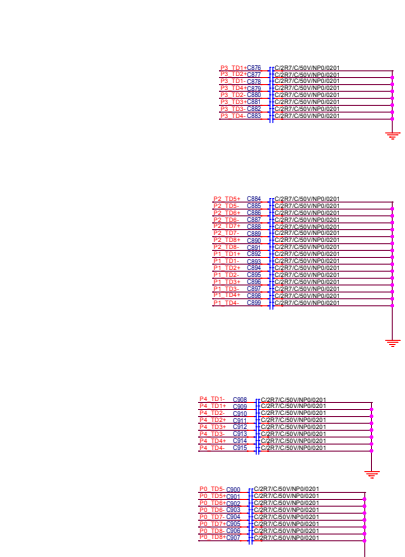
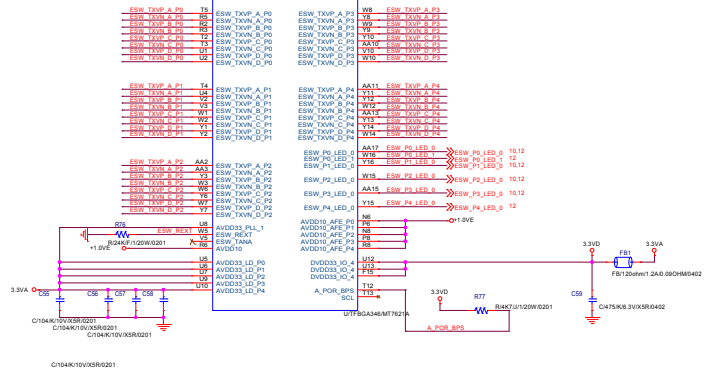


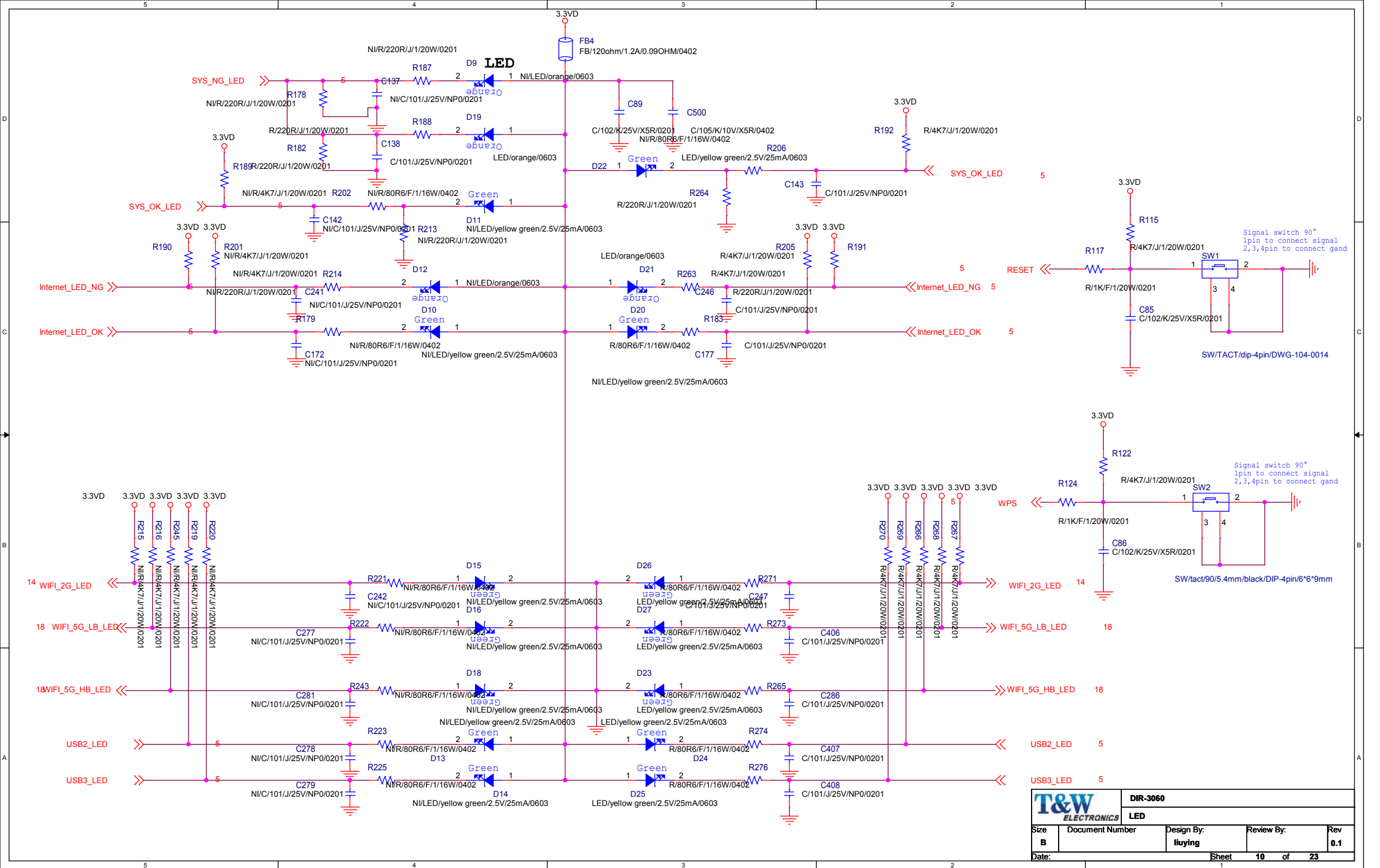
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Size <b>B</b>	Document Number	Design By: liuying	Review By:	Rev <b>0.1</b>
Date:		Sheet 8	of 23	



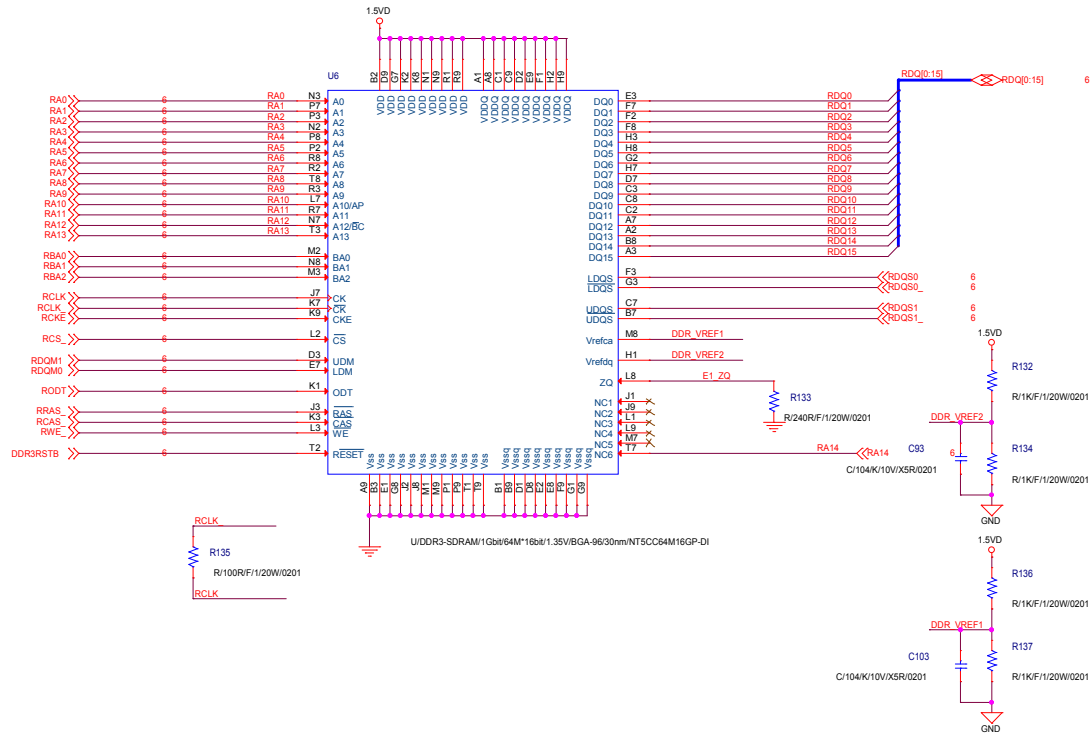
Giga SW

Transformer

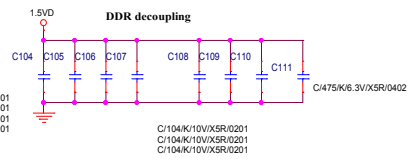
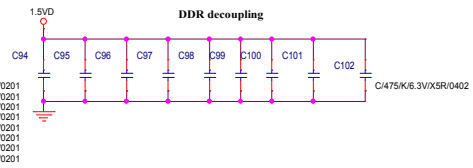
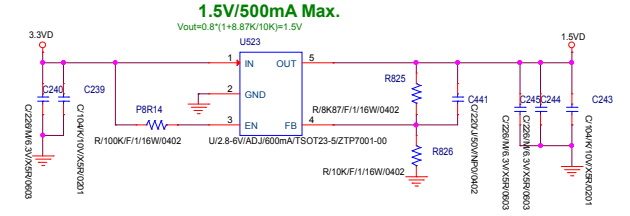




		DIR-3060		
		LED		
Size	Document Number	Design By:	Review By:	Rev
B		liuying		0.1
Date:	Sheet		10	of 23



### 3.3V to 1.5V LDO Converter

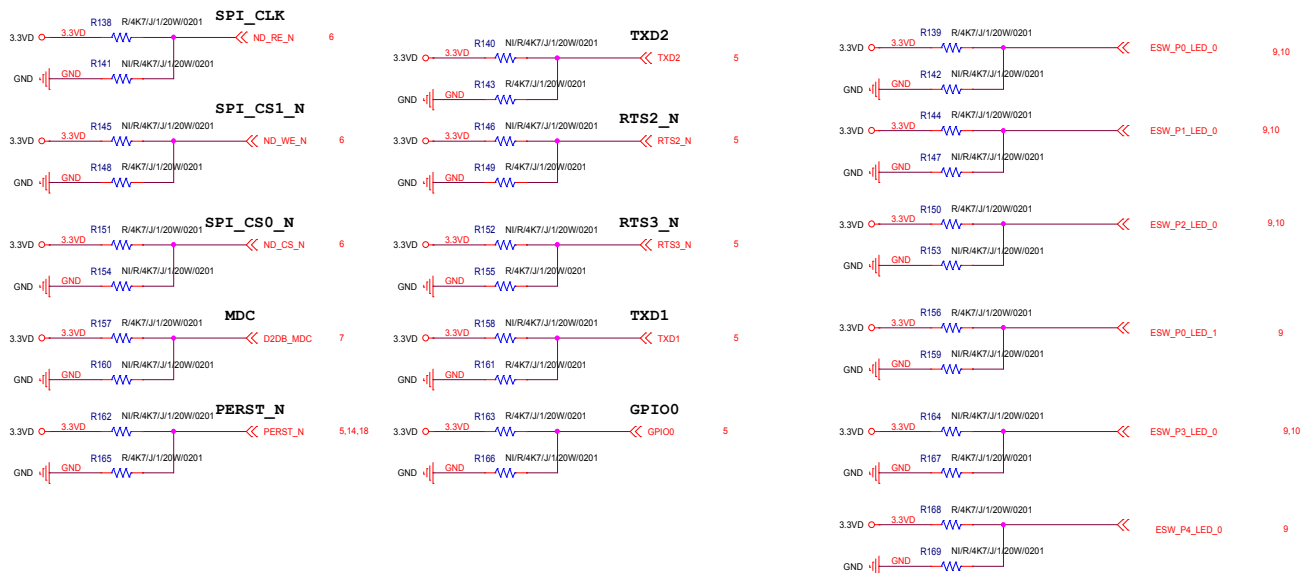


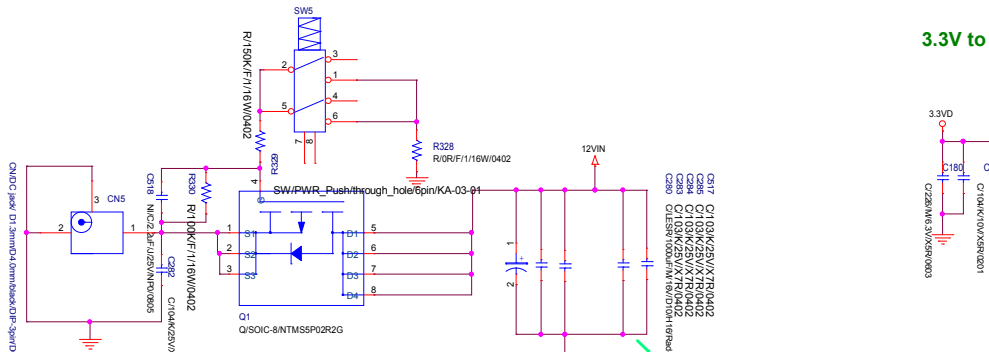
### Boot Strapping

Pin Name	Description	Value
SPI_CLK	DRAM_FROM_EE	For non scan mode: 0: DRAM/PLL configuration from EEPROM 1: DRAM configuration from Auto Detect
{SPI_CS1_N, SPI_CS0_N, MDC }	XTAL_MODE	100: 40 MHz, Single end input 101: 40 MHz, differential input 110: 25 MHz, Self Oscillation mode 111: 25 MHz, Single end input
PERST_N	OCP_RATIO	0: 1:3 1: 1:4
TXD2	DRAM_TYPE	0: DDR3 1: DDR2
{RTS2_N, RTS3_N, TXD1, GPIO0}	CHIP_MODE[3:0]	0000: Normal / Boot from SPI 4-byte address and XTAL clock 0001: Normal / Boot from ROM (NAND page 2k+64 bytes) 0010: Normal / Boot from SPI 3-byte address 0011: Normal / Boot from SPI 4-byte address 0100: iNIC RGMI / Boot from ROM 0101: iNIC MII / Boot from ROM 0110: iNIC RVMI / Boot from ROM 0111: iNIC PHY / Boot from ROM 1000: iNIC RGMII / Boot from ROM and XTAL clock 1001: Normal / Boot from internal SRAM 1010: Normal / Boot from ROM (NAND page 2k+128 bytes) 1011: Normal / Boot from ROM (NAND page 4k+128 bytes) 1100: Normal / Boot from ROM (NAND page 4k+224 bytes) 1101: Debug mode 1110: Scan mode 1111: Final Test

### Giga Switch Hardware Trap

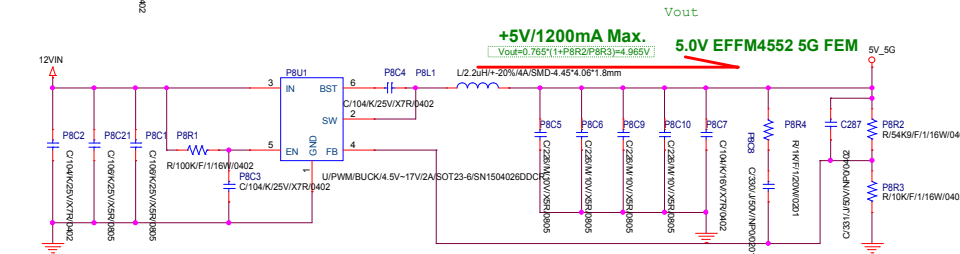
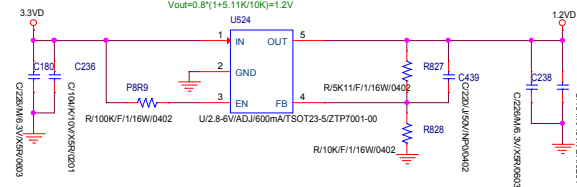
Pin Name	Trap	Fuction	Description	Default
P0_LED_0	HWTRAP[0]	HT_CHIP_MODE[0]	chip_mode[3:0] 4'b0000: IDDO mode 4'b0001: IOTEST mode 4'b0010: NANDTREE mode 4'b0011: RING mode (both IO and std-cell) 4'b0100: MBIST 4'b0101: SCAN mode (internal) 4'b0110: SCAN-COMP mode (compression) 4'b0111: SCAN-MBIST-OLT mode 4'b1000: AFE-OLT mode 4'b1001: GPHY ATE mode 4'b1010: GPHY ADUMP mode 4'b1011: GPHY ADUMP probe mode 4'b1100: Reserved 4'b1101: Reserved 4'b1110: bootup probe mode 4'b1111: normal mode	4'b1111
P1_LED_0	HWTRAP[1]	HT_CHIP_MODE[1]		
P2_LED_0	HWTRAP[2]	HT_CHIP_MODE[2]		
P0_LED_1	HWTRAP[3]	HT_CHIP_MODE[3]		
P3_LED_0	HWTRAP[9]	HT_XTAL_FSEL[0]	External Crystal Frequency Selection xtal_freq_sel[1:0] 2'b01: 20MHz 2'b10: 40MHz 2'b11: 25MHz	2'b10
P4_LED_0	HWTRAP[10]	HT_XTAL_FSEL[1]		





### 3.3V to 1.2V DC-DC Converter

For USB/PCIe PHY Power (1.2V)  
1.2V/300mA Max.



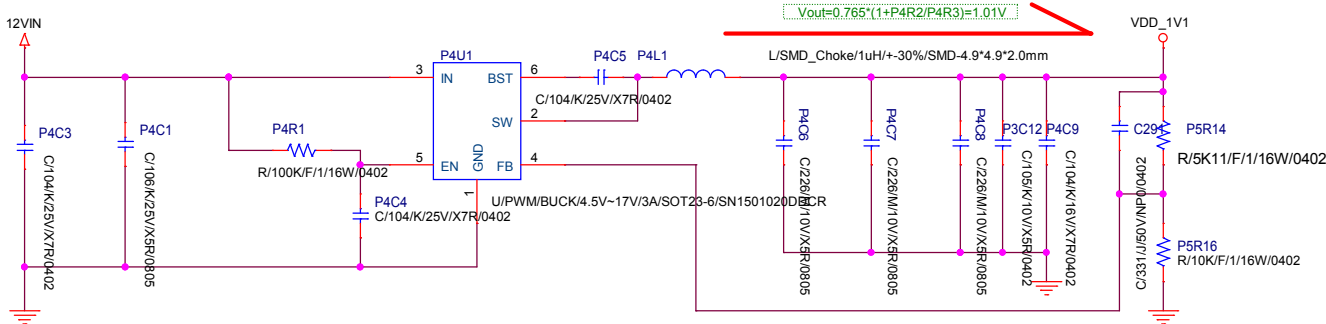




# 12V to 1.1V DC-DC Converter

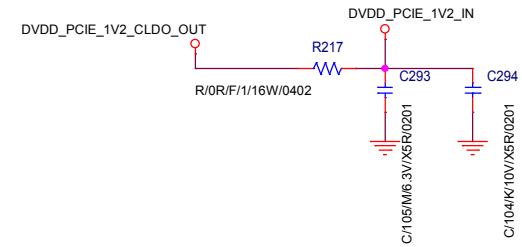
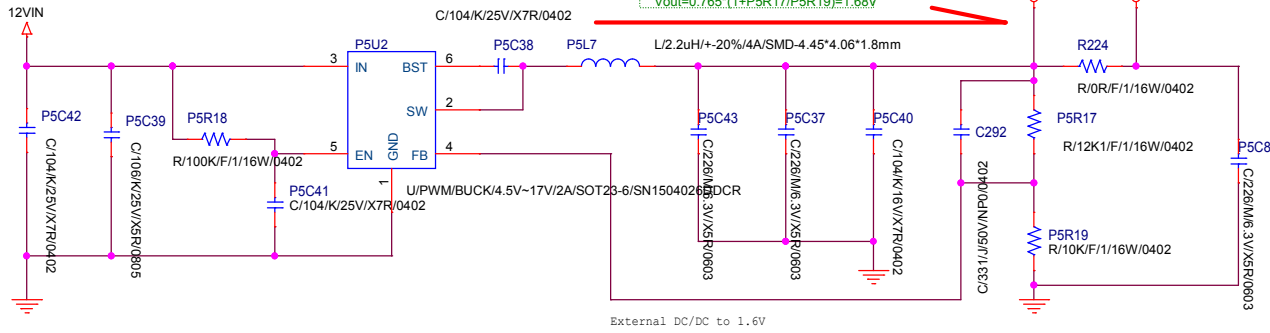
# 1.1V MT7615E Core

1.1V/3000mA Max.



J17 1.15V source from external DC/DC converter  
 J25 1.15V source from power supply  
 (pin 1 need to connect to power supply equipment)

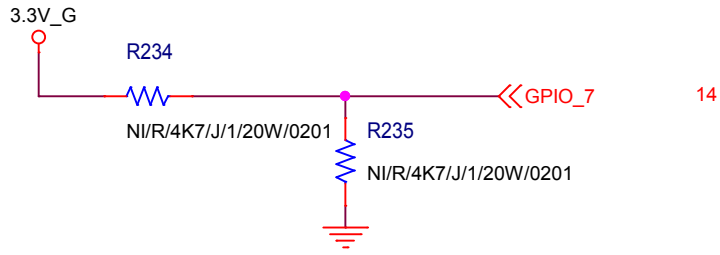
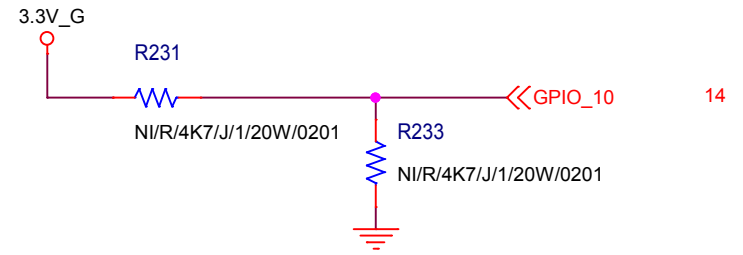
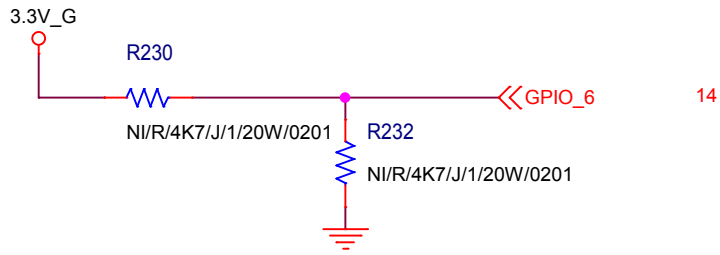
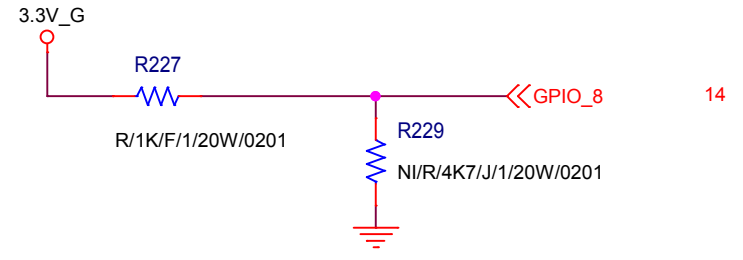
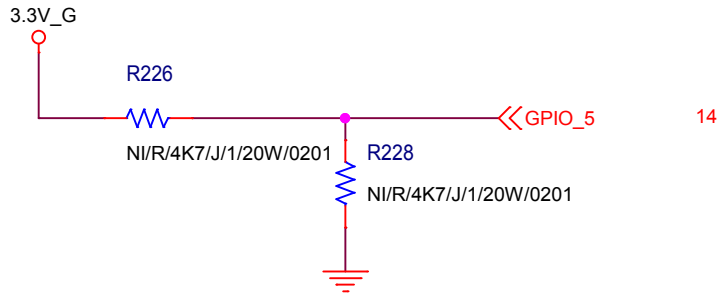
1.68V/1600mA Max.



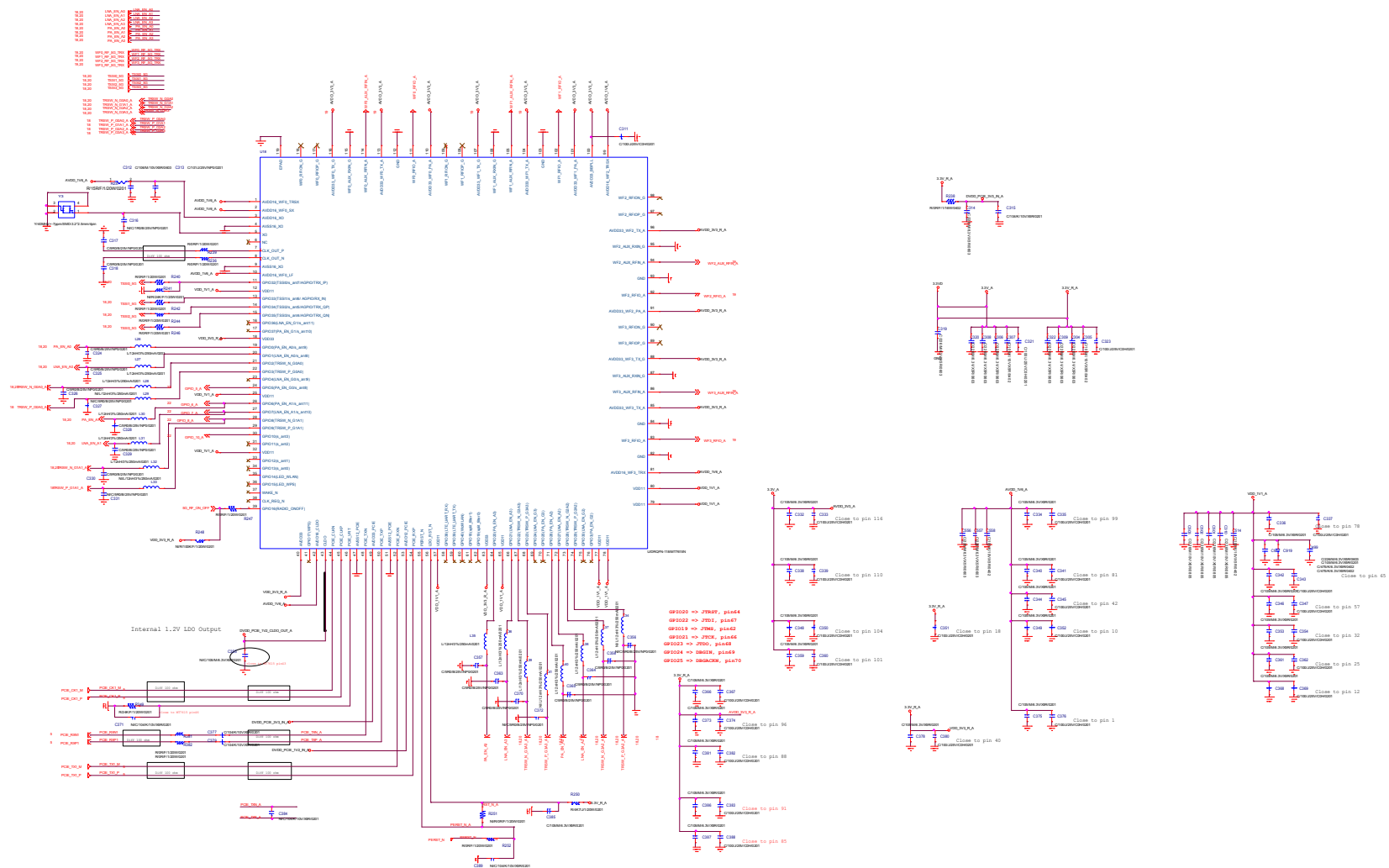
External DC/DC to 1.6V

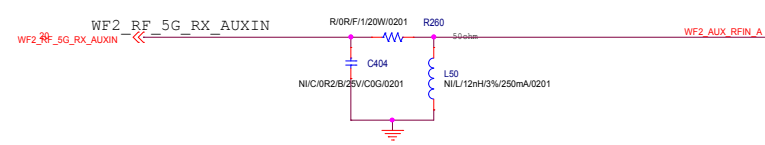
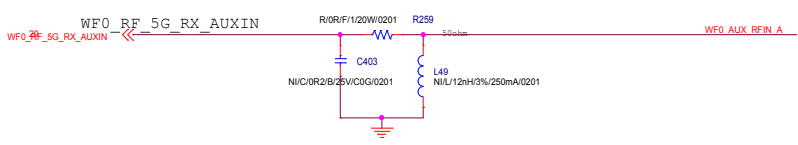
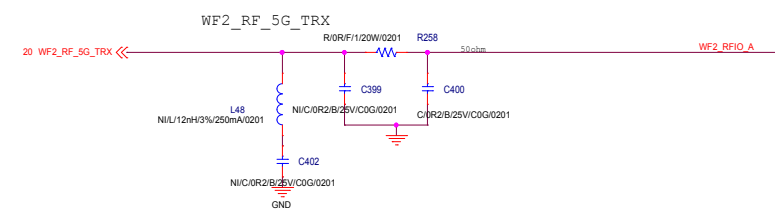
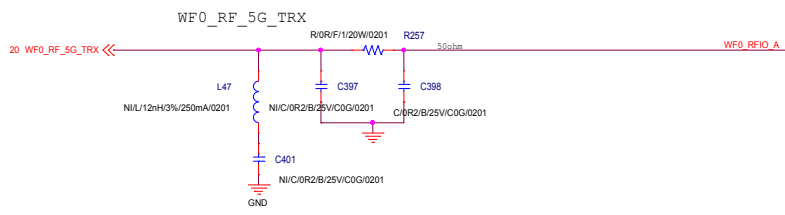
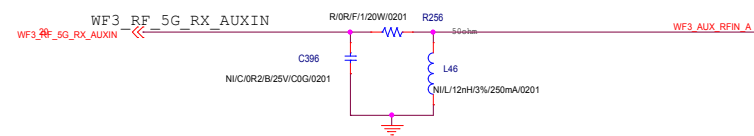
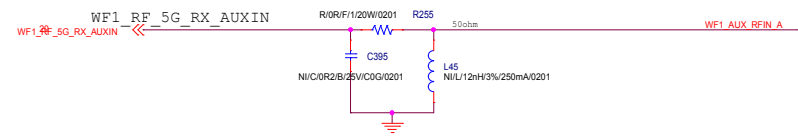
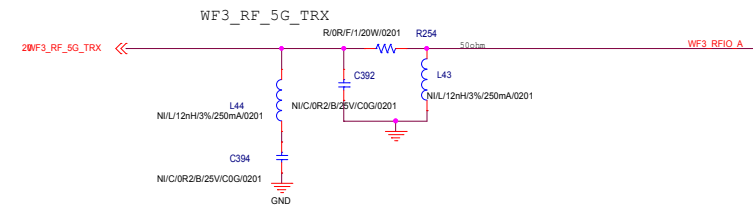
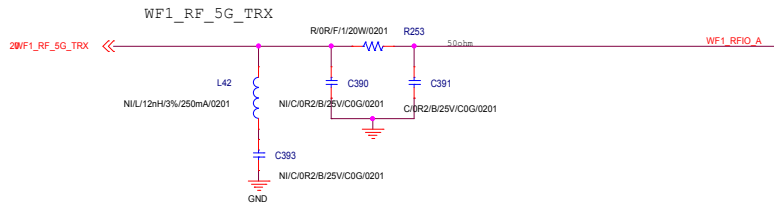
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Date:		Sheet	16	of 23





		DIR-3060		
		2G_Config		
Size A	Document Number	Design By: liuying	Review By:	Rev 0.1
Date:		Sheet 17 of 23		





WF0\_AUX\_RFIN\_A >>> WF0\_AUX\_RFIN\_A 18  
 WF0\_RFIO\_A >>> WF0\_RFIO\_A 18

WF1\_AUX\_RFIN\_A >>> WF1\_AUX\_RFIN\_A 18  
 WF1\_RFIO\_A >>> WF1\_RFIO\_A 18

WF2\_AUX\_RFIN\_A >>> WF2\_AUX\_RFIN\_A 18  
 WF2\_RFIO\_A >>> WF2\_RFIO\_A 18

WF3\_AUX\_RFIN\_A >>> WF3\_AUX\_RFIN\_A 18  
 WF3\_RFIO\_A >>> WF3\_RFIO\_A 18

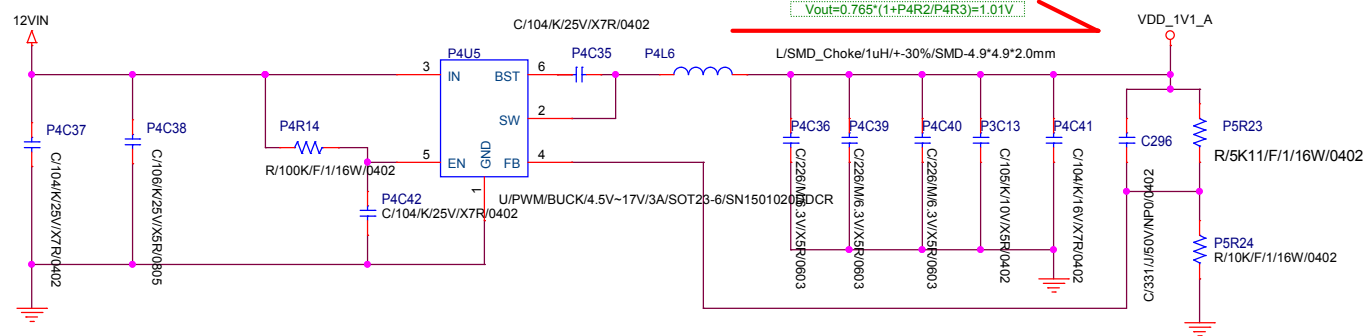


# 12V to 1.1V DC-DC Converter

# 1.1V MT615E Core

1.1V/3000mA Max.

$$V_{out} = 0.765 * (1 + \frac{P4R2}{P4R3}) = 1.01V$$



J17 1.15V source from external DC/DC converter  
 J25 1.15V source from power supply  
 (pin 1 need to connect to power supply equipment)

$$R2 = \frac{R1}{\frac{V_{ref}}{0.6} - 1}$$

The feedback circuit is shown as Figure 2.

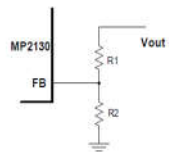
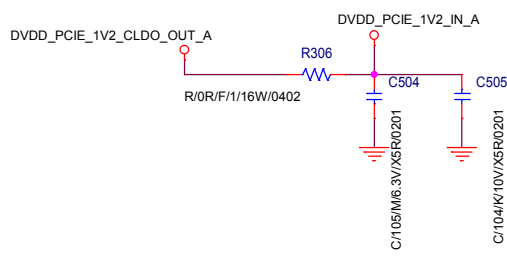
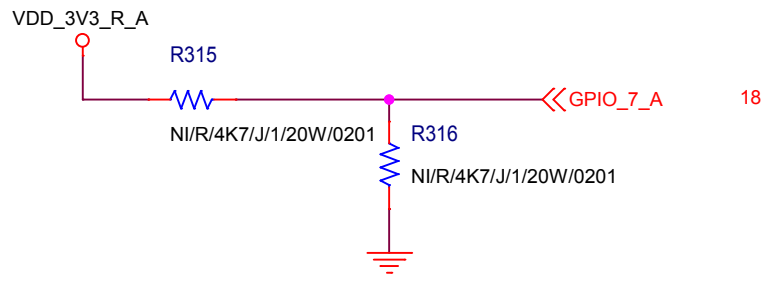
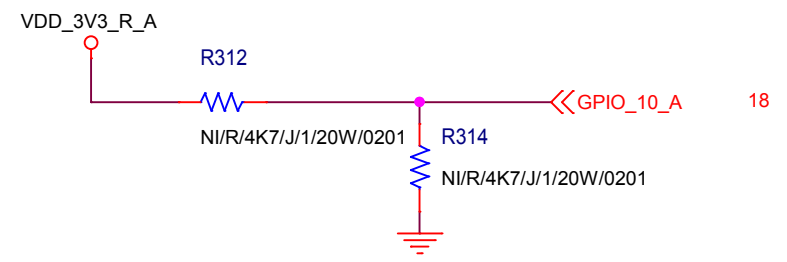
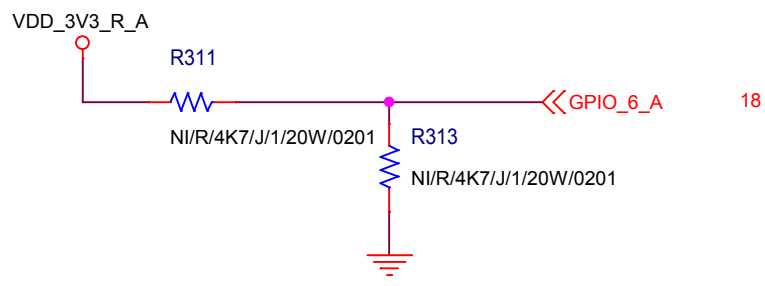
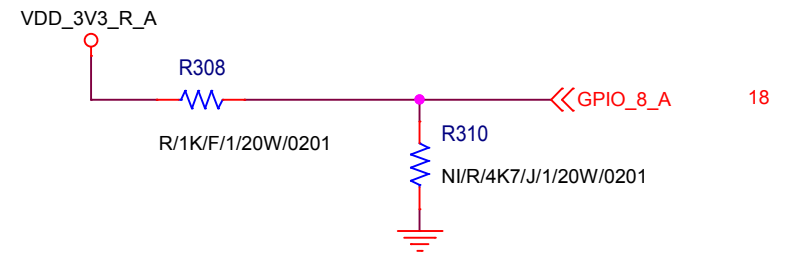
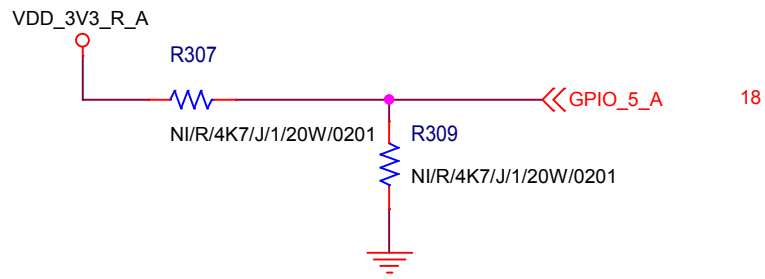


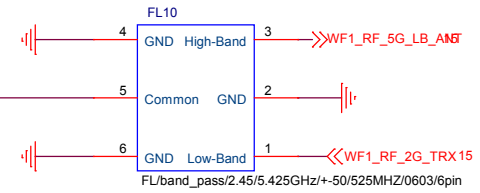
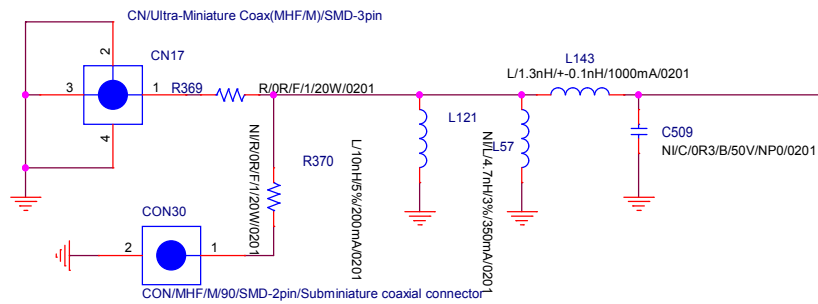
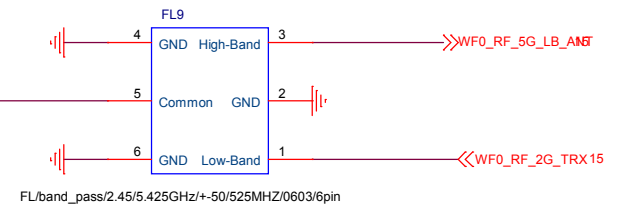
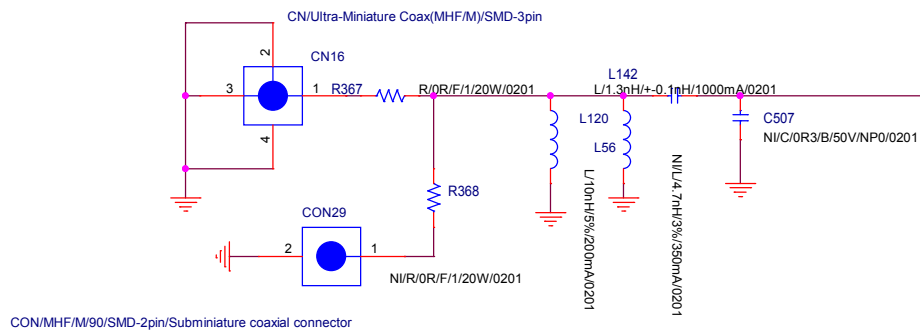
Figure 2— Feedback Network



		DIR-3060		
		Power_5G		
Size B	Document Number	Design By: liuying	Review By:	Rev 0.1
Date:	Sheet			21 of 23



		DIR-3060		
		Config_5G		
Size A	Document Number	Design By: liuying	Review By:	Rev 0.1
Date:		Sheet 22 of 23		



		DIR-3060		
		Diplexer		
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Date:	Sheet 23 of 23			