D-Link Corporation
FCC ID KA2DWLG520MA1
Theory of Operations

The D-Link Corporation **KA2DWLG520MA1** card is based on the Atheros AR2112/AR5513 chipset, which implements IEEE 802.11b, and IEEE 802.11g WLAN solutions. This all-CMOS chipset consists of the following functionality blocks:

- AR2112: Radio-on-a-Chip (RoC): An all-CMOS, single-chip radio transceiver that includes a power amplifier, and integrated dual-conversion filters to convert signals from 2.4GHz to the baseband range. The AR2112 offers fully integrated transmitter, receiver, and frequency synthesizer functions; eliminating the need for external voltage controlled oscillators (VCOs) and surface acoustic wave (SAW) filters.

  There are two AR2112 chips on each **KA2DWLG520MA1** card. These chips are used in two separate radio transceivers, which have outputs that are combined in the far field using phased array antennas. Refer to Theory of Operations Addendum 1 and 2 for additional details on the phased array operation.

- AR5513: An all-CMOS multi-protocol MAC/Baseband processor with interfaces for Flash, SDRAM, PCI, UART, GPIO's, and LED control.

KA2DI634MA1 Block Diagram

The block diagram of the **KA2DWLG520MA1** is shown in Figure 1-1.

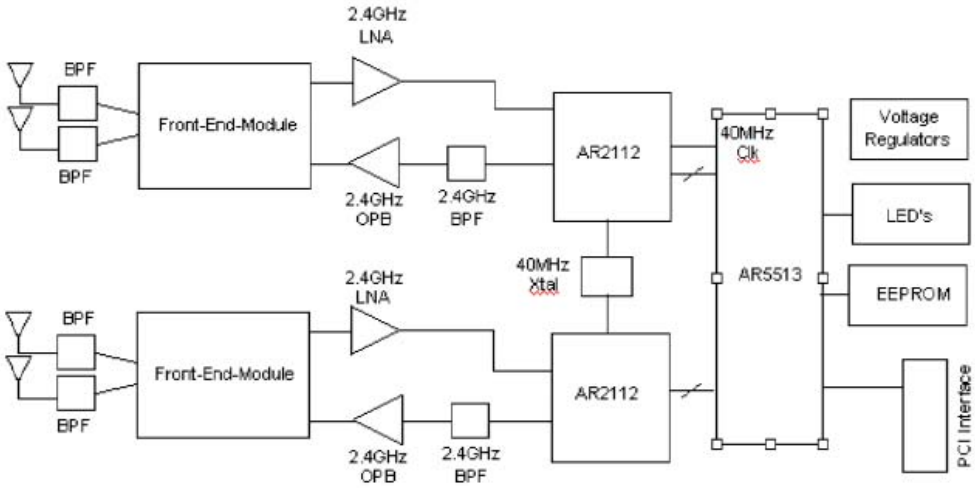

Figure 1-1

The **KA2DWLG520MA1** has three major sections: the digital section, the analog/RF section, and the power supplies.

- The digital section consists of the Atheros AR5513 chip, SDRAM, Flash, and PCI interface.
- The analog/RF section consists of two identical transceivers, each of which includes an Atheros AR2112 chip, external power booster, filters, diplexers, power detectors, external LNA, diversity switch, and antennae.
- The power supplies consist of two low dropout linear regulators.

AR5513

The AR5513 is the source and destination of all signals on the **KA2DWLG520MA1** card. It contains a MAC, 180MHz MIPS R4Kc processor, SDRAM controller and Flash memory interface, PCI interface, UART interface, DACs, ADCs, General Purpose Input/Outputs, LED control outputs, and baseband circuits for transmit beamforming and multiple receive chain combining. Additional information is available on the transmit beamforming function in separate document.

Flash Memory

The **KA2DWLG520MA1** card is populated with a 16M-bit serial Flash device that requires a single 3.3Vdc supply. In addition to storing operating system and application code, the Flash also stores power-on configuration for the processor and the wireless radio. Because of this, an external EEPROM is not required.

PCI Interface

PCI interface of the AR5513 is PCI 2.3 compatible.

Power Supplies

The **KA2DWLG520MA1** card uses three voltage supply rails.

1) 3.3Vdc is supplied directly from the host device. This voltage is used to power the digital circuits of the AR2112 and AR5513 chips and to power the RF front end circuits.
2) 2.5Vdc is derived from the 3.3Vdc supply through a low drop-out linear regulator. This voltage is used to power the core of the AR2112 chips.
3) 1.8Vdc is derived from the 3.3Vdc supply through a low drop-out linear regulator. This voltage is used to power the core of the AR5513 chip.

40MHz Crystal

The 40MHz crystal provides the core clock for the AR2112's and AR5513. This crystal is attached to both AR2112's, which internally form the reference oscillators for their respective synthesizers. The buffered 40MHz output of one of the AR2112's then drives the 40MHz clock input of the AR5513. The maximum frequency tolerance allowed by the IEEE 802.11b/g standard is +/-20ppm.

RF Front-End Overview

The front-end of the **KA2DI634MA1** card employs two identical 2.4GHz transceivers. Each transceiver includes an Atheros AR2112 chip, integrated front-end module, external power amplifier, external LNA, and transmit band-pass filter. The front-end module includes a diversity switch, diplexer, transmit and receive filters, and power detector. Note that the front-end module is a 2.4GHz/5GHz device; however, in this product it will only be used for 2.4GHz operation. The Atheros AR2112 does not operate in the 5GHz frequency band.

The following description applies to both 2.4GHz transceivers:

Tracing the transmit path, the 2.4GHz transmit signal from the AR2112 is first filtered by an LTCC bandpass filter and then boosted with an output booster (OPB). The output of the OPB is directed to an integrated front-end module. This module filters the signal, detects the transmit power level for closed loop power control, and then directs the signal to one of two diversity antennas through a diversity switch.

Tracing the receive path, the 2.4GHz signal is received at the selected antenna and directed by the front-end module's diversity switch. The signal at the output of the switch is then filtered and directed to an external low noise amplifier, which amplifies the signal, before directing it to the AR2112 for additional amplification, filtering, and down-conversion to baseband.

RF Front-End Detail

AR2112
The AR2112 chip is an integrated CMOS radio transceiver that supports the IEEE 802.11b, and IEEE 802.11g standards. The AR2112 supports connection to an external output booster for high performance. The transceiver core, digital logic, and VCO are powered by 2.5V. The tolerances on the 2.5V supply need to be +/-5%. The I/Os are powered by 3.3V.

Matching
2.4GHz Tx output from the AR2112 is matched to external components using lumped-element matching circuits. Since there are sufficient gains in the 2.4GHz Tx front-end, a balun is not needed and a single-ended output is used. The unused output is terminated. On the receive side, a similar single-ended matching configuration is used at the 2.4GHz inputs of the AR2112.

2.4 GHz Tx Band Pass Filter (BPF)
The AR2112 2.4 GHz transmit output is directed to an LTCC band-pass filter. This filter is intended to reduce spurious emissions from the AR2112 before they reach the external 2.4 GHz output booster.

2.4 GHz Power Booster (OPB)
The 2.4 GHz power booster is intended to provide a linear gain boost to the AR2112 transmitter output, thereby improving overall system performance.

2.4 GHz Lowpass Filters (LPF)
The output signal of the 2.4GHz OPB is filtered by a discrete lowpass filter before it enters the front-end module. This filter is a simple 3rd order Butterworth filter designed to suppress all the harmonics of the signal.

Front-End Module (Transmit Chain)
This module filters the input signal from the OPB before directing it to a diplexer. As mentioned previously, the front-end module is capable of 2.4GHz and 5GHz operation; therefore, it contains a diplexer for frequency combining in the transmitter chain. Because the **KA2DI634MA1** only operates in the 2.4GHz band, the diplexer acts as an additional filter for the transmit signal. The output of the diplexer is directed to a power detector. This detector samples the transmit energy, rectifies the signal to produce a dc voltage that is proportional to the transmit power, and then directs this voltage to the AR2112, which then uses the voltage for closed loop output power control. After the power detector, the transmit signal is directed to a DPDT diversity switch that provides both Tx/RX and antenna diversity functions.

Antennae
The diversity switch directs the transmit signal to one of two diversity antennas. One of the antennas is chip antenna with peak antenna gain of 0 dBi, the other antenna is a printed pcb monopole with peak antenna gain of 0 dBi

Front-End Module (Receiver Chain)
The 2.4GHz signal is received at the selected antenna and directed by the front-end module's diversity switch. The switch then directs the receive signal to filters where out-of-band spurious signals are rejected.

External Low Noise Amplifier (XLNA)
The 2.4GHz XLNA is designed to improve the overall system sensitivity by minimizing front end noise figure. The XLNA directs its output to the input of the AR2112 chip, where the signal is further amplified, filtered, and down-converted to baseband for demodulation.