SECTION 6

DETAILED RF TECHNICAL INFORMATION

GENERAL INFORMATION

The GMH series radios are VHF Mobile Transceivers operating in the 136-174 MHz band using frequency modulation. The units are designed for use in the Land Mobile Services, both domestic and foreign. The units are multi-channel digitally synthesized radios using a single crystal for frequency control. Channel frequency information is stored in an EEPROM, with storage capacity of up to 240 receive/transmit frequency pairs.

Controls include an on–off volume control and a rotary channel selector. Software definable momentary contact switches can be used for functions such as repeater talk-around, priority scan and multi-channel scan. Status and channel information is displayed on a vacuum fluorescent display. Connectors are provided on the rear of the unit for an antenna cable, DC power, external speaker and external options/accessories. A microphone connector is provided on the front panel.

An internal adjustment is provided to vary the RF output power between 10 and 50 watts.

A Block Diagram of the Transmitter is shown in figure 1.

SECTION 2.983

In accordance with the Federal Communications Commission's Rules and Regulations, the following data is submitted for Certification. Application is for listing under Parts 22, 74, 80, 90, and 97.

a) BK Radio Inc. is the applicant and the manufacturer of the equipment.

b) Identification: Certification for a Mobile VHF Transceiver is requested under the FCC designator: K95GMH5992X

c) This equipment will be manufactured in quantity.

d) 1) Type of emissions: 16K0F3E, 11K0F3E, 16K0F9W, 11K0F9W

2) Frequency range: 136 – 174 MHz in 1.25 kHz steps

3) Nominal operating power: variable 15 to 50 Watts.

4) Maximum Power: 59 Watts.

5) DC Power input to the Final stage:

		DC Input Current		
Output Power	DC Input Voltage	136 MHz	155 MHz	174 MHz
10 Watts	12.5 V	7 A	5 A	6 A
30 Watts	12.5 V	10 A	8 A	9 A
50 Watts	12.5 V	13.3 A	10 A	12 A

6) The tune-up procedure: Selection of the operating channel is the only adjustment the operator makes to the transmitter. All other transmitter adjustments are inaccessible during normal operation.

7) Transceiver Frequency Generating Circuit: The Transceiver uses a single Stabilized Master Oscillator (SMO) to synthesize the channels between 136 MHz and 174 MHz in 12.5 kHz increments. The same oscillator is offset 16.9 MHz to provide the Local Oscillator signal for Mixer injection in the receive mode. The output signal of the Master Oscillator is divided by a programmable pre–scaler and compared to the reference frequency in the LSI synthesizer. The reference oscillator is a modified Colpitts with a 10.0 MHz crystal in the feedback network.

8) Spurious Suppression: Spurious sidebands are suppressed from the SMO by filtering the control voltage, regulating the supply voltage and by isolation through buffer amplifiers. Components of the reference frequency are removed from the control voltage by a low–pass filter. Harmonic radiation is attenuated by a 9–pole elliptical filter before reaching the antenna port.

A limiter amplifier is used to restrict the peak deviation.

A feedback control circuit is used to maintain the output power to the adjusted level.

9) Digitally Coded Signals: The radio has the capability of using digitally coded signals for the purpose of establishing and maintaining communications. The signals are passed through the low pass audio filter required for F3 emission and the transmitter is adjusted so that the instantaneous deviation does not exceed the maximum value allowed for F3 emission.

THEORY OF OPERATION

INTRODUCTION

This document contains a description of equipment, a theory of operation for the GMH Series radio.

EQUIPMENT DESCRIPTION

The BK Radio GMH Series radio is comprised of the following sub-assemblies:

SYSTEM BOARD

This sub-assembly consist of core microprocessor, synthesizer, regulation and switching circuitry. A casting is used to shield the synthesizer area.

RX/TX BOARD

This sub-assembly consists of the RX/TX antenna switch, the receiver circuitry from the front-end through the discriminator, and the low level transmitter line up.

HIGH LEVEL POWER AMPLIFIER BOARD

This sub-assembly consists of the final two stages of the transmitter power amplifier, harmonic filter, and directional coupler.

OPTIONS BOARD

This sub-assembly consists of receive and transmit audio chains, and interfaces with both the systems board and the control board.

CONTROL BOARD

This sub-assembly consists of a control head microprocessor, switching regulator, display driver, and audio power amplifier. It interfaces with the front panel and accessory connector.

VCO BOARD

The VCO board is a separate assembly that resides in its own shielded enclosure and interconnects with the system board and RX/TX board.

THEORY OF OPERATION

SYSTEMS BOARD

System board functions include:

1. Core Microprocessor
2. Regulation: 5.0, 8.6, 9.6, and 20.0 Volts
3. Synthesizer
4. Squelch Detection
5. CTCSS/CDCSS Decode
6. Power Control

Microprocessor

The core microprocessor (U507) communicates with the control heads microprocessor and controls radio functions such as loading the synthesizer, adjusting the deviation and receiver tuning, and CTCSS/CDCSS detection. An EEPROM is used to store calibration and tuning data unique to each radio. A 32.768 MHz crystal is used as a clock for the core microprocessor.

Various transistors provide level interfaces and current capability.

Regulation: 5.0, 8.6, 9.6 , and 20.0 Volts

U502 and associated circuitry comprise a 9.6 volt low noise feedback regulator for use by noise-sensitive analog circuitry on the systems and RX/TX boards. A low battery indication is derived by sensing the error control voltage of this regulator.

U601 and associated circuitry provide a second level of regulation to supply the VCO and synthesizer with 8.6 volts and 5.0 volts.

U504 is the 5 volt supply for the core of the radio.

The microprocessor drives a FET amplifier (Q503) tied to a voltage doubler. This forms a 20 volt switching regulator which is regulated by error amplifier U502 which controls the gain of the FET.

Synthesizer

Synthesizer IC - U604 forms the main synthesizer IC which contains three programmable CMOS dividers and a sample-and–hold phase detector. The first divider (divided-by-R) divides the reference oscillator down to a frequency which is used as a reference by the sample-and-hold phase detector. The second divider (divide-by-N) divides the output of the Prescaler down to a frequency which is equal to the divided down reference frequency when the loop is locked. The third divider (divide-by-A) controls the modulus control line of the Prescaler. The sample-and-hold phase detector provides a DC voltage that is proportional to the phase error between the divided down reference frequency and the divided down carrier frequency. This voltage is fed through the loop filter to the VCO and adjusts the VCO frequency to maintain phase lock between the divided down frequencies.

Prescaler - The prescaler U602 is the first divider in the feedback path of the synthesizer. It divides the RF signal to a frequency which can be processed by the following CMOS dividers. The prescaler is a dual modulus type which allows the division ratio to be set by the synthesizer to either divide-by-128 (modulus control line high) or divide-by-129 (modulus control line low). This capability allows the channel spacing to be determined by the divided down reference frequency and not a multiple thereof.

Reference Oscillator - The Reference Oscillator provides the frequency reference from which the receiver and transmitter injection signals are synthesized. The oscillator frequency is controlled by the crystal Y601 which operates in the parallel resonant mode. The core microprocessor uses temperature sensor U607 to measure the temperature of the crystal and changes the bias on varactor CR602 accordingly, to compensate the crystal to less than $\pm$2.5 ppm tolerance. The varactor provides a means for modulating the reference oscillator to improve the synthesizer frequency response for low frequency modulation.

Loop Filter - The Loop Filter removes noise and unwanted frequency components from the output of the sample-and-hold phase detector which otherwise would modulate the VCO. In addition, it employs a multiple filter bandwidth design which allows fast response during frequency changes (such as in channel scan) without degrading the noise and spurious performance of the receiver during steady state receive and transmit conditions. The filter bandwidth is switched to a wide condition when the LATCH line pulses high for approximately 6 msec during a frequency change. This allows the new frequency to be reached quickly. When the LATCH line to returns to a low state, the filter bandwidth changes to a narrow condition and provides for good noise and spurious performance. Different filter bandwidths are used for transmit and receive to provide better hum and noise performance in transmit and faster response time in receive. This is accomplished by changing the filter bandwidth to a narrower value when the RX/-TX line goes low during transmit.

Offset D/A – U603 and associated resistors form a serial latching D/A which is loaded by the microprocessor when it loads the synthesizer IC. This provides an offset voltage which is summed into the loop filter op amp U605 to shift up the 0 to 4 volt output of the phase detector. Calibration of the VCO is provided for in the software by altering the loaded values of this IC.
Deviation Compensation – U508 is a digital pot used to control the amplitude of the transmit modulation signal. As the transmit frequency increases, less voltage is needed at the VCO, so the modulation signal is attenuated.

Squelch Detection

U505 and associated circuitry form a bandpass filter that selects and amplifies the noise on the discriminator output near 20 kHz. The core microprocessor samples the output of the filter, averages a number of samples, and compares the result to a threshold number to determine if carrier is present.

CTCSS/CDCSS Decode

U506 and associated circuitry act as a filter and limiter for CTCSS/CDCSS decoding interface to the core microprocessor.

Power Control

The core microprocessor controls the output power of the transmitter by setting the reference voltage of a feedback control loop. U509 and associated circuitry integrate the difference between the reference voltage and the forward detected voltage from the directional coupler, and drives the amplifier/driver Q507. Q507 supplies bias to the low level transmitter driver stage collector.

RX/TX BOARD

Receiver

Buffer - Q101 is an L.O. buffer which provides approximately 15 dB of gain to supply the mixer and transmitter line-up.

Front End - The preselectors are varactor-tuned direct coupled filters with impedance transformations built into the configuration. The bipolar preamp provides approximately 18 dB of gain to overcome filter losses and provides a low noise figure.

Mixer/IF - The active singly-balanced JFET mixer converts the signal to an IF of 16.9 MHz where it is filtered by the crystal filters and amplified by the IF amplifier.

Demodulator IC - I1 is a multi-function IC which provides a second mixer, second IF oscillator, amplifier, and quadrature detection.

Antenna Switch- The antenna switch provide RX/TX isolation and switching using a TX series PIN diode pair (which is located on the High Level PA Board) and RX shunt PIN diode, with the coaxial cable running from the High Level PA Board to the RX/TX Board being one quarter wave-length at mid-band.

Front End Tuning- I2 is a Hex DAC that provides an independent tuning capability for each of the five varactor elements in the two pre-selectors.

Low Level Power Amplifier

Line- up- The low level power amplifier consists of the following stages and power levels:

Low Level Amp	to 0.02 watt
Driver	to 0.2 watt
Final	to 2.0 watts

Boardband matching networks are used throughout the line-up. The Low Level Amp runs class A, and the driver and final are operated in class C mode. The Power control voltage is applied to the driver stage collector.

HIGH LEVEL PA BOARD

Power Amplifier

The high level power amplifier consists of a driver stage with a nominal output power of 15 watts and a final stage with sufficient output power to provide 50 watts at the antenna port. Both stages utilize broadband matching networks and are operated in a class C mode.

Harmonic Filter

A 9^{th} order elliptical filter is used to attenuate harmonic components before they reach the antenna port.

Directional Coupler

A stripline directional coupler and associated detectors provide DC voltages proportional to the forward and reflected power at the antenna connector. The forward detected voltage is used for feedback to the power control loop and the reverse detected voltage is used to detect high VSWR conditions.

OPTIONS BOARD

Control Functions

The routing of audio signals through the options board is determined by analog switch I1. The audio path is controlled by outputs from the control board.

Receiver Audio

Low frequency tones are removed from the audio by a high-pass filter of I2A, I2B, I2C, and associated circuitry. De-emphasis is set by C23.

Transmitter Audio

I3D performs pre – emphasis, and I3C performs limiting. I3B is used as a buffer/amplifier and drives a three pole low pass filter consisting of I3D and associated circuitry. This low pass filter has a cutoff at 3 kHz and provides modulation filtering to within FCC requirements. The output is routed to the system board. Signaling tones are generated on the control boar and summed with the transmitter Audio at I3B.

CONTROL BOARD

Control Board functions include:

1. Microprocessor Control
2. EEPROM Storage
3. Regulation
4. Display Driver
5. Signaling
6. Audio Power Amplifier

Microprocessor Control

U102 controls the interface between the radio and the user. During normal operation, U102 monitors the front panel and push-to-talk switches, and provides data to the display. In the radio programming mode, U102 interprets commands from the serial bus and provides a transparent interface to the external programming source.

EEPROM Storage

EEPROM U105 is used to store the radio configuration and channel information, i.e., receive and transmit frequencies and code guard values for each channel.

Regulation

A switching regulator, U103, is used to generate +32 volts for the vacuum fluorescent display and driver. A +5 volt regulator, U108, is used to supply power requirements for the control and options boards.

Display Driver

Display driver U100 receives data to be displayed from U102 and drives the vacuum fluorescent display.

Signaling

U206 generates audible and subaudible tones (such as CTCSS).

Audio Power Amplifier

The audio amplifier, U107, can deliver a maximum of 4 watts into a 3.2 ohm load. Audio muting is provided by U109.

VCO Board

The VCO is a varactor tuned feedback oscillator using Q1 with feedback from tapped auto transformer T1. A steering voltage is used to set the capacitance of CR1, CR10, CR11, and CR12, which in turn controls the frequency of oscillation. CR3 provides a low sensitivity input for modulating the carrier frequency. The cascode amplifier comprised of Q6 isolates the VCO from its load and provides a nominal drive level of 0 dBm in receive and transmit.