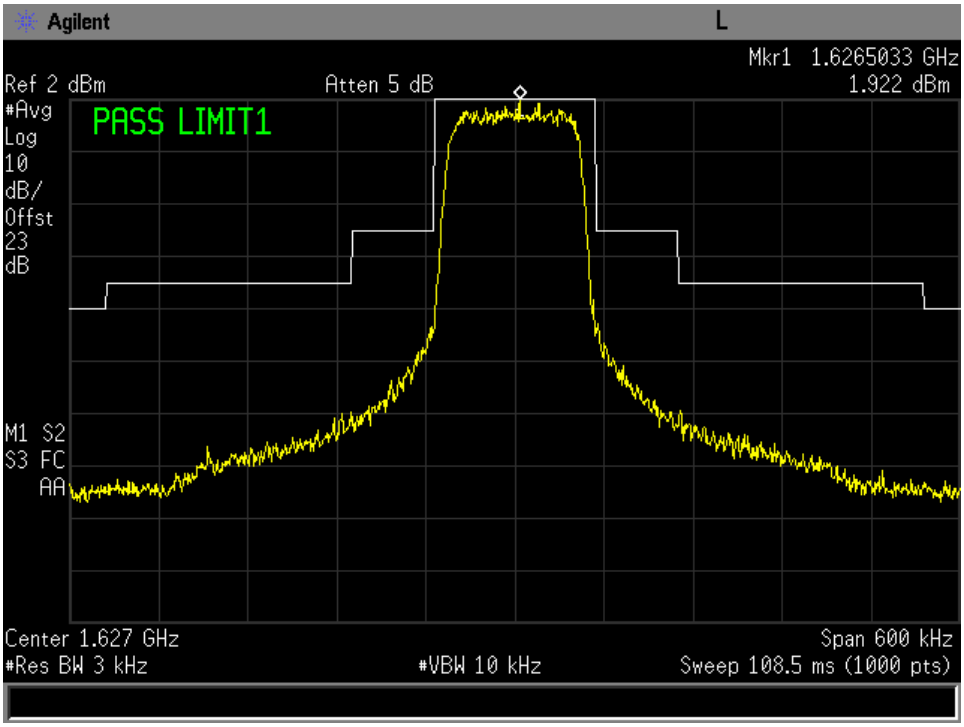
Annex D

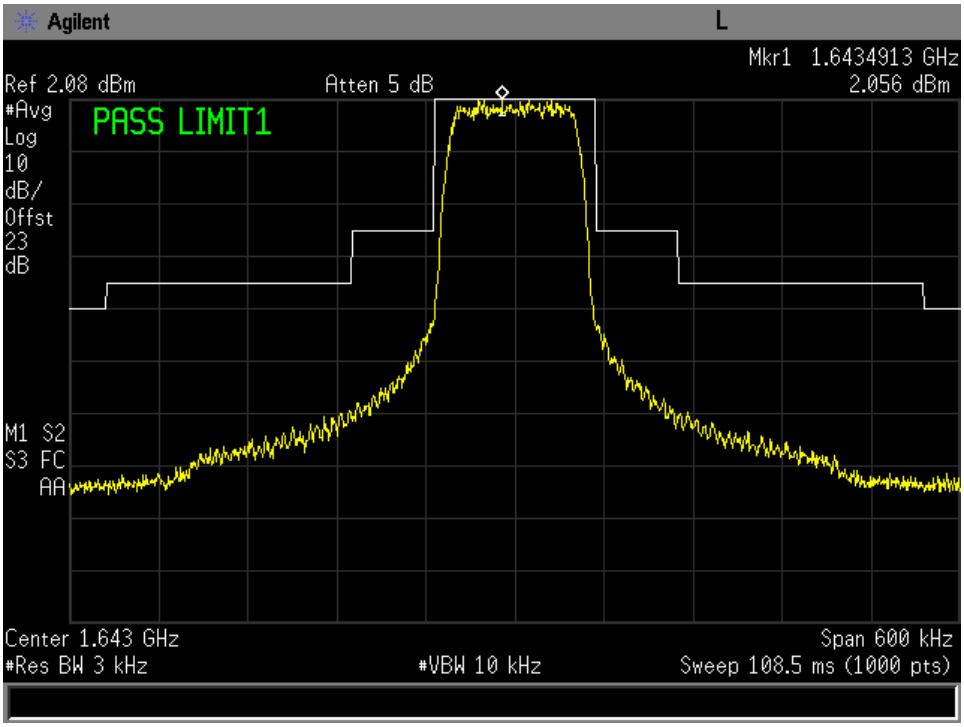
SUD 400

Emission Mask
87.139 (a), 87.139(i)

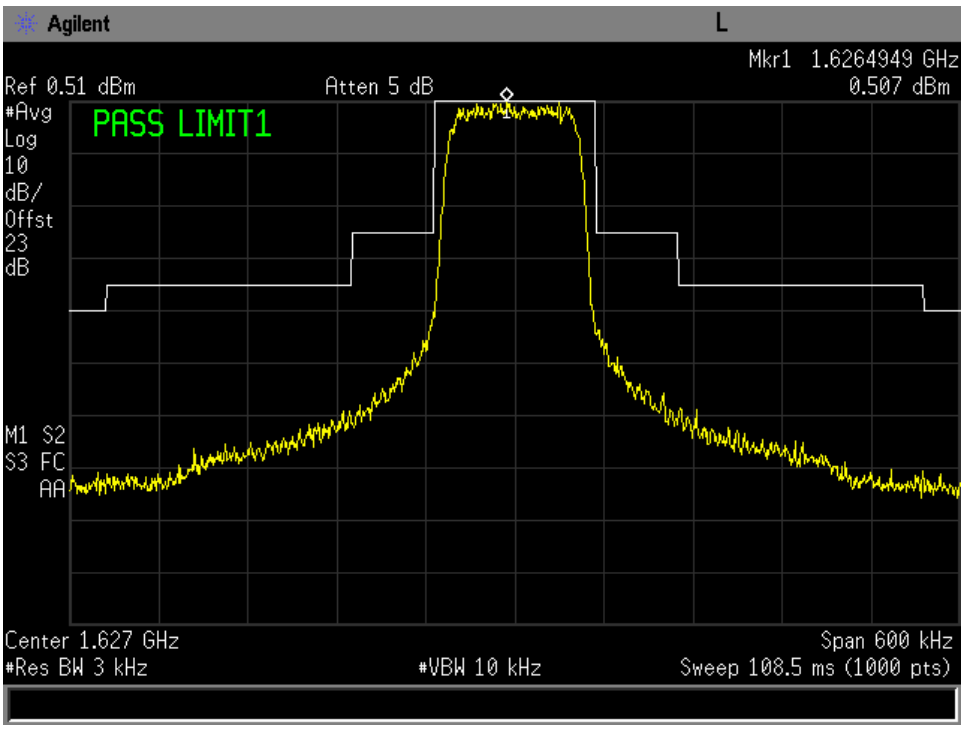
FR802.5X32 Low Channel



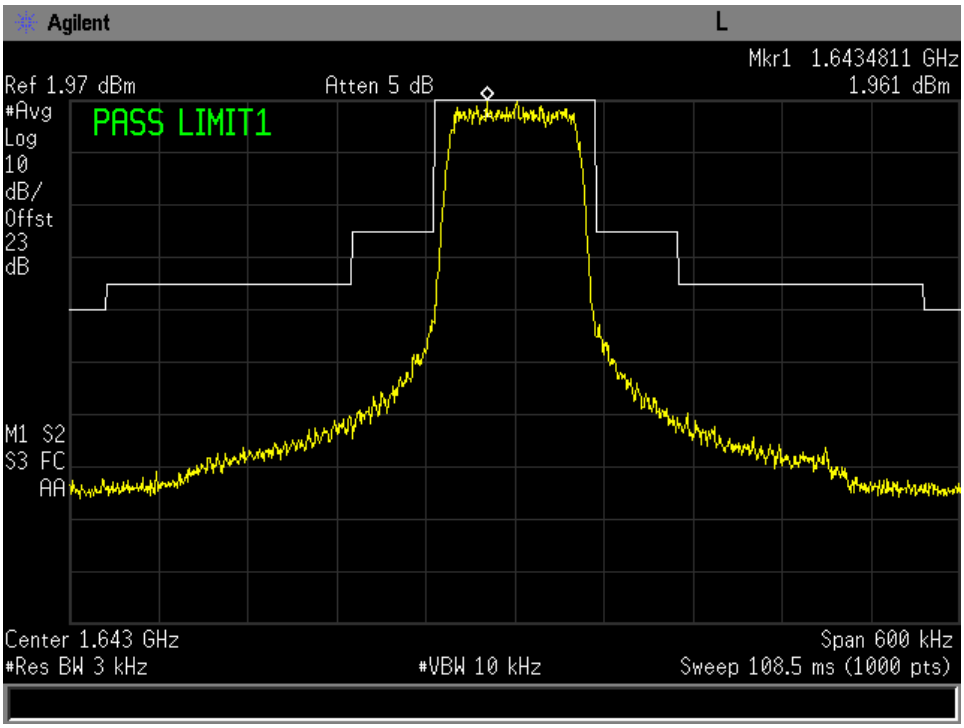
FR802.5X32 Mid Channel



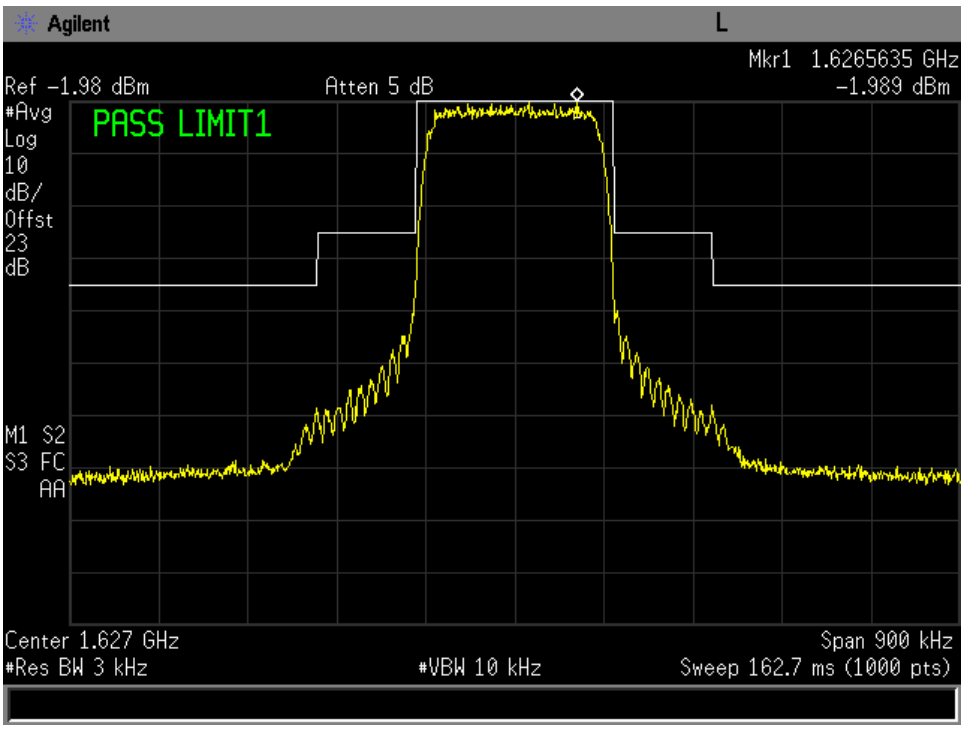
FR802.5X64 Low Channel



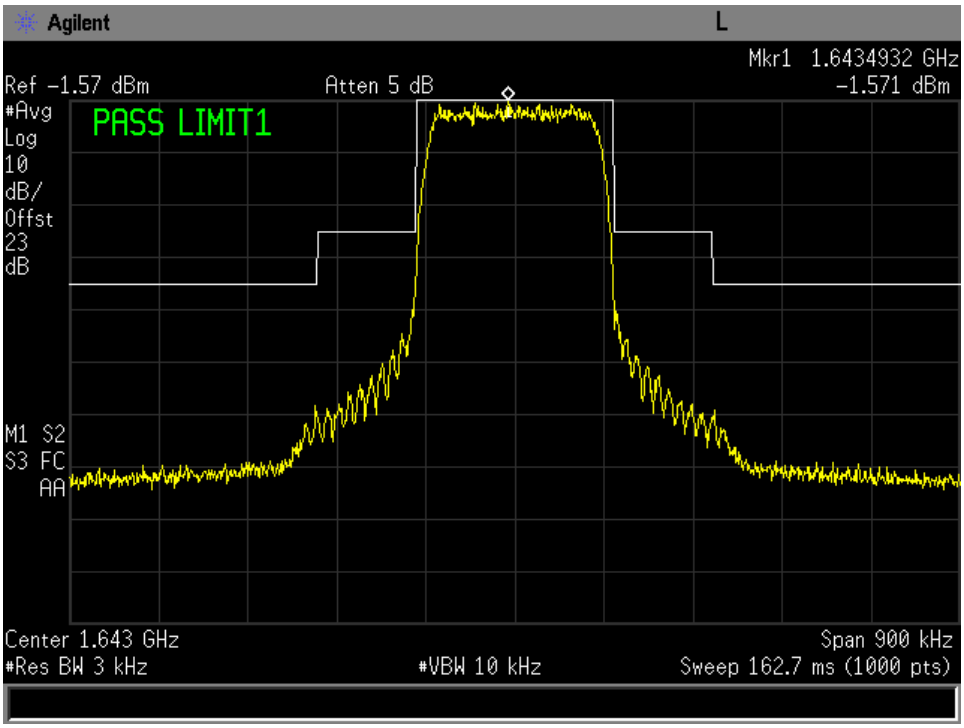
FR802.5X64 Mid Channel



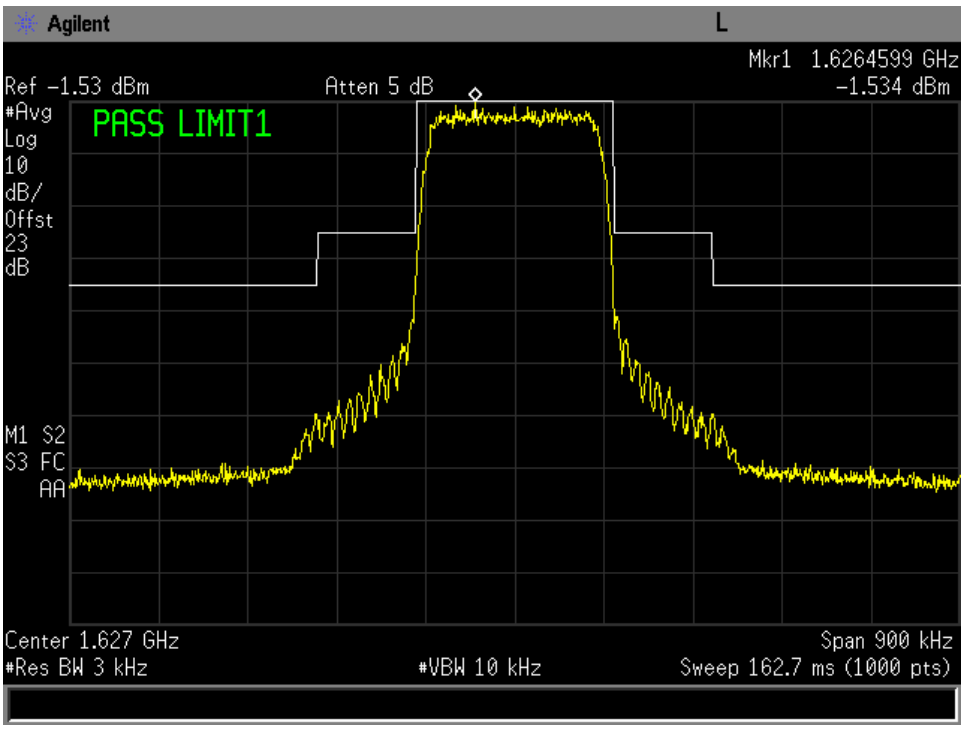
FR805X32 Low Channel



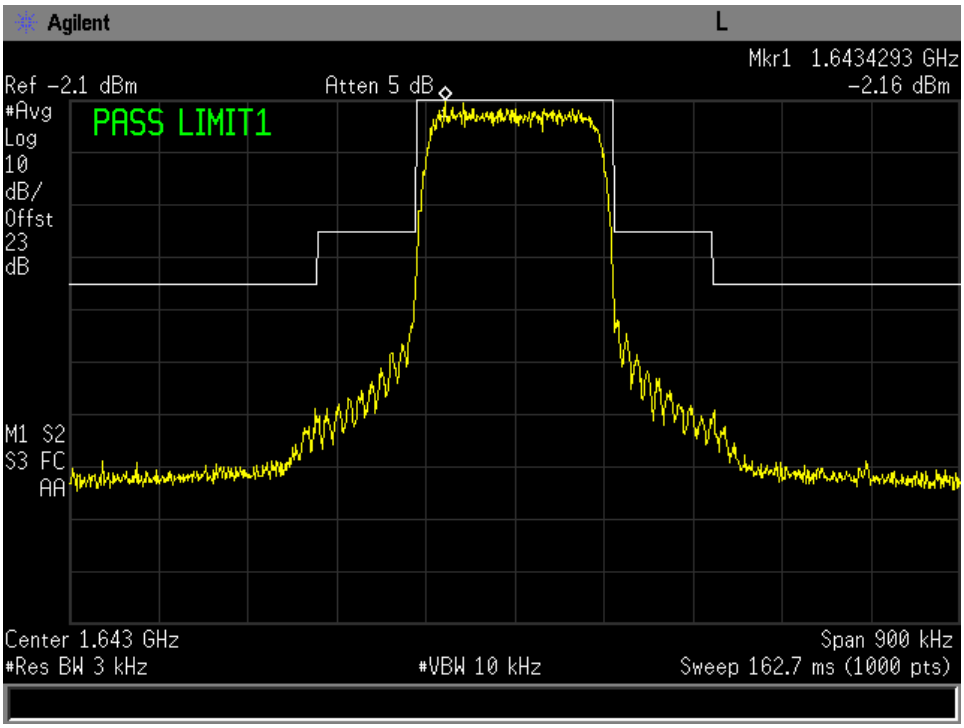
FR805X32 Mid Channel



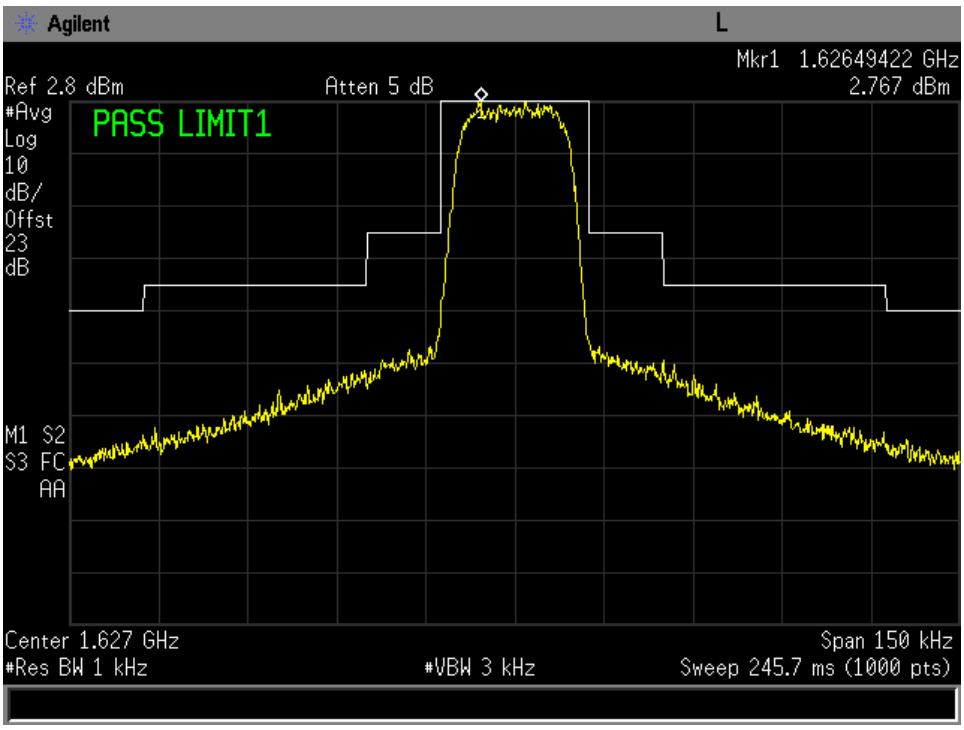
FR805X64 Low Channel



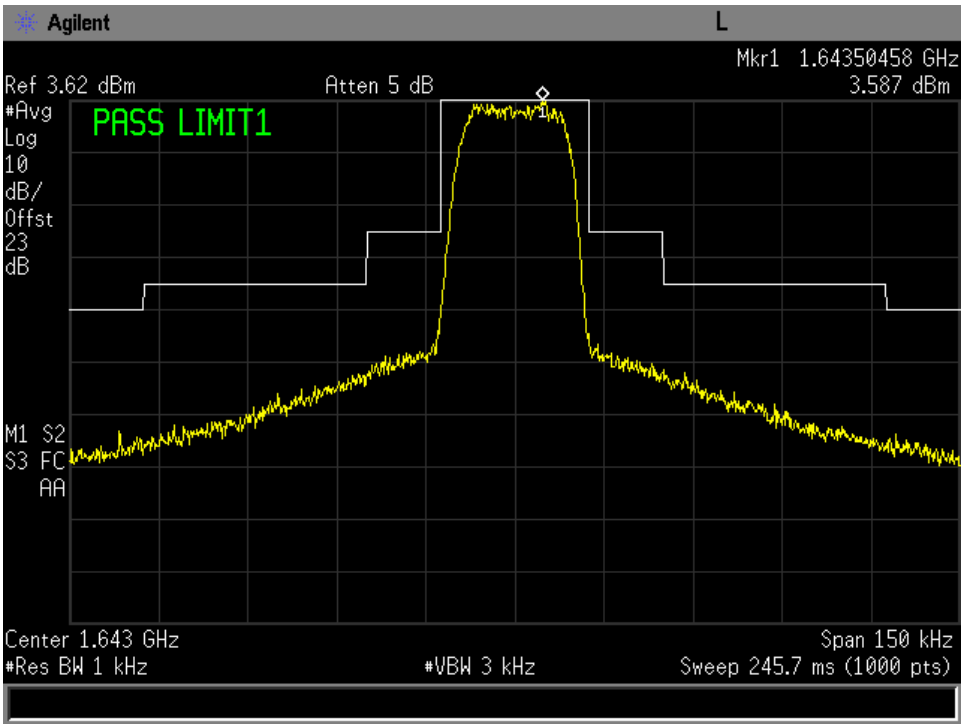
FR805X64 Mid Channel



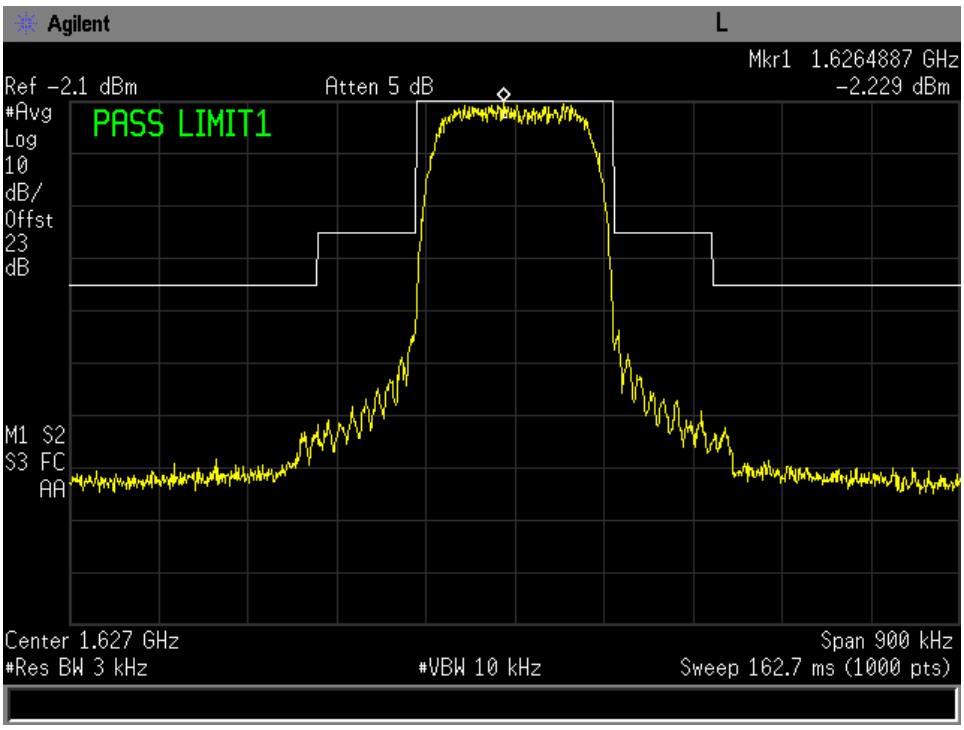
R20T0.5QD Low Channel



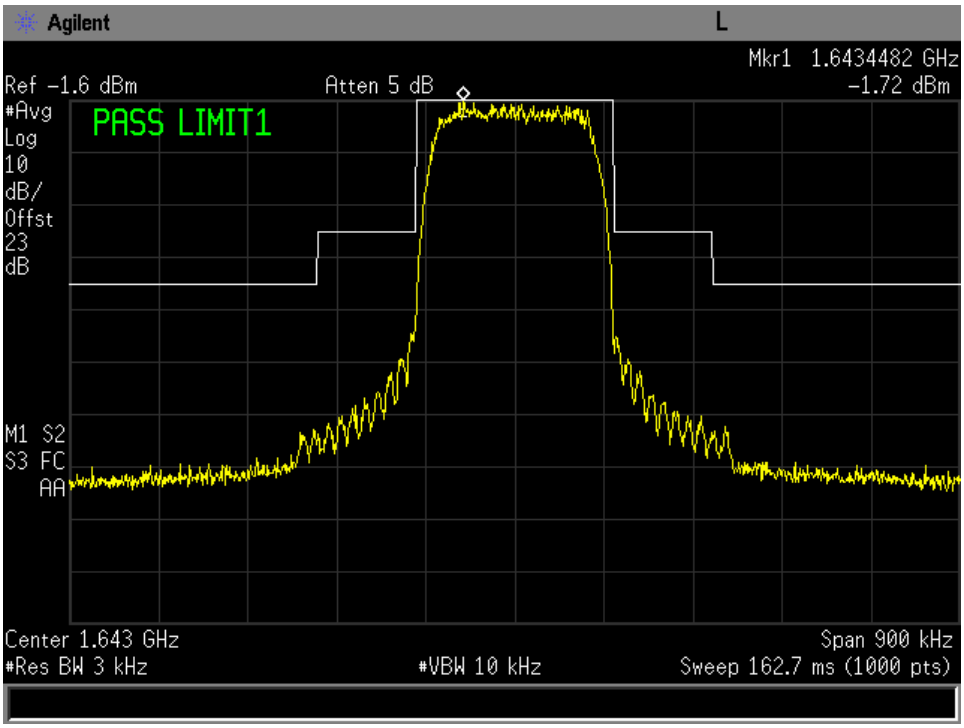
R20T0.5QD Mid Channel



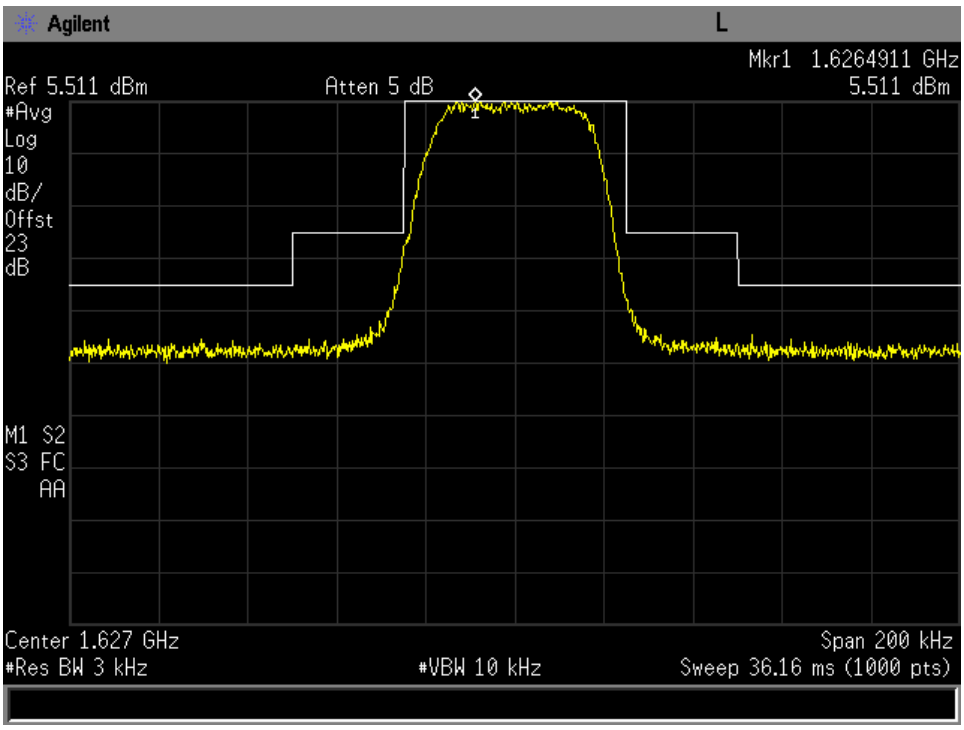
R20T4.5QD Low Channel



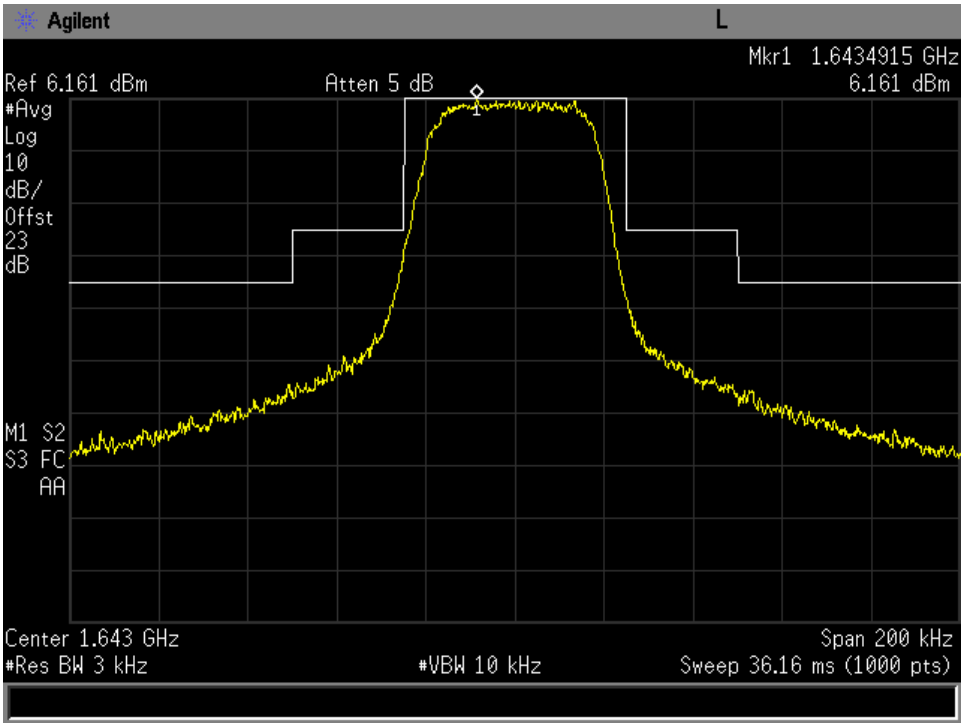
R20T4.5QD Mid Channel



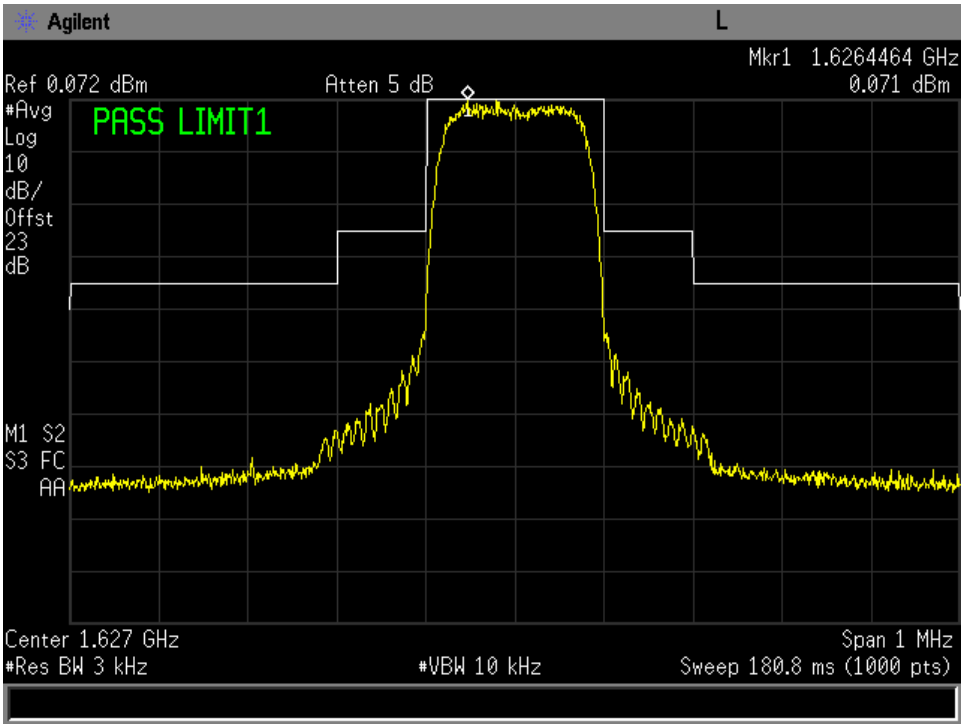
R5T1XD Low Channel



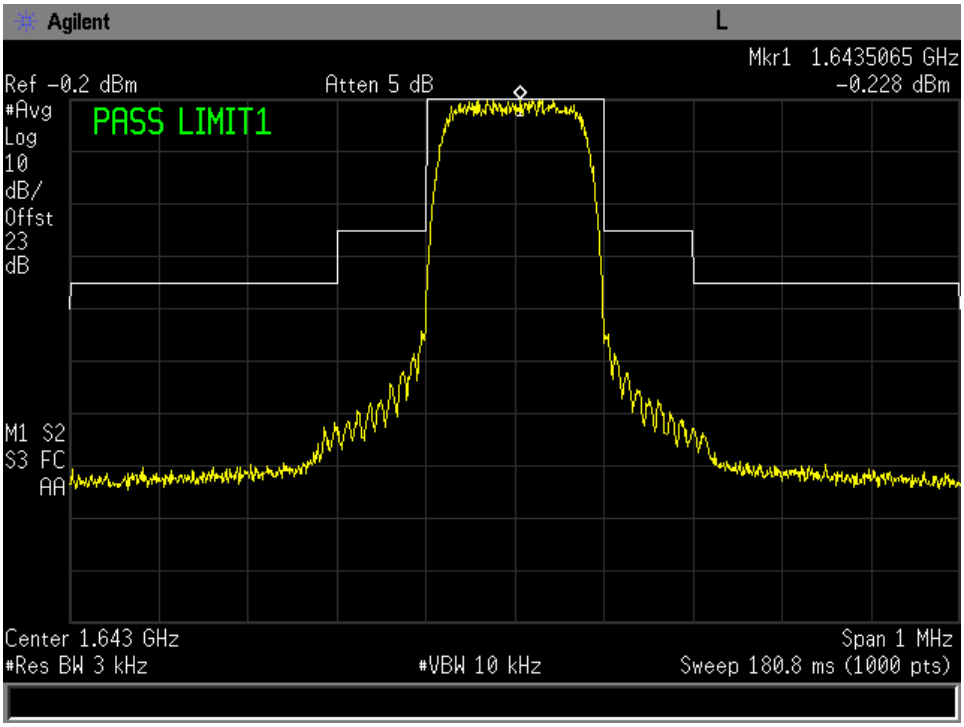
R5T1XD Mid Channel



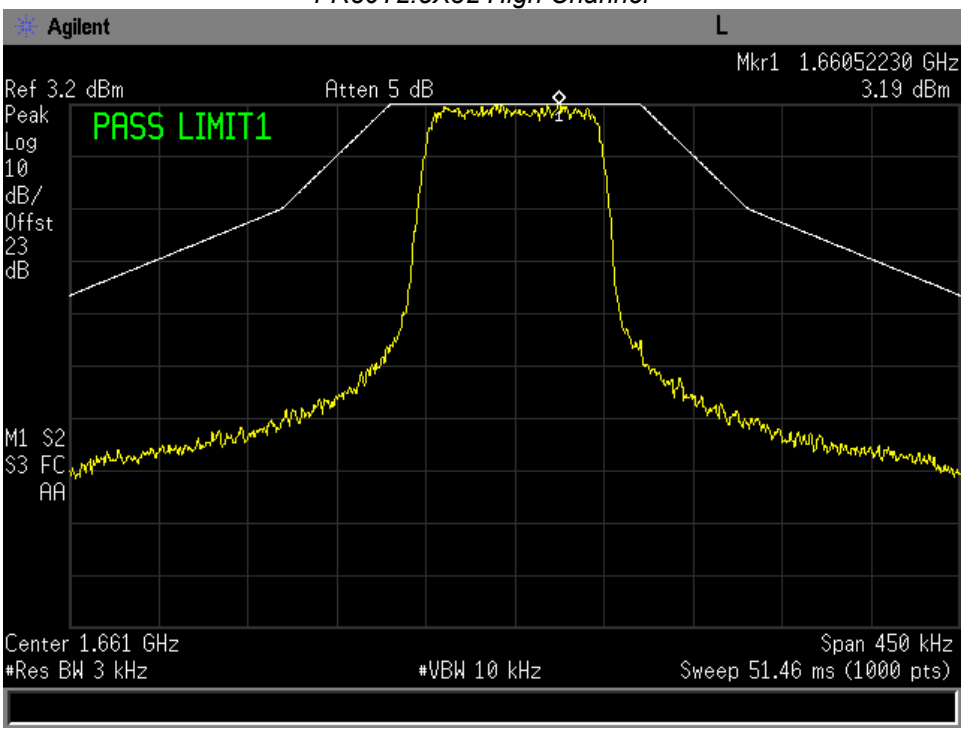
R5T4.5XD Low Channel



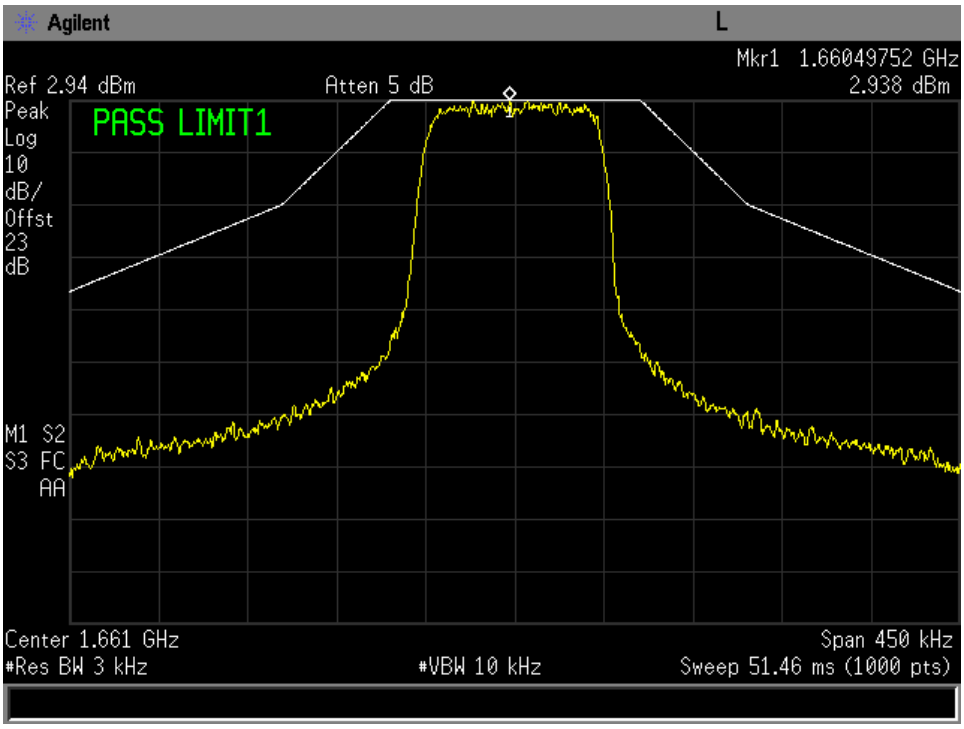
R5T4.5XD Mid Channel



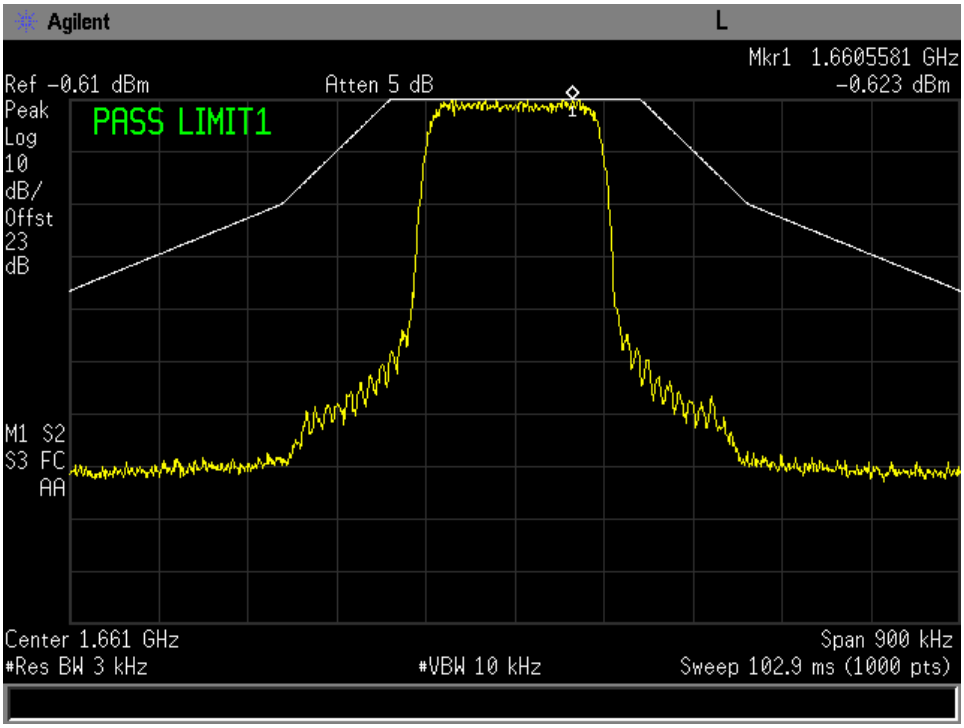
FR80T2.5X32 High Channel



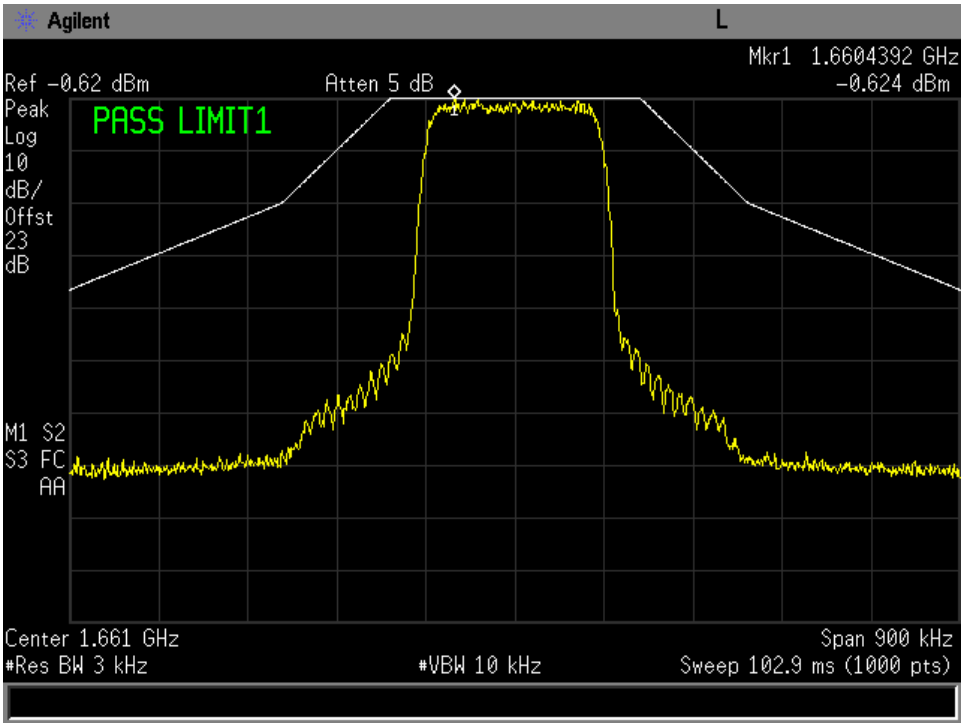
FR80T2.5X64 High Channel



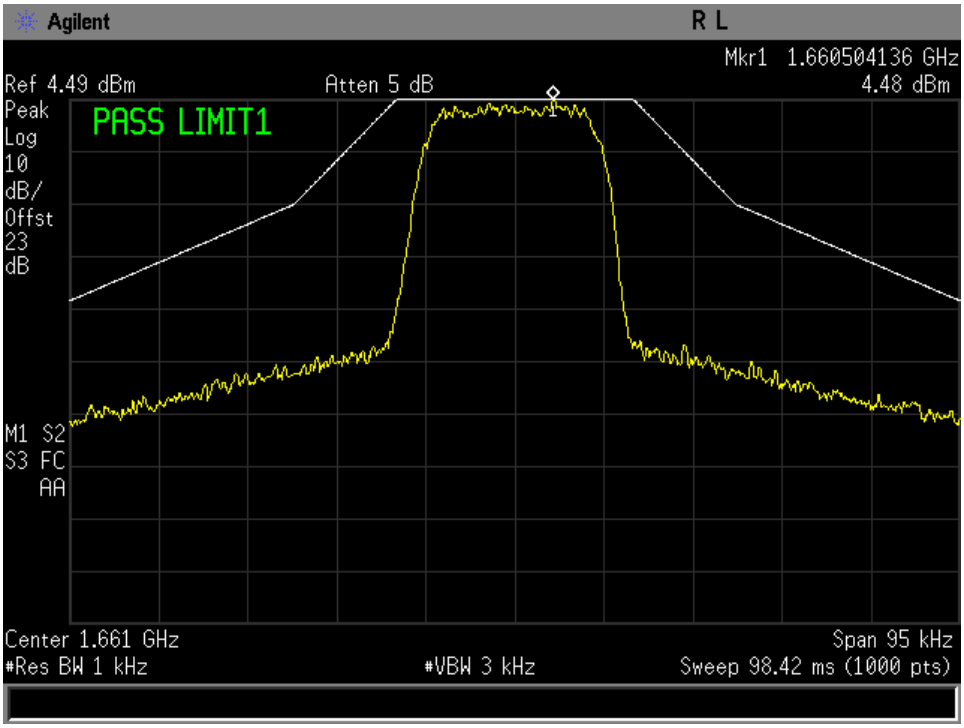
FR80T5X32 High Channel



FR80T5X64 High Channel



R20T0.5QD High Channel



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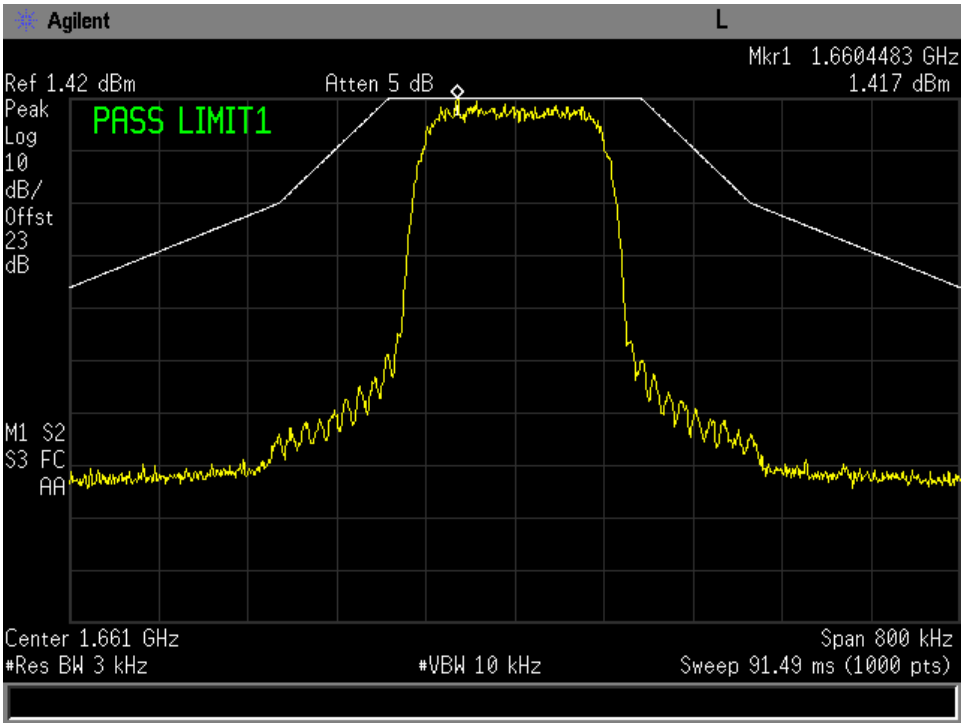
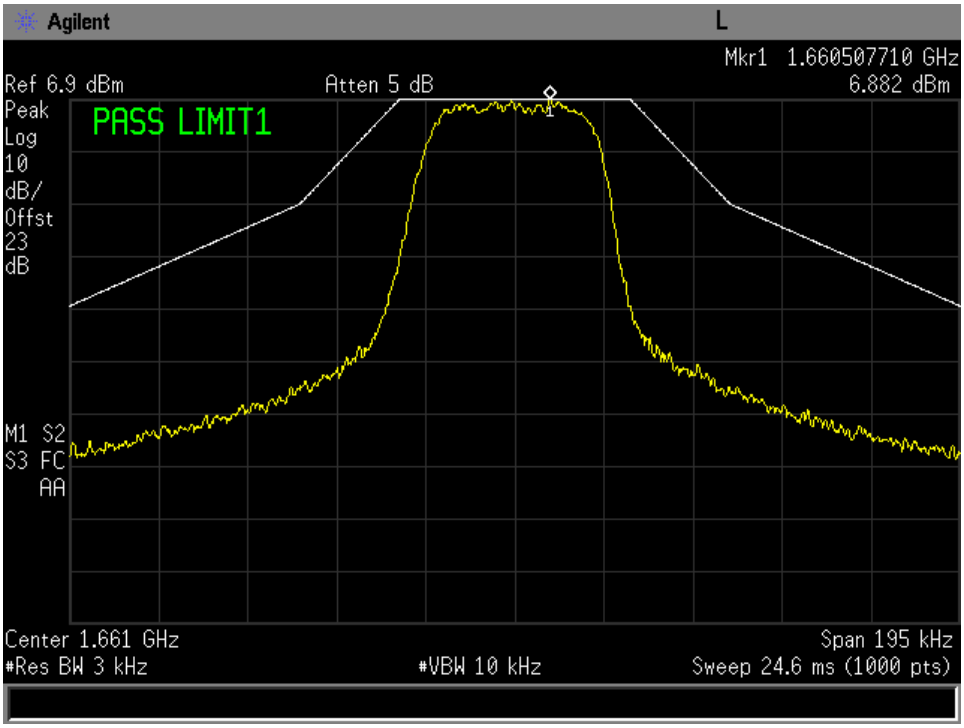


R5T1XD High Channel



R5T4.5XD High Channel