Receive Signal Path

Incoming RF from the RX antenna jack is delivered to the RX Unit and passes through the protection diode D3001 (**MA143**) and a varactor-tuned band pass filter consisting of coils L3002 and L3004, capacitors C3019, C3021, C3024, C3027, and C3028, and diodes D3004 and D3008 (both **HVU350**). Signals are then applied to the RF amplifier, Q3008 (**2SC3357**). The amplified RF signal is applied through a varactor-tuned band pass filter consisting of coils L3009 and L3012, capacitors C3053, C3054, C3059, C3060, and C3065, and diodes D3012 and D3013 (both **HVU350**) to the first mixer D3014 (**GN2011-Q**) along with the first local signal from the PLL circuit..

The first local signal is generated between 114.6 MHz and 152.6 MHz by the RX VCO, which consists of FET Q3007 (**2SK508**) and varactor diodes D3005, D3006, D3009, and D3010 (**HVU350**) according to the programmed receiving frequency; the local signal then passes through buffer amplifier Q3009 (**2SC5226**) and first local amplifier Q3011 (**2SC3357**) to the first mixer D3014.

The 21.4 MHz first IF signal is applied to monolithic crystal filters XF3001 and XF3002 (both **21M10B1**: ±10 kHz B.W.) which strip away unwanted mixer products, and the IF signal is applied to the first IF amplifier Q3016 (**2SC2620QB**). The amplified first IF signal is then delivered to the FM IF subsystem IC Q3012 (**TA31136FN**), which contains the second mixer, second local oscillator, limiter amplifier, noise amplifier, and FM detector.

The second local oscillator signal, generated by the 20.945 MHz crystal X3002, produces the 455 kHz second IF signal when mixed with the first IF signal within Q3021. The second IF signal passes through ceramic filter CF3001 (**CFWM455G**: ±4.5 kHz B.W.) or CF3002 (**CFWM455F**: ±6.0 kHz B.W.) which strips away all but the desired signal, and then passes through the limiter amplifier within Q3021 to ceramic discriminator CD3001 (**CDB455C7**), which removes any amplitude variations in the 455 kHz IF signal before detection of speech. The detected audio passes through the low pass filter, consisting of R3067 and C3115, which rejects the 455 kHz IF component, then delivers the audio to pin 12 of JP3001.

The audio signal from the RX Unit is delivered to the CNTL Unit and passes through the audio amplifier Q4014-3 (**NJM2902M**) to the active high pass filter section of Q4024 (**FX-805**) which rejects the sub-audible frequency component. The filtered audio signal is delivered to potentiometer VR4001, which adjusts the audio sensitivity to compensate for audio level variations, then passes through audio amplifier Q4014-2 (**NJM2902M**), audio switch Q4030 (**NJU4066BM**), a 20 dB attenuater consisting of R4180 and R4211, and limiter amplifier Q4018-2 (**NJM2902M**), to the electronic volume control Q4029 (**M51132FP**), where the maximum deviation is set. The audio signal subsequently passes through the 3-section active low pass filter consisting of Q4019-1/-2/-3 (**NJM2902M**) and audio amplifier Q4019-4 to J4008's pin10, providing the repeater transmit audio.

A portion of the audio signal from the active high pass filter section of Q4024 is de-emphasized by Q4020-1 (**NJM2902M**), providing a flat audio response. The filtered audio then passes through the active band pass filter Q4016 (**NJM2902M**) and audio mute gate Q4038 (**DTC323TK**) to audio power amplifier Q4043 (**TDA2003H**), providing up to 2 Watts of audio power to the 8Ω loudspeaker.

Sub-Audible Signaling (Decoder)

A portion of the audio signal from the audio amplifier Q4014-1 passes through the active low pass filter Q4014-2 and the low pass filtering section of Q4024 to separate the sub-audible tones from the received audio signal. The sub-audible tones are sent to the CTCSS/DCS decoder section of Q4024. When a CTCSS tone or DCS code is received, the CTCSS or DCS information is delivered to pin 20 of the Main CPU Q4012 from pin 4 of Q4024, which compares the CTCSS tone or DCS code with the programmed tone or code data. If the received CTCSS tone or DCS code matches the programmed tone or code, pin 39 of the Main CPU Q4012 goes low, turning on the squelch switch Q4036 (**DTC323TK**) and passing the received audio signal to the audio power amplifier, Q4043.

Squelch Control

The squelch circuit consists of noise amplifier Q3014 (**2SC4116**) and noise detector D3018 (**MA143**) on the RX Unit, and control circuitry within main microprocessor Q4012 on the CNTL Unit.

When no carrier is received, noise at the output of the audio detector stage of Q3012 is amplified by Q3014 (**2SC4116GR**), and then rectified by D3018 (**MA143**) to provide a DC control voltage for the squelch switch. The resulting DC voltage is delivered to pin 6 of JP3001.

The DC voltage from the RX Unit is delivered to the A-D analog input port (pin 31) of the Main CPU Q4012 (**HD64F3337YF16**) on the CNTL Unit, which compares the squelch threshold level to that which is memorized in EEPROM Q4008 (**NM93C86A**) or set by the front panel **SQL** control.

RX PLL and VCO Circuits

The receiver's PLL circuitry consists of PLL subsystem IC Q3001 (**MB15A02PFV1**) on the RX Unit, which contains a reference oscillator/divider, serial-to-parallel data latch, programmable divider, phase comparator and a swallow counter. Stability is obtained by a regulated 5 VDC supply via Q3021 (**TA78L05**) and temperature compensated 14.4 MHz crystal oscillator **X3001** via thermistor **TH3001** and **TH3002**.

The RX VCO, consisting of FET **Q3007** and varactor diodes **D3005**, **D3006**, **D3009**, and **D3010**, oscillates between 114.6 MHz and 152.6 MHz according to the programmed receiving frequency. The RX VCO output passes through buffer amplifier **Q3009** and first local amplifier **Q3011** to the first mixer **D3014**, as described previously. A portion of the RX VCO output is applied to the prescaler/swallow counter section in the PLL IC, Q3001. There the RX VCO signal is divided by 64 or 65, according to a control signal from the Main CPU **Q4012** on the CNTL Unit, before being applied to the programmable divider section of the PLL IC **Q3001**.

The data latch section of the PLL IC **Q3001** also receives serial dividing data from the Main CPU **Q4012**, which causes the pre-divided RX VCO signal to be further divided by 22,920 ~ 30,520 in the programmable divider section in the PLL IC **Q3001**, depending upon the desired receive frequency, so as to produce a 5 kHz or 6.25 kHz derivative of the current RX VCO frequency. Meanwhile, the reference divider section of the PLL IC **Q3001** divides the 14.4 MHz crystal reference from the reference oscillator **X3001** and **Q3002** (**2SC4116GR**) by 2880 (or 2304) to produce the 5 kHz (or 6.25 kHz) loop reference.

The 5 kHz or 6.25 kHz signal from the programmable divider (derived from the RX VCO) and that derived from the crystal are applied to the phase detector section of the PLL IC **Q3001**, which produces a pulsed output with pulse duration depending on the phase difference between the input signals. This pulse train is then converted to DC, low pass filtered, then fed back to the RX VCO varactor diodes **D3005**, **D3006**, **D3009**, and **D3010**.

Changes in the DC voltage applied to the varactor diodes **D3005**, **D3006**, **D3009**, and **D3010** affect the reactance in the tank circuit RX VCO **Q3007**, changing the oscillating frequency according to the phase difference between the signals derived from the RX VCO and the crystal reference oscillator. The RX VCO is thus phase-locked to the reference frequency standard.

Transmit Signal Path

The TX VCO, consisting of FET **Q2005** (**2SK508**) and varactor diodes **D2004** and **D2005**, oscillates between 136 MHz and 174 MHz according to the programmed transmit frequency. The theory of operation of the remainder of the PLL circuitry is similar to that of the RX PLL circuit; however, dividing data from the Main CPU **Q4021** on the CNTL Unit is such that the VCO frequency is the actual transmit frequency.

The speech audio from the CNTL Unit is applied to the varactor diode **D2005** (**HVU350**), which frequency modulates the TX VCO from the unmodulated carrier at the transmit frequency. The modulated transmit signal is buffered by **Q2008** (**2SC5226**), then passes through the RF amplifier **Q2010** (**2SC3357**) and RF diode switch **D2008** (**RN739F**) to the PA Unit.

The transmit signal is applied to the RF amplifier **Q1501** (**2SC3357**) and RF power module IC **Q1502** (**PF0310A**), then finally amplified by power amplifier **Q1507** (**2SC5125**) up to 50 Watts. Harmonic and spurious radiation in the final output is suppressed by a low pass filter consisting of coils L1511 ~ L1515, plus capacitors C1546, C1547, C1554, C1556, C1560, and C1566 on the PA Unit, before delivery to the TX antenna jack.

APC (Automatic Power Control)

RF power output from the final amplifier **Q1507** is sampled by C1548/C1558 and is then rectified by **D1503**/**D1504** (both **1SS319**). The resulting DC voltage is applied to the comparator **Q1509** (**TA75S01F**), where the voltage is compared with a reference voltage from the Main CPU **Q4021** on the CNTL Unit, to produce a control voltage for the Automatic Power Controller **Q1503** (**2SB1122S**) and **Q1504** (**2SC4116GR**), which regulates supply voltage to the RF power module IC **Q1502**, so as to maintain stable high (or low) output power under varying antenna loading conditions.

Control (CNTL) Unit

The CNTL Unit consists of 8-bit CPU **Q4012** (**HD64F3337YF16**), EEPROM **Q4008** (**BR93LC66RF**), RX and TX speech audio circuits, and various analog switches for the CPU and repeater interconnections.

Microprocessor operational code is stored in **Q4008**, while channel data and repeater configuration information is programmed from an external PC connected to the front panel's **MIC** jack via a VPL-1 programming cable.

The output from the Main CPU, **Q4012**, contains serial control data used for REPEATER/BASE mode control, as well as TX and RX PLL data. Crystal X4001 oscillates at 16 MHz, and provides stable clock timing for the Main

CPU. When the repeater is powered on, the voltage at pin 8 of **Q4012** becomes stable, and the output of voltage detector IC **Q4005** (**RH5VL45AA**), which is tied to **Q4012** (pin 1-RST) becomes high, resetting the Main CPU.

Base Operation *(Tx, Line-Input Audio)*

Line input from J4009 (pins 3 and 4) is impedance matched by transformer T4001, then passes through the audio amplifier **Q4018** (**NJM2902M**) and audio switch **Q4030** (**NJU4066BM**) to the pre-emphasis network at **Q4018-1**, where the signal is processed in the same manner as previously described. The line level can be attenuated by switch S4002, and line sensitivity can be adjusted to -10 dBm ~ +10 dBm by potentiometer VR4003 to compensate for audio line level variations.

Base Operation *(Tx, Mic-Input Audio)*

Microphone input is delivered past the MIC MUTE switch **Q4026** (**DTC323TK**), then passes through the audio amplifier and active low pass filter at **Q4021** (**NJM2902M**) to the pre-emphasis network at **Q4018-1**, where the signal is processed in the same manner as previously described.