Circuit Description

Reception and transmission are switched by "RX5V" and "TX5V" lines from the microprocessor unit (MPU). The receiver uses double-conversion-superheterodyne circuitry, with a 21.4 MHz 1st IF and 455 kHz 2nd IF. The 1st LO,produced by a PLL synthesizer,yields the 21.4 MHz 1st IF.

The 2nd LO uses a 20.945 MHz (21.4 MHz-455 kHz) signal generated by a crystal oscillator. The 2nd mixer and other circuits use a custom IC to convert and amplify the 2nd IF, and detect FM to obtain demodulated signals.During transmit, the PLL synthesizer oscillates at the desired frequency directly, for amplification to obtain RF power output. During transmit, voice modulation and CTCSS (or DCS) modulation are applied to this synthesizer.Transceiver functions, such as tx/rx control, PLL synthesizer settings, and channel programming, are controlled using the MPU.

Receiver

Incoming RF signals from the antenna connector are delivered to the MAIN Unit, and pass through a low-pass filter (LPF) consisting of coils L2001,L2002,L2004 & L2024, capacitors C2002,C2004,C2009,C2111,C2112,C2113 and C2114 and antenna switching diodes D2001, D2002 and D2013 to the receiver front end.

The signal is then band-pass filtered and amplified by Q2001 (**2C3356**). The signals are then fed to the input of the 1st mixer, Q2004 (**SGM2016AM**) ,where they are mixed with the 1st local signal from the PLL.The 21.4 MHz 1st mixer product then passes through monolithc crysral filters XF2001 and XF2002, and is amplified by Q2010 (**2SC2714Y**) and delivered to the input of the FM subsystem IC Q2013 (**MC3372ML**). This IC contains the 2nd mixer, a local oscillator, limiter amplifier, FM detector, and audio amplifier. The 2nd LO in the IF-IC is produced from crystal X2002 (20.945 MHz), and the 1st IF is converted to 455kHz by the 2nd mixer and stripped of unwanted components by ceramic filters CF2001 and CF2002. After passing through a limiter amplifier, the signal is demodulated by the FM detector.

Demodulated receive audio from the IF-IC is amplified by Q1005 (**NJM2902M**).After volume adjustment by the AF power amplifier Q1003 (**LA4425A**) and passed to the speaker jack.

PLL synthesizer

The 1st LO maintains stability from the PLL synthesizer by using a 12.8 MHz reference signal from crystal X2001. PLL synthesizer IC Q2009 (**MC145191F**) consists of a prescaler, reference counter, swallow counter, programmable counter, a serial data input port to set these counters based on the external data , a phase comparator, and charge pump.

The PLL-IC divides the 12.8 MHz reference signal by 1,280 using the reference counter (10.0 kHz comparison frequency). The VCO output is divided by the prescaler, swallow counter and programmable counter. These two signals are compared by the phase comparator and applied to the charge pump. A voltage proportional to their phase difference is delivered to the low-pass filter circuit, then fed back to the VCO as an error-correcting voltage,controlling and stabilizing the oscillating frequency.

The VCO is comprised of Q2008 (**2SC3356**) and D2003 (**HVU350**), and oscillates at 21.4 MHz during receive, and at the fundamental frequency during transmit, with direct frequency-modulation using varactor diode D2004 (**HVU350**). The VCO output passes through buffer amplifier Q2011 (**2SC3356**), and a portion is fed to the PLL IC, and at the same time amplified by Q2016 (**2SC3356**) to obtain stable output. The VCO DC supply is regulated by Q2017 (**2SC2812**). Synthesizer output is fed to the 1st mixer by diode switch D2010 (**1SS184**) during receive, and to drive amplifier Q2015 (**μPC2710**) for transmit. The reference oscillator feeds the PLL synthesizer, and is composed of crystal X2001(12.8 MHz),the temperature compensation circuit which includes D2007 (**1SS353**)and thermostats TH2001 and TH2002, and the transmit (DCS) modulation circuit D2005 D2006 (**HVU350**).

Transmitter

Voice audio from the microphone or external inputs passes through a low-pass filter Q1005 (**NJM2902M**),and a limiter amplifier and low-pass filter at Q1006 (**NJM2902M**),then is adjusted for optimum deviation level and delivered to the next stage.

Voice input from the microphone, or external inputs and CTCSS, are frequecy-modulated at the VCO of the synthesizer, while DCS audio is modulated by the reference frequency oscillator of the synthesizer. Synthesizer output, after passing through diode switch D2010 (**1SS184**), is amplified by driver Q2015 (**μPC2710**) and power module Q2003 (**M68739M**) to obtain full RF output. The RF penergy then passes through antenna switch D2001/ D2002 and a low-pass filter circuit and finally to the antenna connector.

RF output power from the final amplifier is sampled dy C2117 and C2118 and is rectified by D2017(**1SS321**).The resulting DC is fed through Automatic Power Controller Q2018 (**TA75S01F**) to transmitter power module,Q2003.

Generation of spurious products by the transmitter is minimized by the fundamental carrier frequency being equal to the final transmitting frequency, modulated directly in the transmit VCO. Additoinal harmonic suppression is provided by a low-pass filter consisting of L2001, L2002, and L2024 and C2002,C2004,C2009,C2111,C2112,C2113 and C2114, resulting in more than 60dB of harmonic suppression prior to delivery to the RF energy to the antenna.

DCS Demodulator

DCS signals are demodulated on the RF-UNIT, and are applied to low-pass filter in sections3 and 4 of Q1040 (**NJM2902M**) ,as well as the limiter comparator in section 1 of Q1040.

CTCSS encoder/decoder

Generation, demodulation, and detection of the CTCSS tones are carried out by IC Q1014 (**MX165C**).

MPU

Operation is controlled by 8-bit MPU IC Q1039 (**HD64F3334YTF**). The system clock uses a 9.8304 MHz crystal for a time base. IC Q1015 (**RH5VL45AA**) resets the MPU when the power is on, and monitors the voltage of the regulated 5V power supply line.

EEPROM

The EEPROM retains Tx and Rx data for all 16 channels, CTCSS data, DCS data, prescaler dividing, IF frequency, local oscillator injection side (upper/lower), and REF oscillator data (internal/external).