CIRCUIT DESCRIPTION

Receive Signal Path

Incoming RF from the antenna jack is passed through a low-pass filter and high-pass filter consisting of coils L1023, L1024, L1025, L1039, L1030 & L1031, capacitors C1260, C1266, C1267, C1269, C1270, C1272, C1273, C1274, C1276, C1278 & C1281 and antenna switching diodes D1034 and D1036 (both **RLS135**) to the receiver front end section.

Signals within the frequency range of the transceiver is applied to the receiver front end which contains RF amplifier Q1067 (**2SC5226**) and varactor-tuned band-pass filter consisting of coils L1012, L1014, L1018, L1019, L1027 & L1028, capacitors C1209, C1211, C1212, C1217, C1221, C1225, C1228, C1236 & C1275, and diodes D1029, D1031, D1032 & D1040 (all **HVU350**), then applied to the 1st mixer Q1068 (**2SC5226**).

Buffered output from the VCO is amplified by Q1030 (**2SC5226**) to provide a pure 1st local signal between 143.4 and 172.4 MHz for injection to the 1st mixer. The 35.4 MHz 1st mixer product then passes through monolithic crystal filter XF1001 (**35S15A**, 7.5 kHz BW) which strips away all but the desired signal, which is then amplified by mixer postamp Q1060 (**2SC4215Y**).

The amplified 1st IF signal is applied to the AM/FM IF subsystem IC Q1052 (**TK10931V**), which contains the 2nd mixer, 2nd local oscillator, limiter amplifier, noise amplifier and AM/FM detector.

A 2nd local signal is generated by PLL reference/2nd local oscillator Q1045 (**2SC4116GR**) from the 17.475 MHz crystal X1002 to produce the 450 kHz 2nd IF when mixed with the 1st IF signal within Q1052. The 2nd IF then passes through the ceramic filter CF1001 (**CFWM450D**) to strip away unwanted mixer products.

In the FM mode, a 2nd IF signal from the ceramic filter CF1001 applied to the limiter amplifier section of Q1052, which removes amplitude variations in the 450 kHz IF before detection of the speech by the ceramic discriminator CD 1001 (**CDBM450C24**). Detected audio from Q1052 is passed through the de-emphasis, consisting of the resistors R1102, R1105, R1111 & R1162, capacitors C1100, C1101, C1103 & C1145, and Q1028 (**NJM2904V**), then applied to the AF amplifier Q1028 (**NJM2904V**).

In the AM mode, detected audio from Q1052 is passed through the audio amplifier Q1028 (**NJM2904V**) and ANL circuit, then applied to the AF amplifier Q1028 (**NJM2904V**). When impulse noise received, a portion of the AM detector output signal

from the AM/FM IF subsystem Q1052, including pulse noise is rectified by D1019 (**BAS316**). The resulting DC is applied to the ANL MUTE gate Q1029 (**UMG2N**), thus reducing the pulse noises.

The processed audio signal from Q1028passes through the audio mute gate Q1016 (**DTC124TU**) and the volume control to the audio power amplifier Q1009 (**TDA72330**), providing up to 0.4 Watts to the headphone jack or 8 Ω loudspeaker.

A portion of the AF signal from the AM/FM IF subsystem Q1052 converted into DC voltage within the IC, and then passes through the AGC amplifier Q1059 (**2SA1602A**) and Q1062 (**UMW1**) to the inversion amplifiers Q1063 and Q1066 (both **2SC5226**). These amplifier reduce the amplifier gain of the IF amplifier Q1060 and the RF amplifier Q1067 while receiving a strong signal.

Squelch Control

When signal is received, appear the DC squelch control voltage at pin 15 of AM/FM IF subsystem Q1052 according to the receiving signal strength. This DC is applied to pin 16 of microprocessor Q1014.

The DC squelch control voltage is compared with the SQL threshold level by the microprocessor Q1014. If the DC squelch control voltage is higher, pin 89 of Q1014 goes high. This signal activate the AF MUTE gate Q1016 (**DTC124TU**), thus disabling the AF audio.

Also, the microprocessor stops scanning, if active, and allows audio to pass through the AF MUTE gate Q1016.

Transmit Signal Path

Speech input from the microphone is passed through the microphone sensitivity potentiometer VR1001 and microphone amplifier Q1005-3 (**NJM2904V**), then applied to the ALC amplifier Q1008 (**AN6123MS**). The amplified speech signal is passed through the high-pass filter Q1005-1 (**NJM2904V**) and low-pass filter Q1005-2 (**NJM2904V**), then applied to the power amplifier Q1061 (**2SK2973**) which AM modulate the Tx frequency with speech signal.

When using the optional headset, the SIDETONE signal from Q1011 (**UMG2**) becomes “HIGH”, turning Q1015 (**TC7S66FU**) on, therefore a portion of the speech signal applied to the AF power amplifier Q1009 as a monitor signal.

The carrier signal from the VCO Q1025 (**2SC5226**) passes through the buffer

amplifier Q1030 (**2SC5226**) and TX/RX switch D1027 (**MC2848**), then amplified by Q1047 (**2SC3356**) and Q1051 (**2SK2973**), then applied to the power amplifier Q1061 which increases the signal level up to 5 watts output power.

The transmit signal then passes through the antenna switch D1034 (**RLS135**), and is low-pass filtered to suppress away harmonic spurious radiation before delivery to the antenna.

Automatic Transmit Power Control

RF power output from the final amplifier is sampled by C1265/C1271 and is rectified by D1039 (**HSM88WA**). The resulting DC voltage passes through the Automatic Power Controller Q1057 (**NJU7012F**) to the APC attenuator D1010 (**RN739F**) and final amplifier Q1061(**2SK2974**), so as to control the power output.

Transmit Inhibit

When the transmit PLL is unlocked, pin 14 of PLL chip Q1031 (**LV2105V**) goes to a logic "HIGH". The resulting DC "unlock" control voltage is switches off TX inhibit switches Q1038 (**RT1N241M**), Q1040 (**2SC4116GR**), and Q1041 (**DTA143EU**) to disable the supply voltage to transmitter RF amplifiers Q1047, disabling the transmitter.

Spurious Suppression

Generation of spurious products by the transmitter is minimized by the fundamental carrier frequency being equal to the final transmitting frequency. Additional harmonic suppression is provided by a low-pass filter consisting of L1024, L1025 & L1029 and C1260, C1266, C1267, C1272, C1273 & C1278, resulting in more than 60 dB of harmonic suppression prior to delivery of the RF signal to the antenna.

PLL Frequency Synthesizer

PLL circuitry consists of VCO Q1025 (**2SC5226**), VCO buffer Q1030 & Q1039 (both **2SC5226**), and PLL subsystem IC Q1031 (**LV2105V**), which contains a reference divider, serial-to-parallel data latch, programmable divider and phase comparator.

Stability is maintained by a regulated 3.5 V supply via Q1044 (**2SB1132Q**) and

Q1034 (**S-81235SGUP-DQI**) which feeds the PLL reference oscillator Q1045 (**2SC4116GR**), as well as capacitors associated with the 17.475 MHz frequency reference crystal X1002.

In the receive mode, VCO Q1025 oscillates between 153.4 and 172.4 MHz. The VCO output is buffered by Q1030 and Q1039, and applied to the prescaler section of Q1031. There the VCO signal is divided by 64 or 65, according to a control signal from the data latch section of Q1031, before being applied to the programmable divider section of Q1031. The data latch section of Q1031 also receives serial dividing data from the microprocessor Q1014 (**LC87F72CBA**), which causes the pre-divided VCO signal to be further divided in the programmable divider section, depending upon the desired receive frequency, so as to produce a 5 kHz derivative of the current VCO frequency.

Meanwhile, the reference divider section of Q1031 divides the 17.475 MHz crystal reference from the reference oscillator Q1045 by 3495 to produce the 5 kHz loop reference. The 5 kHz signal from the programmable divider (derived from the VCO) and that derived from the reference oscillator are applied to the phase detector section of Q1031, which produces a pulsed output with pulse duration depending on the phase difference between the input signals. This pulse train is filtered to DC and returned to the varactor D1011 (**HVU350**).

Changes in the level of the DC voltage applied to the varactors affect the reactance in the tank circuit of the VCO, changing the oscillating frequency of the VCO according to the phase difference between the signals derived from the VCO and the crystal reference oscillator. The VCO is thus phase-locked to the crystal reference oscillator.

The output of the VCO Q1025 is buffered by Q1030 before application to the 1st mixer, as described previously.

For transmission, the VCO Q1025 oscillates between 118 and 137 MHz. The remainder of the PLL circuitry is shared with the receiver. However, the dividing data from the microprocessor is such that the VCO frequency is at the actual transmit frequency (rather than offset for IFs, as in the receiving case).

Receive and transmit buses select which VCO is made active by Q1021 (**RT1N241M**). FET Q1032 (**2SK880GR**) buffers the VCV line for application to the tracking band-pass filters in the receiver front end.

When the power saving feature is active, the microprocessor periodically signals to the PLL IC Q1032 to conserve power, and to shorten lock-up time.

Push-To-Talk Transmit Activation

The PTT switch on the microphone is fed through the PTT controller, Q1002 (**UMZ2N**), to pin 35 of microprocessor Q1014, so that when the PTT switch is closed, pin 88 of Q1014 goes high. This signals cut off the receiver by disabling the 5 V supply bus at Q1019 (**DTA143EU**) which feeds the front-end, FM IF subsystem IC Q1052, and receiver VCO circuitry. At the same time, Q1040 (**2SC4116GR**) and Q10341(**DTA143EU**) activates the transmit 5 V supply line to enable the transmitter.

VOR Circuit

When the transceiver is set in the navigation band (108.000-117.975 MHz), VOR CNTL port (pin 100 of Q1014) becomes "Low" turning the 3.5V supply bus Q1046 (**RT1P441U**) ON, therefore the VOR circuit ON.

A portion of the AF signal form the AM/FM IF subsystem IC Q1052 applied to the VOR circuit, consisting of Q1053(**NJM2901V**), and Q1058 (**NJM2902V**), where it is detected a variable signal and reference signal from a VOR station. The VOR circuit sends these signals to the microprocessor Q1014.