VXA-120 CIRCUIT DESCRIPTION

Receive Signal Path

Incoming RF from the antenna jack is passed through a low-pass filter and high-pass filter consisting of coils L1025, L1027, L1028, L1030, L1031 & L1034, capacitors C1231, C1235, C1236, C1238, C1240, C1242, C1243, C1244, C1245, C1246 & C1248 and antenna switching diodes D1032 and D1033 (both **RLS135**) to the receiver front end section.

Signals within the frequency range of the transceiver is applied to the receiver front end which contains RF amplifier Q1059 (**2SC5226**) and varactor-tuned band-pass filter consisting of coils L1013, L1016, L1021, L1022, L1032 & L1033, capacitors C1192, C1193, C1194, C1200, C1202, C1204, C1206, C1211, C1217, C1237, C1243 & C1247, and diodes D1027, D1029, D1030 & D1037 (all **HVU350**), then applied to the 1st mixer Q1061 (**2SC5226**).

Buffered output from the VCO is amplified by Q1023 (**2SC5226**) to provide a pure 1st local signal between 143.4 and 172.4 MHz for injection to the 1st mixer. The 35.4 MHz 1st mixer product then passes through monolithic crystal filter XF1001 (**35M15A1**, 7.5 kHz BW) which strips away all but the desired signal, which is then amplified by mixer postamp Q1056 (**2SC4215Y**).

The amplified 1st IF signal is applied to the AM/FM IF subsystem IC Q1047 (**TK10931V**), which contains the 2nd mixer, limiter amplifier, and AM/FM detector.

A 2nd local signal is generated by PLL reference/2nd local oscillator Q1040 (**2SC4116GR**) from the 17.475 MHz crystal X1002 to produce the 450 kHz 2nd IF when mixed with the 1st IF signal within Q1047. The 2nd IF then passes through the ceramic filter CF1001 (**CFWM450F**) to strip away unwanted mixer products.

In the FM mode, a 2nd IF signal from the ceramic filter CF1001 applied to the limiter amplifier section of Q1047, which removes amplitude variations in the 450 kHz IF before detection of the speech by the ceramic discriminator CD 1001 (**CDBM450C24**). Detected audio from Q1047 is passed through the de-emphasis, consisting of the resistors R1081, R1089, R1093 & R1135, C1136, and Q1033-2 (**NJM2904V**), then applied to 047 is passed through the audio amplifier Q1033-1

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(**NJM2904V**) and ANL circuit, then applied to the AF amplifier Q1033-2 (**NJM2904V**). When impulse noise received, a portion of the AM detector output signal from the AM/FM IF subsystem Q1047, including pulse noise is rectified by D1019 (**1SS355**). The resulting DC is applied to the ANL MUTE gate Q1028 (**FMG2**), thus reducing the pulse noises.

The processed audio signal from Q1033-2 passes through the audio mute gate Q1014 (**DTC124TU**) and the volume control to the audio power amplifier Q1005 (**TDA72330**), providing up to 0.3 Watts to the headphone jack or 8 Ω loudspeaker.

A portion of the AF signal from the AM/FM IF subsystem Q1047 converted into DC voltage within the IC, and then passes through the AGC amplifier Q1063 (**FMW1**) and Q1064 (**2SA1602A**) to the inversion amplifiers Q1057 and Q1060 (both **2SC5226**). These amplifier reduce the amplifier gain of the IF amplifier Q1056 and the RF amplifier Q1059 while receiving a strong signal.

Squelch Control

When signal is received, appear the DC squelch control voltage at pin 15 of AM/FM IF subsystem Q1047 according to the receiving signal strength. This DC is applied to pin 2 of microprocessor Q1012.

The DC squelch control voltage is compared with the SQL threshold level by the microprocessor Q1012. If the DC squelch control voltage is higher, pin 49 of Q1012 goes high. This signal activates the AF MUTE gate Q1014 (**DTC124TU**), thus disabling the AF audio.

Also, the microprocessor stops scanning, if active, and allows audio to pass through the AF MUTE gate Q1014.

Transmit Signal Path

Speech input from the microphone is passed through the microphone sensitivity potentiometer VR1001, and then applied to the ALC amplifier Q1003 (**AN5123MS**). The amplified speech signal is passed through the high-pass filter Q1006-1 (**NJM2904V**) and low-pass filter Q1006-2 (**NJM2904V**) to the AM modulator D1021 (**RN739F**).

When using the optional headset, the SIDETONE signal from Q1008 (**FMG2**) becomes “HIGH”,

turning Q1011 (**TC7S66FU**) on, therefore a portion of the speech signal applied to the AF power amplifier Q1005 as a monitor signal.

The carrier signal from the VCO Q1019 (**2SC5226**) passes through the buffer amplifier Q1023 (**2SC5226**) and TX/RX switch D1018 (**MC2848**) to the AM modulator D1021, where it is low-level modulation by an amplified speech signal.

The modulated signal from D1021 is amplified by Q1043 (**2SC5226**), Q1049 (**2SC3356**) and Q1051 (**2SK2973**), and ultimately applied to the final amplifier Q1055 (**2SK2975**) which increases the signal level up to 4 watts output power. The transmit signal then passes through the antenna switch D1032 (**RLS135**), and is low-pass filtered to suppress away harmonic spurious radiation before delivery to the antenna.

Automatic Transmit Power Control

RF power output from the final amplifier is sampled by C1234/C1239 and is rectified by D1035 (**1SS321**). The resulting DC is fed through the Automatic Power Controller Q1050 (**2SC4116GR**) to the APC attenuator D1024 (**RN739F**), thus allowing control of the power output.

Transmit Inhibit

When the transmit PLL is unlocked, pin 7 of PLL chip Q1026 (**MB15A01PFV1**) goes to a logic low. The resulting DC “unlock” control voltage is switches off TX inhibit switches Q1029 (**2SA1602A**), Q1031 (**RT1N241M**), Q1035 (**2SC4116GR**), and Q1036 (**DTA143EU**) to disable the supply voltage to transmitter RF amplifiers Q1043 and Q1048, disabling the transmitter.

Spurious Suppression

Generation of spurious products by the transmitter is minimized by the fundamental carrier frequency being equal to the final transmitting frequency. Additional harmonic suppression is provided by a low-pass filter consisting of L1027, L1028 & L1030 and C1231, C1235, C1236, C1240, C1242 & C1246, resulting in more than 60 dB of harmonic suppression prior to delivery of the RF signal to the antenna.

PLL Frequency Synthesizer

PLL circuitry consists of VCO Q1019 (**2SC5226**), VCO buffer Q1023 & Q1024 (both **2SC5226**), and PLL subsystem IC Q1026 (**MB15A01PFV1**), which contains a reference divider, serial-to-parallel data latch, programmable divider, phase comparator and charge pump.

Stability is maintained by a regulated 3.5 V supply via Q1030 (**S-81235SGUP-DQI**) which feeds the PLL reference oscillator Q1040 (**2SC4116GR**), as well as capacitors associated with the 17.475 MHz frequency reference crystal X1002.

In the receive mode, VCO Q1019 oscillates between 153.4 and 172.4 MHz. The VCO output is buffered by Q1023 and Q1024, and applied to the prescaler section of Q1026. There the VCO signal is divided by 64 or 65, according to a control signal from the data latch section of Q1026, before being applied to the programmable divider section of Q1026. The data latch section of Q1026 also receives serial dividing data from the microprocessor Q1012 (**M38257E8**), which causes the pre-divided VCO signal to be further divided in the programmable divider section, depending upon the desired receive frequency, so as to produce a 5 kHz derivative of the current VCO frequency.

Meanwhile, the reference divider section of Q1026 divides the 17.475 MHz crystal reference from the reference oscillator Q1040 by 3495 to produce the 5 kHz loop reference. The 5 kHz signal from the programmable divider (derived from the VCO) and that derived from the reference oscillator are applied to the phase detector section of Q1026, which produces a pulsed output with pulse duration depending on the phase difference between the input signals. This pulse train is filtered to DC and returned to the varactor D1012 (**HVU350**).

Changes in the level of the DC voltage applied to the varactors affect the reactance in the tank circuit of the VCO, changing the oscillating frequency of the VCO according to the phase difference between the signals derived from the VCO and the crystal reference oscillator. The VCO is thus phase-locked to the crystal reference oscillator.

The output of the VCO Q1019 is buffered by Q1023 before application to the 1st mixer, as described previously.

For transmission, the VCO Q1019 oscillates between 118 and 137 MHz. The remainder of the PLL circuitry is shared with the receiver. However, the dividing data from the microprocessor is such that the VCO frequency is at the actual transmit frequency (rather than offset for IFs, as in the

receiving case).

Receive and transmit buses select which VCO is made active by Q1017 (**RT1N241M**). FET Q1027 (**2SK880GR**) buffers the VCV line for application to the tracking band-pass filters in the receiver front end.

When the power saving feature is active, the microprocessor periodically signals to the PLL IC Q1026 to conserve power, and to shorten lock-up time.

Push-To-Talk Transmit Activation

The PTT switch on the microphone is fed through the PTT controller, Q1001 (**UMZ2N**), to pin 41 of microprocessor Q1012, so that when the PTT switch is closed, pin 18 of Q1012 goes high. This signals the microprocessor to activate the TX/RX controller Q1062 (**FMW-1**), which cut off the receiver by disabling the 5 V supply bus at Q1016 (**DTA143EU**) which feeds the front-end, FM IF subsystem IC Q1026, and receiver VCO circuitry. At the same time, Q1035 (**DTA143EU**) and Q1036 (**2SC4116GR**) activates the transmit 5 V supply line to enable the transmitter.