VX-800U Circuit Description

1. Overview

The VX-800U is a UHF/FM hand-held transceiver designed to operate in the frequency range of 400 to 512MHz.

2. Circuit Configuration by Frequency

The receiver is a double-conversion superheterodyne with a first intermediate frequency @(IF) of 44.25MHz and a second IF of 450kHz. Incoming signals from the antenna are mixed with the local signal from PLL to produce the first IF of 44.25MHz.

This is then mixed with the 43.8MHz second local oscillator (using the 14.6MHz reference crystal) output to produce the 450kHz second IF. This is detected to give the demodulated signal.

The transmit signal frequency is generated by PLL VCO, and modulated by the signal from the microphone. It is then amplified and sent to the antenna.

3. Receive Signal Path

3-1 Front-end RF amplifier

Incoming RF from the antenna jack is delivered to the RF Unit and passes through a low-pass filter and high-pass filter consisting of coils L1004, L1005, L1006, L1030, L1001, L1028, L1029, L1002 & L1003, capacitors C1013, C1014, C1015, C1017, C1019, C1020, C1282, C1001, C1005, C1006, C1283, C1007, C1008, & C1009 and antenna switching diode D1020 (HSU277).

Signals within the frequency range of the transceiver are then amplified by Q1001 (2SC4227-R34) and enter a varactor-tuned band-pass filter consisting of coils L1008, L1010 & L1011, capacitors C1041, C1042, C1044, C1045, C1046, C1047, C1068, C1069, C1070, C1071, C1072, C1073, C1074 & C1174 and diodes D1018, D1023 & D1024 (all HVC350) before first mixer.

3-2 First Mixer

Buffered output from the VCO is amplified by Q1030 (2SC5226-4/5) to provide a pure first local signal between 355.75 and 467MHz for injection to the first mixer D1030 (GN2011-Q). The 44.25MHz first mixer product then passes through monolithic crystal filters XF1001, XF1002 (44-11BF-P2, +/- 5.5 kHz BW) to strip away all but the desired signal.

3-3 IF amplifier

The first IF signal is amplified by Q1037 (2SC4215Y).

The amplified first IF signal is applied to FM IF subsystem IC Q1046 (BA4116FV) which contains the second mixer, second local oscillator, limiter amplifier, noise amplifier, and S-meter amplifier.

A second local signal is generated by Q1022 (2SC4617) using the 14.6MHz crystal X1002 as a reference, producing a 43.8MHz signal which yields a 450kHz second IF when mixed with the first IF signal within Q1046.

The second IF then passes through the ceramic filter CF1001 (PBFC450R15D), CF1002 (SFPC450G: only Narrow Channel) to strip away unwanted mixer products, and is applied to the limiter amplifier in Q1046, which removes amplitude variations in the 450kHz IF, before detection of the speech by the ceramic discriminator CD1001 (CDBC450CX24).

3-4 Audio amplifier

Detected audio from Q1046 is applied to Q1028 (AK2345) and audio low-pass filter, and then past the volume control (Q1025: M62364FP) to the audio amplifier Q1017 (TDA2822D; external speaker) or Q1063 (TDA2822D; internal speaker), providing up to 0.5 Watts to the optional headphone jack or 16-ohm loudspeaker.

Attention: *Audio output is BTL output.*

3-5 Squelch Control

The squelch circuitry consists of a noise amplifier & band-pass filter within Q1046, and noise detector D1053 (DA221).

When no carrier received, noise at the output of the detector stage in Q1046 is amplified and band-pass filtered by the noise amplifier section of Q1046 and the network between pins 7 and 8, and then rectified by D1053.

The resulting DC squelch control voltage is passed to pin 19 of the microprocessor Q1048. If no carrier is received, this signal causes pin 32 of Q1048 to go low and pin 89 to go high. Pin 32 signals Q1008 (CPH6102), Q1064 (2SA1774-R) and Q1065 (2SA1774-R) to disable the supply voltage to the audio amplifier Q1017 and Q1063, while pin 89 makes Q1014 (UMA2N) hold the green (Busy) half of the LED off, when pin 32 is low and pin 89 is high.

Thus, the microprocessor blocks output from the audio amplifier, and silences the receiver while no signal is being received, and during transmission.

When a carrier appears at the discriminator, noise is removed from the output, causing pin 19 of Q1048 to go low and the microprocessor to blink the busy LED via Q1048.

The microprocessor then checks the DTMF decoder chip on the Optional Unit, the CTCSS and the CDCSS code for DTMF or CTCSS or CDCSS code squelch information, if enabled, respectively. If not transmitting and CTCSS or CDCSS is not activated, or if the received tone or code matches that programmed, the microprocessor stops scanning, if active, and allows audio to pass through the audio amplifier Q1017, Q1063 (TDA2822D) to the loudspeaker by enabling the supply voltage to it via Q1008, Q1064 and Q1065.

4. Transmit Signal Path

4-1 Microphone amplifier

Speech input from the microphone is amplified in Q1022 (BA10324AFV) after there is a filter and is sent to Q1025 (M62364FP) and sent to Dummy Unit (or Optional Unit). The audio, which returned from Dummy Unit, passes Q1028 (AK2345) to be pre-emphasized.

The processed audio is then mixed with a CTCSS tone generated by Q1028 (AK2345) and delivered to D1035 (HVC350) for frequency modulating the PLL carrier up to +/- 5kHz from the unmodulated carrier at the transmitting frequency.

If an external microphone is used, PTT switching is controlled by Q1007 (UMZ2N), which signals the microprocessor when the impedance at the microphone jack drops.

If a CDCSS code is enabled for transmission, the code is generated by microprocessor Q1048 and delivered to D1055 (HVC350) for CDCSS modulating.

If DTMF is enabled for transmission, the tone is generated by the microprocessor Q1048 and applied to the splutter filter section in place of speech audio. Also, the tone is amplified for monitoring in the loudspeaker.

4-2 Noise canceling microphone circuit

The two signals from internal microphone (main and sub) are input to the positive input (sub) and to the negative input (main) and of the Q1022 (BA10324AFV). If the same signal is input to both main and sub, the main signal is canceled at the output of Pin7 of the Q1022. In other words, noise from nearby sources not directly connected to the transceiver enters the main and sub input at the same signal and is therefore canceled out.

When a signal is only input to main and there is no signal at sub, the main signal is output as is from Q1022.

4-3 Drive and Final amplifier

The modulated signal from the VCO Q1039 (2SC5226-4/5) is buffered by Q1034 (2SC5226-4/5) and amplified by Q1030 (2SC5226-4/5) and Q1060 (2SC3356-R25). The low-level transmit signal is then applied to the Power Module Q1019 (M68732HA-22) for final amplification up to 5 watts output power.

The transmit signal then passes through the antenna switch D1020 (HSU277) and is low-

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pass filtered to suppress away harmonic spurious radiation before delivery to the antenna.

4-4 Automatic Transmit Power Control

RF power output from the final amplifier is sampled by C1016, C1018, is rectified by D1019 (RB715F). The resulting DC is fed back through Q1018 (BA1324AFV) to the Power Module, and thus the power output.

The microprocessor selects either “High” or one of three “Low” power levels.

4-5 Transmit Inhibit

When the Transmit PLL is unlocked, pin 18 of PLL chip Q1054 goes to logic low. The resulting DC unlock control voltage is passed to pin 20 of the microprocessor Q1048. While the transmit PLL is unlocked, pin 85 of Q1048 remains low, which then turns off the Automatic Power Controller Q1010 (UMC5N) and Q1018 (BA1324AFV) to disable the supply voltage to the Power Module Q1019, disabling the transmitter.

4-6 Spurious Suppression

Generation of spurious products by the transmitter is minimized by the fundamental carrier frequency being equal to final transmitting frequency, modulated directly in the transmit VCO. Additional harmonic suppression is provided by a low-pass filter consisting of L1004, L1005 & L1006 and C1013, C1014, C1015, C1017, C1019 & C1020, resulting in more than 60 dB of harmonic suppression prior to delivery to the antenna.

5 PLL Frequency Synthesizer

PLL frequency synthesizer consists of the VCO Q1033 (2SK508-K52:RX) and Q1039 (2SC5226-4/5:TX), VCO buffers Q1033 (2SC5226-4/5), Q1041 (2SC5225-4/5), Q1030 (2SC5225-4/5), PLL subsystem IC Q1054 (SA7025DK) and 14.6MHz reference crystal X1002.

The frequency stability is +/- 2.5ppm within temperature range of –30 to +60 degree. The output of the 14.6MHz reference is applied to pin 8 of the PLL IC.

While receiving, VCO Q1033 oscillates between 355.75 and 467.75MHz according to the transceiver version and the programmed receiving frequency. The VCO generates 355.75 to 467.75MHz for providing to the first local signal. In TX, the VCO generates 400 to 512MHz.

The output of the VCO is amplified by the Q1041 and routed to the pin 5 of the PLL IC. Also the output of the VCO is amplified by the Q1030 and routed first local /Power Module according to D1031.

The PLL IC consists of a prescaler, fractional divider, reference divider and phase comparator and charge pump. This PLL IC is fractional-N type synthesizer and performs in the 40 or 50kHz reference signal, which is eighth of the channel step (5, 6.25 or 7.5kHz). The input signal from pin 5 and 8 of the PLL IC is divided down to the 40 or 50kHz and compared at phase comparator. The pulsed output signal of the phase comparator is applied to the charge pump and transformed into DC signal in the loop filter. The DC signal is applied to the pin 1 of the VCO and locked to keep the VCO frequency constant.

PLL date is output from DTA (pin100), CLK (pin2) and PSTB (pin98) of the microprocessor Q1048. The data are input to PLL IC when the channel is changed or when transmission is changed to reception and vice versa. A PLL lock condition is always monitored by the pin20 of the Q1048. When the PLL is unlocked, the UL goes low.

6. Miscellaneous Circuits

6-1 Push-To-Talk Transmit Activation

The PTT switch on the microphone is connected to pin 36 of microprocessor Q1048, so that when the PTT switch is closed, pin 85 of Q1048 goes high. This signals the microprocessor to activate the TX / RX controller Q1004 (UMG2N), which then disables the receiver by disabling the 5 V supply bus at Q1011 (UN911F) to the front-end, FM IF subsystem IC Q1046 and receiver VCO circuitry.

At the same time, Q1003 (XP1501), Q1002 (CPH6102) activates the TX 5V supply line

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to enable the transmitter.

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