VX-5500L Circuit Description

Reception and transmission are switched by "RX" and "TX" lines from the microprocessor unit (MPU). The receiver uses double-conversion super-heterodyne circuitry, with a 17.7MHz 1st IF and 450 kHz 2nd IF. The 1st LO, produced by a PLL synthesizer, yields the 17.7MHz 1st IF.

The 2nd LO uses a 17.25 MHz (17.7 MHz-450 kHz) signal generated by a crystal oscillator. The 2nd mixer and other circuits use a custom IC to convert and amplify the 2nd IF, and detect FM to obtain demodulated signals. During transmit, the PLL synthesizer oscillates at the desired frequency directly, for amplification to obtain RF power output. During transmit, voice modulation and CTCSS (or DCS) modulation are applied to this synthesizer. Transceiver functions, such as Tx/Rx control, PLL synthesizer settings, and channel programming, are controlled using the MPU.

Receiver

Incoming RF signals from the antenna connector are delivered to the MAIN Unit, and pass through a low-pass filter (LPF) antenna switching network consisting of coils L1011, L1012, L1014, and L1009 , capacitors C1017, C1024, C1029, C1030, C1034 and C1002, and antenna switching diodes D1032 and D1001 for delivery to the receiver front end.

Signals within the frequency range of the transceiver are then passed through a varactor-tuned band-pass filter consisting of T1001, T1002 before RF amplification by Q1006.

The amplified RF is then band-pass filtered again by varactor-tuned resonators T1003, T1004 to ensure pure in-band input to 1st mixer Q1040.

Buffered output from the VCO Unit is amplified by Q1027 and low-pass filtered by L1023 / L1020 and C1161 / C1152 / C1143, to provide a pure 1st local signal between 54.7 and 67.7 MHz to the 1st mixer.

The 17.7MHz 1st mixer product then passes through dual monolithic crystal filters XF1001 and XF1002 (12 kHz BW) is amplified by Q1035 and delivered to the input of the FM IF subsystem IC Q1034.

This IC contains the 2nd mixer, 2nd local oscillator, limiter amplifier, FM detector, noise amplifier, and squelch gates.

The 2nd LO in the IF-IC is produced from crystal OSC amp X1001,Q1033 (17.25MHz), and the 1st IF is converted to 450kHz by the 2nd mixer and stripped of unwanted components by ceramic filter CF1001 . After passing through a limiter amplifier, the signal is demodulated by the FM detector.

Demodulated receive audio from the IF-IC is amplified by Q2019. After volume adjustment by the AF power amplifier Q2018, the audio signal is passed to the optional headphone jack or 4 Ω loudspeaker.

PLL synthesizer

The 1st LO maintains stability from the PLL synthesizer by using a 17.7 MHz reference signal from crystal OSC amp X1001,Q1033. PLL synthesizer IC Q1029 consists of a prescaler, reference counter, swallow counter, programmable counter, a serial data input port to set these counters based on the external data, a phase comparator, and charge pump. The PLL-IC divides the 17.700 MHz reference signal by 885 using the reference counter (20.0 kHz comparison frequency). The phase detector comparison frequency to be eight times the channel spacing (5kHz). The VCO output is divided by the prescaler, swallow counter and programmable counter. These two signals are compared by the phase comparator and input to the charge pump. A voltage proportional to their phase difference is delivered to the low-pass filter circuit, then fed back to the VCO as a voltage with phase error, controlling and stabilizing the oscillating frequency. This synthesizer also operates as a modulator during transmit.

The RX-VCO is comprised two oscillator. The one is comprised of Q1015 and D1016, D1017, and oscillates between 54.7MHz and 61.199MHz. The another is comprised of Q1042 and D1038, D1039 and oscillated between 61.2MHz and 67.7MHz. The each VCO is programmed according to receiving frequency.

And the TX-VCO is comprised of Q1016 and D1012, D1013, D1014,D1015 and oscillates between 37.0MHz and 50.0MHz according to the programmed transmit frequency. The VCO output passes through buffer amplifier Q1021, and a portion is fed to the buffer amplifier Q1023 of the PLL IC, and at the same time amplified by Q1027 to obtain stable output. The VCO DC supply is regulated by Q1007. Synthesizer output is fed to the 1st mixer by diode switch D1022 during receive, and to drive amplifier Q1004 for transmit.

Transmitter

Voice audio from the microphone is delivered via the MIC (Jack) Unit to the MAIN Unit, after passing through amplifier Q3039/Q2041, pre-emphasis, limiter (IDC instantaneous deviation control), and LPF Q2001, is adjusted for optimum deviation level and delivered to the next stage.

Voice input from the microphone and CTCSS are FM-modulated to the VCO of the synthesizer, while DCS audio is modulated by the reference frequency oscillator of the synthesizer.
Synthesizer output, after passing through diode switch D1022, is amplified by driver Q1004 / Q1002 and power amp Q1001 to obtain full RF output. The RF energy then passes through antenna switch D1033, D1034 and a low-pass filter circuit and finally to the antenna connector.

RF output power from the final amplifier is sampled by CM coupler and is rectified by D1036, D1037. The resulting DC is fed through Automatic Power Controller Q1038 to transmitter RF amplifier and thus the power output.

Generation of spurious products by the transmitter is minimized by the fundamental carrier frequency being equal to the final transmitting frequency, modulated directly in the transmit VCO. Additional harmonic suppression is provided by a low-pass filter consisting of L1017 L1012, L1011 and C1102, C1098, C1088,C1034,C1030,C1029 and C1024, resulting in more than 60 dB of harmonic suppression prior to delivery to the RF energy to the antenna.

DCS Demodulator

DCS signals are demodulated on the MAIN-UNIT, and are applied to low-pass filter Q2040 as well as the limiter comparator Q2003.

CTCSS encoder/decoder

The CTCSS code is generation and encoding by MPU IC Q2025.
Demodulation and detection of the CTCSS tones are carried out by IC Q2017.

MPU

Operation is controlled by 16-bit MPU IC Q2025. The system clock uses a 16.000 MHz crystal for a time base. IC Q2035 resets the MPU when the power is on, and monitors the voltage of the regulated 5V power supply line.

EEPROM

The EEPROM retains Tx and Rx data for all memory channels and CTCSS data, DCS data, prescaler dividing, and REF oscillator data (internal/external).