VX-3200U Circuit Description

1. Overview
The VX-3200U is a UHF/FM mobile transceiver designed to operate in the frequency range of 450 to 490MHz.

2. Circuit Configuration by Frequency
The receiver is a double-conversion superheterodyne with a first intermediate frequency (IF) of 44.25MHz and a second IF of 450kHz. Incoming signals from the antenna are mixed with the local signal from PLL to produce the first IF of 44.25MHz.
This is then mixed with the 44.25MHz second local oscillator (using the 14.6MHz reference crystal) output to produce the 450kHz second IF. This is detected to give the demodulated signal.
The transmit signal frequency is generated by PLL VCO, and modulated by the signal from the microphone. It is then amplified and sent to the antenna.

3. Receive Signal Path
Incoming RF signals from the antenna connector are delivered to the RF Unit, and pass through a low-pass filter (LPF) antenna switching network consisting of coils L1001, L1003, L1004 and L1005, capacitors C1004, C1008, C1009, C1011, and C1014, and antenna switching diodes D1005 and D1007 for delivery to the receiver front end.
Signals within the frequency range of the transceiver are then passed through a varactor-tuned bandpass filter consisting of L1009, and L1014 before RF amplification by Q1011 (2SC4227).
The amplified RF is then band-pass filtered again by varactor-tuned resonators L1026, and L1027 to ensure pure in-band input to 1st mixer Q1025 (GN2011-Q).
Buffered output from the VCO Unit is amplified by Q1021 (2SC5107) and low-pass filtered by L1030 / L1031 and C1178 / C1180 / C1182, to provide a pure 1st local signal between 405.75 and 445.75MHz to the 1st mixer.
The 44.25MHz 1st mixer product then passes through dual monolithic crystal filters XF1001 and XF1002 (± 5.5 kHz BW), and is amplified by Q1029 (2SC4215Y) and delivered to the input of the FM IF subsystem IC Q1028 (TA31136FN).
This IC contains the 2nd mixer, 2nd local oscillator, limiter amplifier, FM detector, noise amplifier, and squelch gates.
The 2nd LO in the IF-IC is produced from crystal X1001 (14.600MHz) and the 1st IF is converted to 450kHz by the 2nd mixer and stripped of unwanted components by ceramic filter CF1001 or CF1002. After passing through a limiter amplifier, the signal is demodulated by the FM detector CD1001 (CDBC450CX24).
Detected audio from Q1029 is applied to Q2016 (AK2345) and audio low-pass filter. After volume adjustment by Q2014 (M62364FP), the audio signal is amplified by the AF power amplifier Q1509 (TDA2003H) and passed to speaker jack.

4. Transmit Signal Path
Voice audio from the microphone is delivered via the Mic (Jack) Unit to the PANEL Unit, after passing through amplifier Q2022 (NJM2902V), Mic gain-volume Q2014 (M62364FP) pre-emphasisQ2015 (NJM2902V), and limiter (IDC instantaneous deviation control), is adjusted for optimum deviation level and delivered to the next stage.
Voice input from the microphone and CTCSS are FM-modulated to the VCO of the synthesizer, while DCS audio is modulated by the reference frequency oscillator of the synthesizer.
Synthesizer output, after passing through diode switch D1022 (1SS321), is amplified by driver Q1025 (2SC5415E) / Q1026 (2SC5107) and power module Q1014 (RA45H4452M) to obtain full RF output. The RF energy then passes through antenna switch D1005 / D1007 and a low-pass filter circuit and finally to the antenna connector.
RF output power from the final amplifier is sampled by CM coupler and is rectified by D1011, D1012 (HSM88AS x 2). The resulting DC is fed through Automatic Power Controller Q1003 (M5223AGP), Q1002 (2SC4154E), Q1032 (2SC4254E), and TH1003 to transmitter RF amplifier and thus the power output.
Generation of spurious products by the transmitter is minimized by the fundamental carrier frequency being equal to the final transmitting frequency, modulated directly in the transmit VCO. Additional

harmonic suppression is provided by a low-pass filter consisting of L1001, L1003, L1004, C1004, C1008, C1009, C1011 and C1014, resulting in more than 60dB of harmonic suppression prior to delivery to the RF energy to the antenna.

5 PLL Frequency Synthesizer

PLL frequency synthesizer consists of the VCO Q1013 (2SK508-K52:RX) and Q1015 (2SC4226-R24:TX), VCO buffers Q1018 (2SC5107-0), Q1020 (2SC5107-0), Q1021 (2SC5107-0), PLL subsystem IC Q1023 (MA15A02PFV1) and 14.6MHz reference crystal X1001.

The frequency stability is ± 2.5ppm within temperature range of –30 to +60 °C. The output of the 14.6MHz reference is applied to pin 1 of the PLL IC.

While receiving, VCO Q1013 oscillates between 405.75 and 445.75MHz according to the transceiver version and the programmed receiving frequency. The VCO generates 405.75 to 445.75MHz for providing to the first local signal. In TX, the VCO generates 450 to 490MHz.

The output of the VCO is amplified by the Q1020 and routed to the pin 8 of the PLL IC. Also the output of the VCO is amplified by the Q1021 and routed first local /Power Module according to D1022.

The PLL IC consists of a prescaler, fractional divider, reference divider and phase comparator and charge pump. This PLL IC is fractional-N type synthesizer and performs in the 40 or 50kHz reference signal, which is eighth of the channel step (5 or 6.25kHz). The input signal from pin 1 and 8 of the PLL IC is divided down to the 20kHz and compared at phase comparator. The pulsed output signal of the phase comparator is applied to the charge pump and transformed into DC signal in the loop filter. The DC signal is applied to the pin 1 of the VCO and locked to keep the VCO frequency constant.

PLL data is output from DCS_E (pin100), CLOCK (pin2) and PLL_E (pin98) of the microprocessor Q2013. The data are input to PLL IC when the channel is changed or when transmission is changed to reception and vice versa. A PLL lock condition is always monitored by the pin20 of the Q2013. When the PLL is unlocked, the UL goes low.

6. Miscellaneous Circuits

6-1 DCS Demodulator

DCS signals are demodulated on the PANEL-UNIT, It is demodulated by Q2116 (AK2345), amplifier Q2015, and comparator Q2021.

6-2 CTCSS encoder/decoder

The CTCSS code is generation and encoding by CTCSS encoder/decoder IC Q2016 (AK2345).

6-3 MPU

Operation is controlled by 8-bit MPU IC Q2013 (LC87F72C8A). The system clock uses a 3.6864MHz crystal for a time base. IC Q2003 (S-80735SN) resets the MPU when the power is on, and monitors the voltage of the regulated 5V power supply line