Circuit description

RECEIVER

1, Receive Signal Path

Incoming signals within the frequency range of the transceiver from the antenna jack is delivered to the RF UNIT and passes through a low-pass filter and band-pass filter consisting of coils L1026, L1027, L1028, L1020, L1015 and L1016 , capacitors C1127, C1128, C1130, C1131, C1092, C1278, C1279, C1280, C1033, C1051, C1275, C1281, C1282 and C1283 and antenna switching diode D1008 (RLS135).

Then amplified by Q1008 (2SC5226) and enter a varactor-tuned band-pass filter consisting ofcoils L1009, L1010, L1011 & L1012, capacitors C1053, C1039, C1040, C1054, C1034, C1041, C1035, C1042, C1055, C1043, C1036, C1044, C1061, C1062, C1045, C1046, C1056, and C1018 before first mixing by Q1005 (SGM2016M).

Buffered output from the VCO is amplified by Q1019 (2SC5226) to providea pure first local signal between 326.65 MHz and 438.65 MHz for injection to the first mixer Q1005 (SGM2016M). The 73.35 MHz first mixer product then passes
through monolithic crystal filters XF1001 (73S10A 10 kHz BW), then amplified by Q1005 (2SC5226), which is then XF1002 (73S10A 10 kHz BW) to strip away all but the desired signal.

The amplified first IF signal is applied to FM IF subsystem IC Q1009 (TA31136FN), which contains the second mixer, second local oscillator, limiter amplifier, noise amplifier, and S-meter amplifier.

A second local signal is generated the 72.895 MHz crystal X1001 to produce the 455 kHz second IF when mixed with the first IF signal within Q1009.

The second IF then passes through the ceramic filter CF1001 (PBFS455P9DR) or CF1002 (PBFS455P12DR) to strip away unwanted mixer products, and is applied to the limiter amplifier in Q1008, which removes amplitude variations in the 455 kHz IF, before detection of the speech by the ceramic discriminator CD1001 (CDBC450C24X).

Detected audio from Q1009 is applied to Q1048 for de-emphasis and band-pass filtering and then past the volume control to the audio power amplifier Q1045 (TDA1519A) on the RF

UNIT, providing up to 10 Watts to the optional external speaker jack or 4 Ω loudspeaker.

2, Squelch Control

The squelch circuitry consists of a noise amplifier & band-pass filter within Q1009, and amplifier Q1006 (2SC4116) before the noise detector D1001 and D1002 (MA143).

When no carrier is received, noise at the output of the detector stage in Q1009 is amplified and band-pass filtered by the noise amplifier section of Q1009 and the network between pins 7 and 8, and noise amplifier Q1006 then rectified by D1001 and D1002 (MA143).
The resulting DC squelch control voltage is passed to pin 30 of the microprocessor Q1046. If no carrier is received, this signal causes pin 52 of Q1045 to low, and pin 53 of Q1046 to high. Pin 53 signals Q1049 (UN5213) ON then mute the audio amplifier Q1045, while pin 52 makes turn off the audio switch Q1047 (TC4S66F) .

Thus, the microprocessor blocks output from the audio amplifier, and silences the receiver while no signal is being received, and during transmission.

When a carrier appears at the discriminator, noise is suppressed from the output, when nise amplified and inputed to A/D converter (Q1046). if A/D converted data is comparated the squelch data then small, this signal causes pin 52 of Q1046 to high, and pin 53 of Q1046 to low. Pin 53 signals Q1049 (UN5213) OFF then unmute the audio amplifier Q1045, while pin 52 makes turn on the audio switch (Q1047 ,TC4S66F) .

While receiving, detected audio from Q1009 is de-emphasized and amplified by the Q1048 de-emphasis amplifier section, and then band-pass filtered by the Q1048 band-pass filter section. If the audio is scrambled by inverting the voice band, it then passes through the voice band inverter section within Q1048 to recover clear speech.

The microprocessor and base-band processing IC,s (Q1046, Q1048), the received tone or code matches that programmed, the microprocessor stops scanning, if active, and allows audio to pass through the audio amplifier Q1045 (TDA1519A) to the loudspeaker.

TRANSMITTER

1, Transmit Signal Path

Speech input from the microphone is delivered to the FRONT UNIT, where it is amplified by Q1048 (SC11372), Q1048 (SC11372) is include pre-emphasis,limitter and lowpass filter.

The pre-emphasized audio then returns to the Q1048, to provide IDC (Instantaneous Deviation Control), and the splutter filter which filters the speech signal to suppress any high frequency spectrum that might result in over-deviation.

The processed audio is delivered to D1021 (1SV270) for frequency modulating the PLL carrier up to ± 2.5 kHz or ±5kHz from the unmodulated carrier at the transmitting frequency.

If a CDCSS code or CTCSS code is enabled for transmission, the code is generated by the microprocessor Q1046 ,base-band Q1048 and delivered to D1024 (HVU350) for CDCSS and CTCSS modulating.

If DTMF is enabled for transmission, the tone is generated and applied to the splutter filter section in place of speech audio by the base-band IC Q1048. Also, the tone is amplified for monitoring in the loudspeaker.

The modulated signal from the VCO Q1034 (2SK508) is buffered by Q1019 (2SC5226), amplified by Q1017 and Q1014 (2SC5019), pre driver Q1016 (2SK2596), driver Q1018 (MRF5015) and RF power amplified Q1015 (SRF-7044) up to 40watts rf output power.

The transmit signal then passes through the antenna switch D1010 (UM9401) and is low-pass filtered to suppress away harmonic spurious.

2, Automatic Power Control (APC)

RF power output from the final amplifier is sampled by C1129, C1132 and is rectified by D1015 (1SS319). The resulting DC is fed back through and power control DC volt input to comparetor Q1027 (TA75S01). the comparetor output voltage is drived Q1028 (2SC4116), then pre drive (Q1016) supply voltage controlled for Q1022 (2SB1201) .

The microprocessor selects either high or one of two low power levels.

3, Transmit Inhibit

When the transmit PLL is unlocked, pin 7 of PLL chip Q1021 goes to a logic low. unlock signal drived Q1010 (2SA1586) and Q1011 (DTC114TK), then Q1011 output is logic high. The resulting DC unlock control voltage is passed to pin 14 of the microprocessor Q1046. While the transmit PLL is unlocked, pin 62 of Q1046 remains high, which then turns off the taransmitter for power supply switch Q1039 (XN1213) and Q1037 (2SB1201). disable the transmitter .

4, Spurious Suppression

Generation of spurious products by the transmitter is minimized by the fundamental carrier frequency being equal to the final transmitting frequency, modulated directly in the transmit VCO. Harmonic spurious suppression is provided by a low-pass filter consisting of L1026. L1027 & L1028 and C1127, C1128, C1130 and C1131. Resulting in more than 60 dB of harmonic suppression prior to delivery to the antenna.

PLL Frequency Synthesizer

1, Frequency Reference

Stability is maintained by a regulated 5V supply via Q1026 (2SB1132) and Q1033 (MM1216). The 14.4MHz frequency reference crystal X1002whith in temperature compensationg. high temparature compensatio for thermister TH1001 (NTCCM20123NH153) and Q1060 (2SC4116), low temparature compensation for thermister TH1002 (NTCCM20123SH223) and Q1061 (2SA1586).

2, Synthesizer

PLL circuitry on the RF UNIT consists of VCO Q1020 (2SK508), Q1034 (2SK508) and VCO buffers Q1019 (2SC5226). PLL subsystem IC Q1021 (MB15A02), which contains a reference divider. serial-to-parallel data latch. programmable divider. phase comparator, charge pump.

While receiving, VCO Q1020 (2SK508) oscillates between 326.65 MHz and 438.65 MHz accordingto the transceiver version and the programmed receiving frequency. The VCO output is buffered by Q1019 (2SC5226) and applied to the prescaler section of Q1021

(MB15A02). There the VCO signal is divided by 64 or 65 and 128 or 129, according to a control signal from the data latch section of Q1021 (MB15A02), before being applied to the programmable divider section of Q1021 (MB15A02).

The data latch section of Q1021 also receives serial dividing data from the microprocessor Q1048 on the RF UNIT, which causes the pre-divided VCO signal to be further divided in the programmable divider section, depending upon the desired receive frequency, so as to produce a 5 kHz or 6.25 kHz or 7.5kHz and 10kHz or 12.5kHz or 15kHz derivative of the current VCO frequency.

Meanwhile, the reference divider section of Q1021 divides the 14.4MHz crystal reference from the reference oscillator Q1031.

The 5 kHz (or 6.25 kHz or 7.5kHz) signal from the programmable divider (derived from the VCO) and that derived from the reference oscillator are applied to the phase detector section of Q1021, which produces a pulsed output with pulse duration depending on the phase difference between the input signals.

This pulse train is filtered to DC and returned to the varactor D1012,D1013,D1014,D1015 (HVU350). Changes in the level of the DC voltage applied to the varactor, affect the reactance in the tank circuit of the VCO, changing the oscillating frequency of the VCO according to the phase difference between the signals derived from the VCO and the crystal reference oscillator.

The VCO is thus phase-locked to the crystal reference oscillator. The output of the VCO Q1020, after buffering by Q1019, is applied to the first mixer, as described previously.

For transmission, the VCO Q1034 oscillates between 400 MHz and 512 MHz according to the model version and programmed transmit frequency. The remainder of the PLL circuitry is shared with the receiver. However, the dividing data
from the microprocessor is such that the VCO frequency is at the actual transmit frequency (rather than offset for IFs, as in the receiving case). Also, the VCO is modulated by the speech audio applied to D1021 (1SV270), asdescribed previously.